Digital Amplifier TAS57xx Family Deep Dive

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Texas Instruments

About This Slides

- This slide gives detail and advanced descriptions for TAS57xx devices, some examples are also provided to help customer to do programming.
- The method and function provided in this slides are mostly based on TAS5706. However, most of functions for the device in TAS57xx family are the same, take this slides for your reference.
- This slide is suitable for experienced FAE and customer engineer.

TAS57XX MCU EVM Design Review

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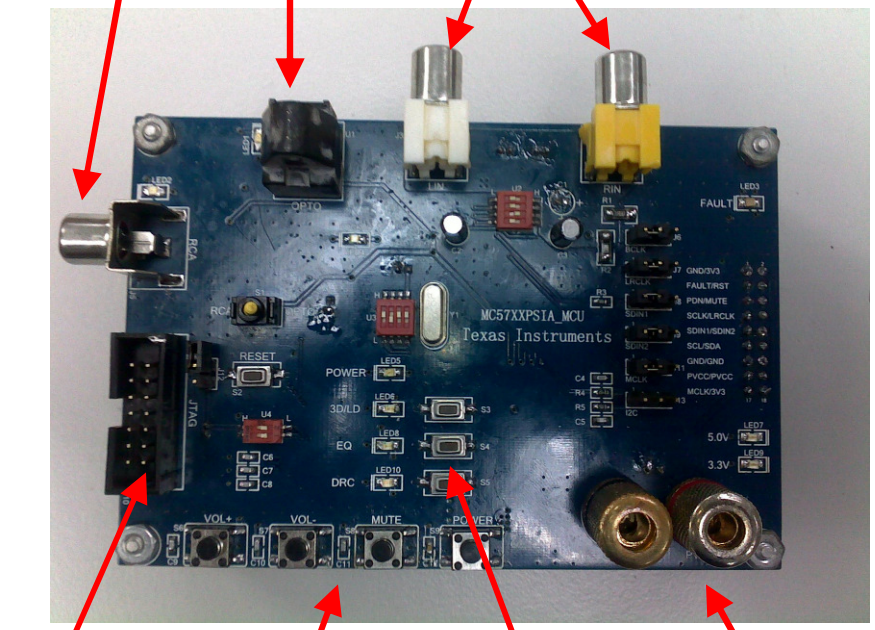
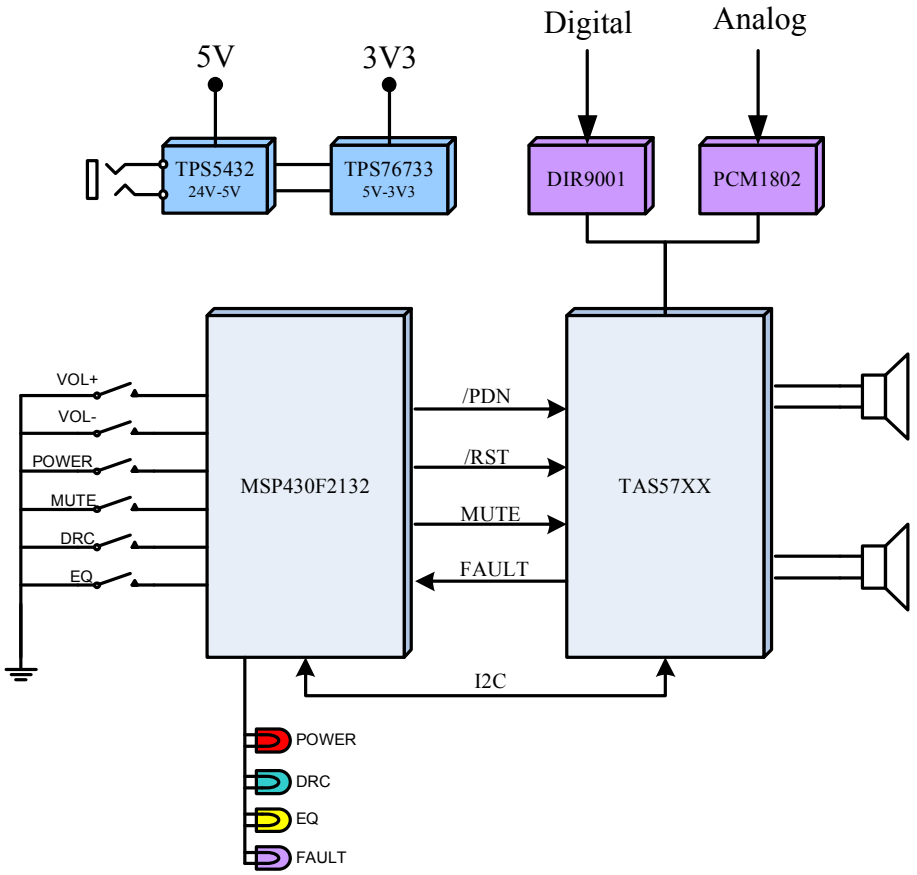
TAS57XX MCU EVM Project Overview





What's the diff. between GDE and MCU Ver.

GDE Version	MCU Version
Advantages	*Advantages*
1. Integrated EQ, DRC parameters generator GUI. 2. Can modify register parameters by User. 3. Graphic User Interface is preferred by some customers.	1. Stand alone demo board running without PC. 2. TI can provide sample code for customer now. 3. Demo EQ, DRC, Loudness by press only one button. 4. Support All standard TAS57XX EVM daughter board. 5. Integrated swift DC/DC controller, only one PVCC is required. 6. ADC is replaced by PCM1802 with better performance for test. 7. TI FAE can evaluate different timing sequence on this EVM.
Disadvantages	*Disadvantages*
1. Must have PC to demo our device to customer. 2. Take more time when adjust EQ, DRC during demo. 3. Can't provide coding guidance to customer 4. Can't test exactly startup/shut down sequence 5. AVCC and PVCC two power rails are needed.	1. Must need GDE to generate EQ, DRC etc.. parameters. 2. Only engineer familiar with coding can modify register setting. 3. Can't support GDE software.

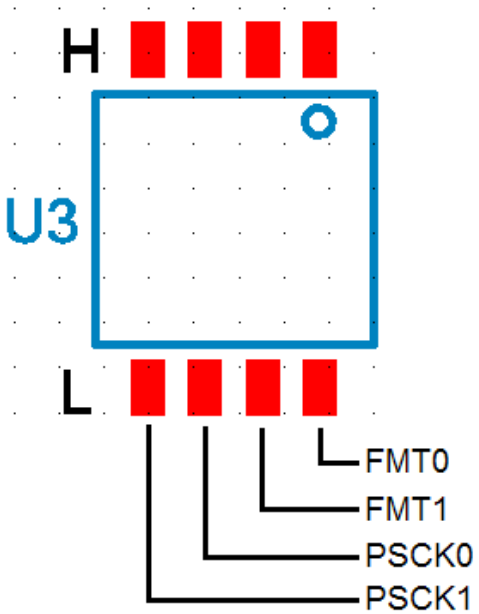
Next Version combined all advantages: TAS57XX MCU EVM with TAS1020B

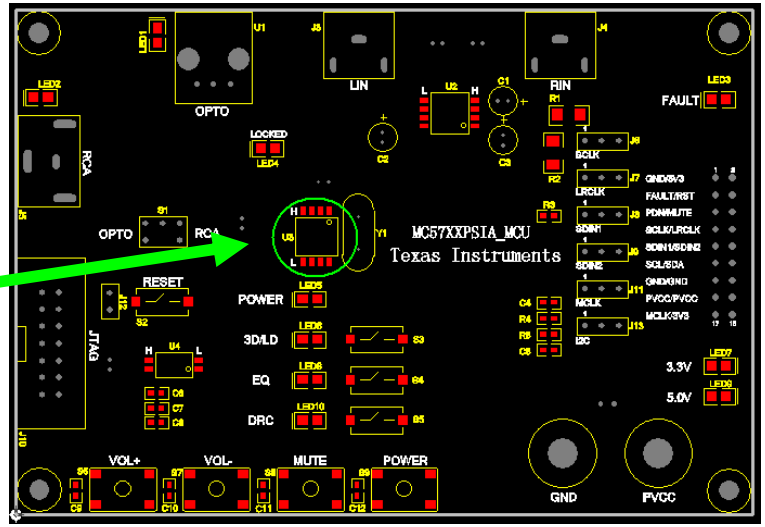
1. Integrate TAS1020B in TAS57XX MCU EVM to support GDE software control from USB.
2. I2C Jumpers are provided to select control source, from GDE USB control or MCU stand alone control.

Nice to have:

1. TAS1020B support USB I2S converting, provide USB audio input function.

I2S Format Select Switch

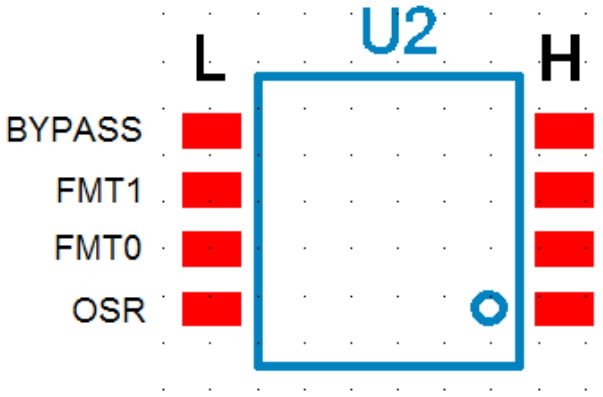


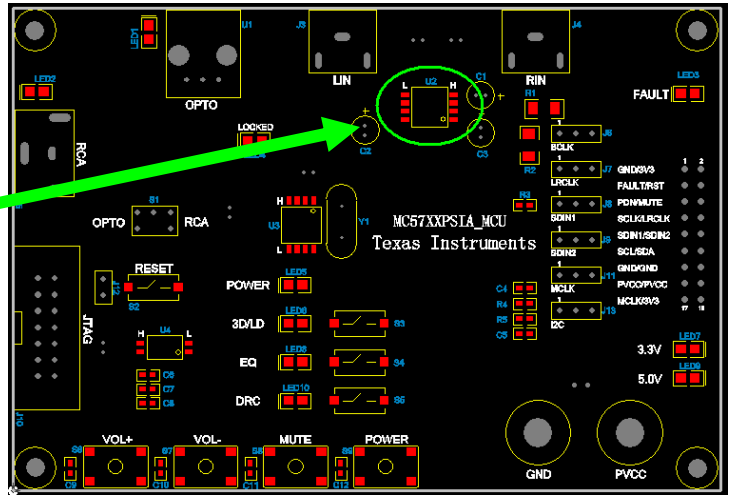


FMT1	FMT0	S/PDIF DOUT FORMAT
L	L	16-bit, MSB-first, right-justified
L	H	24-bit, MSB-first, right-justified
H	L	24-bit MSB-first, left-justified
H	H	24-bit, MSB-first, I2S

PSCK[1:0] SETTING		OUTPUT CLOCK FROM PLL SOURCE		
PSCK0	**PSCK1**	**SCKO**	**BCKO**	**LRCK**
L	L	128fs	64fs	fs
L	H	256fs	64fs	fs
H	L	384fs	64fs	fs
H	H	512fs	64fs	fs

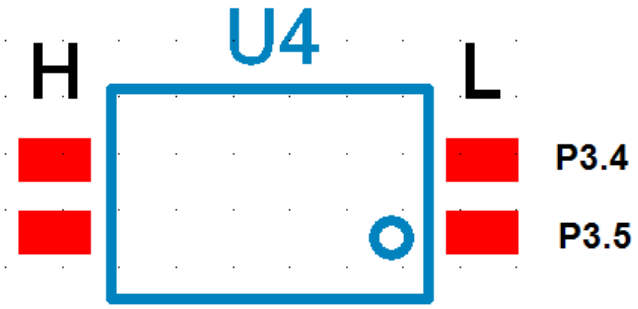
ADC I2S Format Select Switch

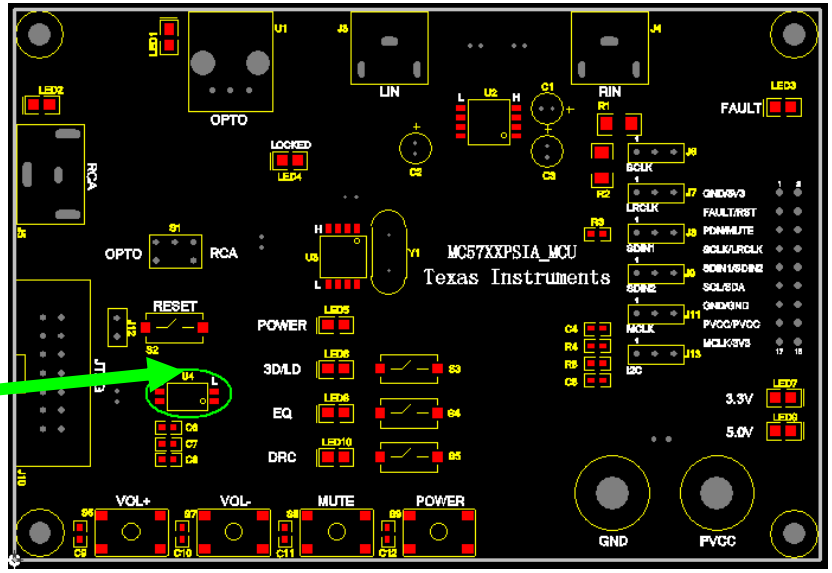




FMT1	FMT0	ADC DOUT FORMAT
L	L	Left-justified, 24-bit
L	H	I2S, 24-bit
H	L	Right-justified, 24-bit
H	H	Right-justified, 20-bit
BYPASS		**HPF(HIGH-PASS FILTER) MODE**
L		Normal (no dc component on DOUT) mode
H		Bypass (dc component on DOUT) mode
OSR		**OVERSAMPLING RATIO**
L		64fs
H		128fs (fs<50kHz)

Output Type Selector





P3.4	P3.5	OUTPUT TYPE
L	L	2.0 Channel Output
L	H	2.1 Channel Output
H	L	2.1 (external) Channel Output
H	H	4.0 Channel Output

Firmware 1.0 function list

- All function is based on TAS5706 now.
- 2.0 / 2.1 output has been supported.
- EQ, DRC demo for 2.0/2.1 is ok now.
- All Volume and Power control key function is OK.

- Already demo to customer successfully.

Device ID Version Check

- All devices in TAS57xx family have Device ID, stored in 0x01 register.
- Same Device ID means basic functions provided are the same. (Unless disabled on purpose)

Firmware Ver.	Device P/N
0x23	TAS5705
0x28	TAS5706
0x2A	TAS5706A/TAS5706B/TAS5716
0x68	TAS5708
0x70	TAS5707/TAS5709 /TAS5710
???	TAS5711

- Where I can find firmware version information?

---- Check this register in datasheet: “Device ID register”

0x01	Device ID register	1	Description shown in subsequent section	0x28

I2S-Input Family Comparison Matrix

Device	Closed Loop	PVDD	BQs	DRC	SE 2.1	PWM Outs	Robust DC Protection	3D/Bass Boost	Audio Input Ports	Package
TAS5704 (H/W Ctrl) (20W)	Yes	10 to 26V	-	-	-	1x	-	-	2x (32–192kHz)	10x10mm 64- HTQFP
TAS5705 (20W)	-	8 to 23V	18	2x	-	2x	-	-	2x (32–192kHz)	10x10mm 64- HTQFP
TAS5706A/B (20W)	Yes	10 to 26V	18	2x	Yes	2x	-	-	2x (32–192kHz)	10x10mm 64- HTQFP
TAS5716 (20W)	Yes	10 to26V	18	2x	Yes	2x	-	Yes	2x (32–192kHz)	10x10mm 64- HTQFP
TAS5707 (20W)	-	8 to 26V	14	1x	-	-	-	-	1x (8–48kHz)	7x7mm 48- HTQFP
TAS5708 (20W)	Yes	10 to 26V	14	1x	-	-	-	-	1x (8–48kHz)	7x7mm 48- HTQFP
TAS5709 (20W)	-	8 to 24V	22	2-band	-	-	-	Yes (Best)	1x (8–48kHz)	7x7mm 48- HTQFP
TAS5710 (20W)	Yes	10 to 26V	22	2-band	-	-	-	Yes (Best)	1x (8–48kHz)	7x7mm 48- HTQFP
TAS5711 (20W)	-	8 to 26V	21	2-band	Yes	-	-	Yes (Best)	1x (8–48kHz)	7x7mm 48- HTQFP
TAS5713 (25W) (110mΩ FETS)	-	8 to 26V	18	2-band (Best)	-	-	-	Improved Bass Boost	1x (8–48kHz)	7x7mm 48- HTQFP
TAS5715 (25W) (110mΩ FETS)	-	8 to 26V	16	2-band (Best)	-	1x	Yes	Improved Bass Boost	1x (8–48kHz)	7x7mm 48- HTQFP

P2P/Footprint Compatible **P2P/Footprint Compatible** **P2P/Footprint Compatible**

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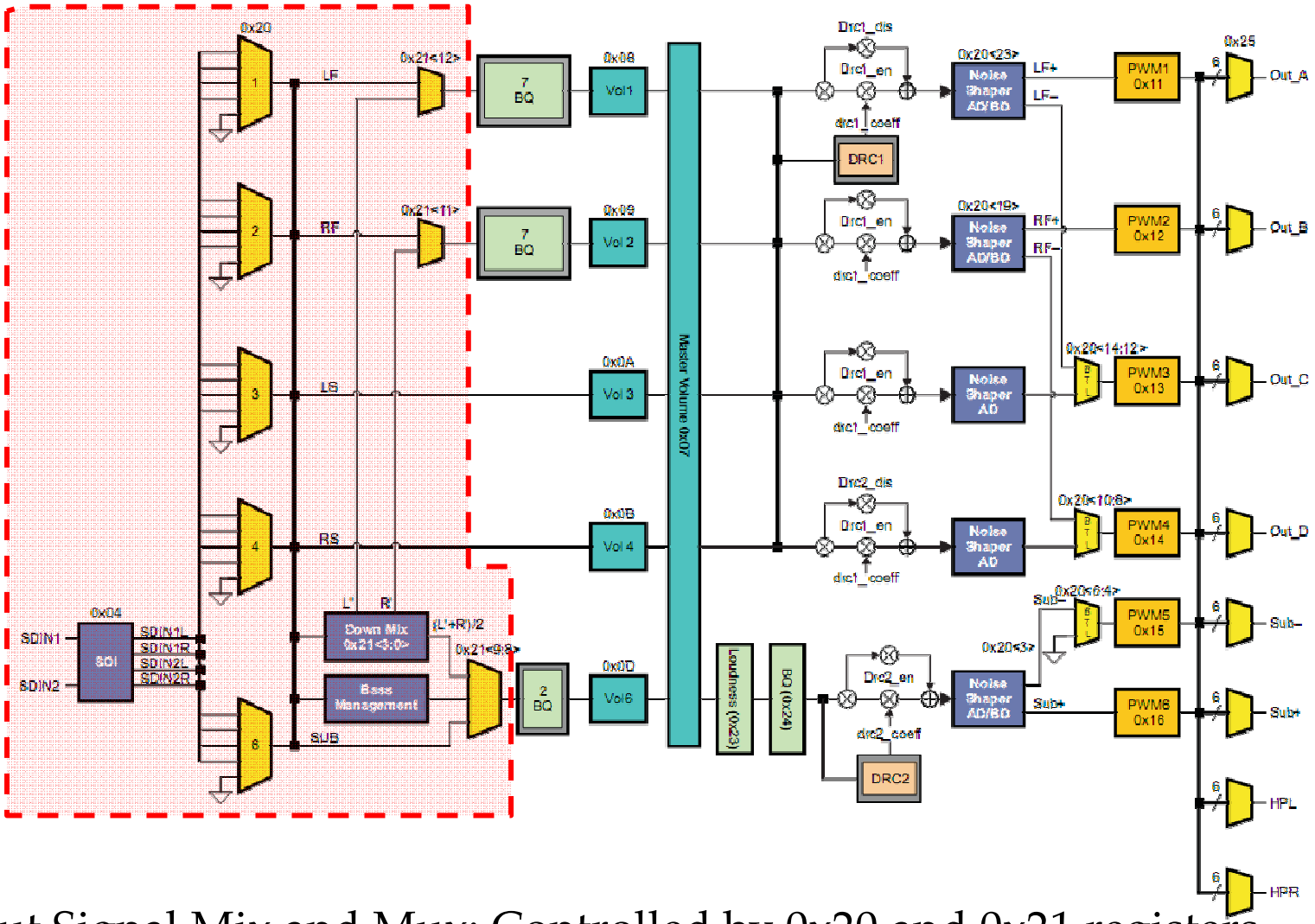
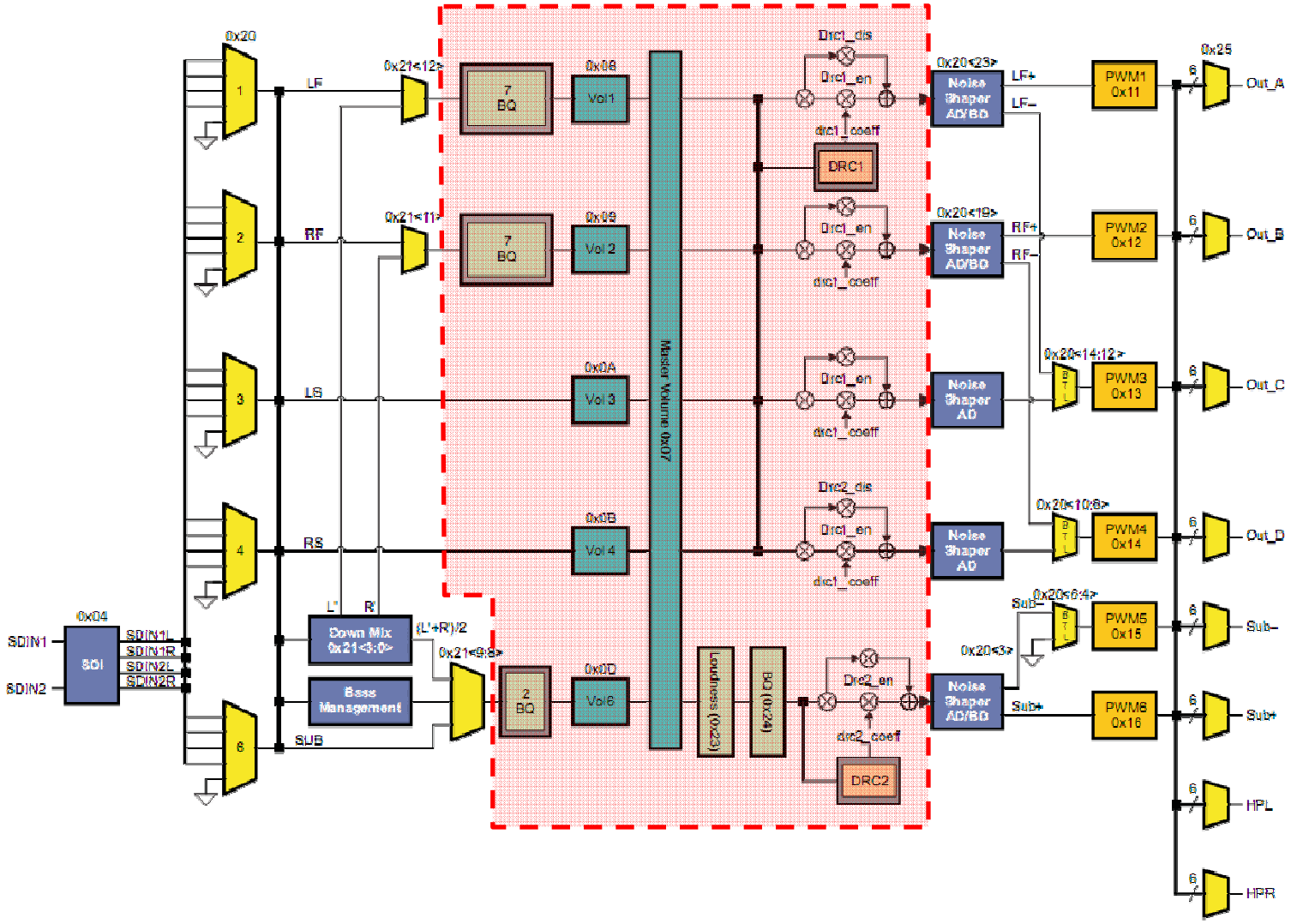
Typical Signal Flow of TAS57XX

Get Started with Typical Signal Flow of TAS57xx



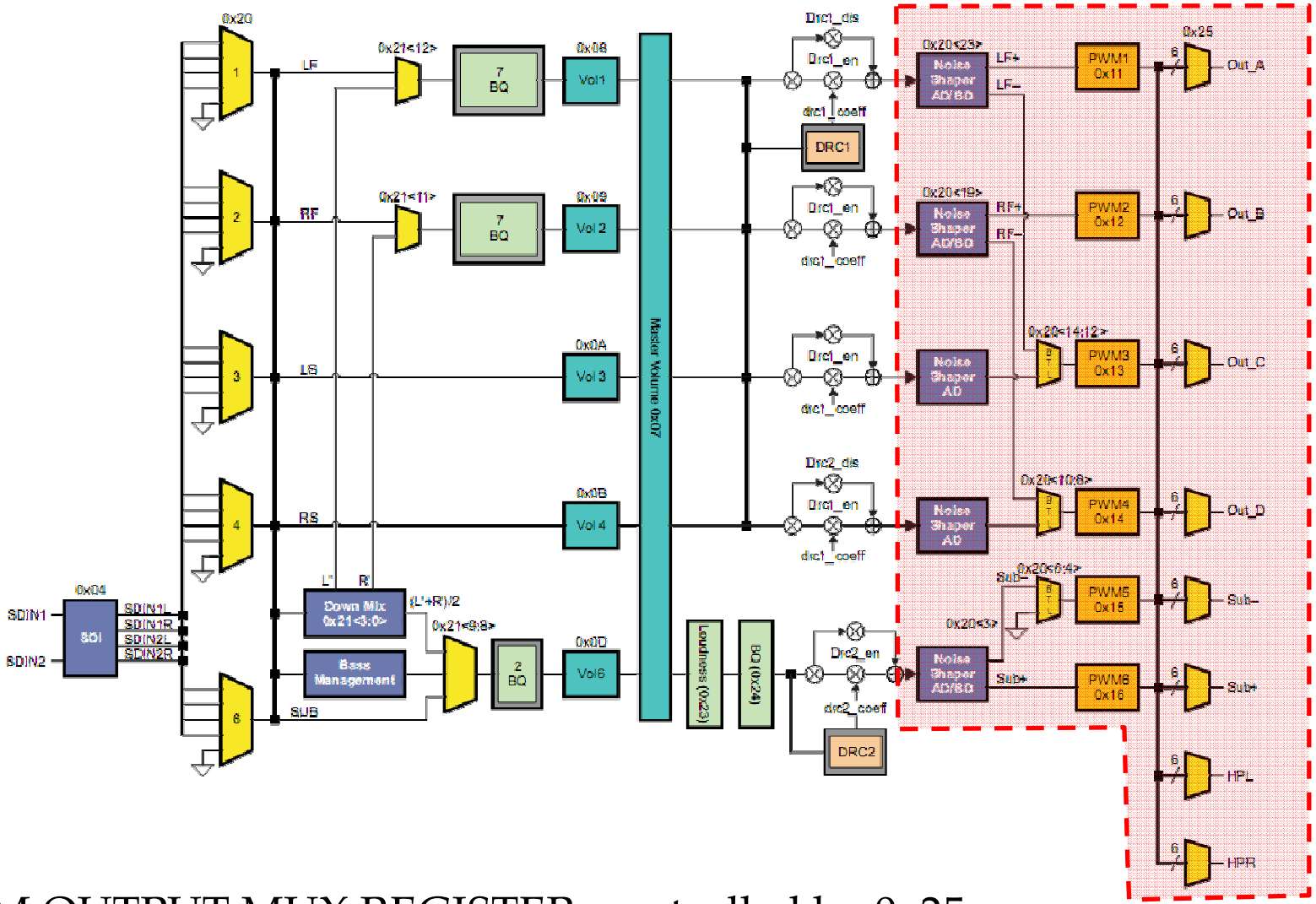
Input Signal Mix and Mux: Controlled by 0x20 and 0x21 registers

Get Started with Typical Signal Flow of TAS57XX



Internal DAP channel blocks provide EQ, Vol, DRC, Loudness functions.

Get Started with Typical Signal Flow of TAS57XX



PWM OUTPUT MUX REGISTER, controlled by 0x25.

Critical Registers Setting

INPUT MUX and DOWN MIX REGISTERS

Register: 0x20
Register: 0x21

Critical Register Setting ---- 0x20

0x20, INPUT MULTIPLEXER REGISTER

Invert Output Phase

Table 19. Input Multiplexer Register (0x20)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	0	–	–	–	–	–	–	**Reserved = 0x00**
		0						**Do not negate Ch6 volume in speaker mode**
		1						Negate Ch6 volume in speaker mode (1)
			0					**Do not negate Ch5 volume in speaker mode**
			1					Negate Ch5 volume in speaker mode (1)
				0				**Do not negate Ch4 volume in speaker mode**

[D31:D24] Output Phase Negative Function On/Off

Set these bits to 1 means that channel output phase is inverted by 180degree. This function is used in Single Ended output, to avoid supply pumping effect. Remember speaker wire connection MUST be inverted to make sure outputs keep in phase.

Example:

CH1 and CH2 are configured to SE output, CH6 is Bass channel.

Set [D31:D24] to 0x01 to inverter CH1 output. CH1 and CH2 are now 180degree reversed. CH1 negative and positive speaker wires must be exchanged.

Critical Register Setting ---- 0x20

0x20, INPUT MULTIPLEXER REGISTER

Input Signal Routing

D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
0	–	–	–	–	–	–	–	Channel-1 AD mode
1	–	–	–	–	–	–	–	**Channel-1 BD mode** (2)
–	**0**	**0**	**0**	–	–	–	–	**SDIN1-L to channel 1** (2)
–	0	0	1	–	–	–	–	SDIN1-R to channel 1
–	0	1	0	–	–	–	–	SDIN2-L to channel 1
–	0	1	1	–	–	–	–	SDIN2-R to channel 1
–	1	0	0	–	–	–	–	Reserved
–	1	0	1	–	–	–	–	Reserved
–	1	1	0	–	–	–	–	Ground (0) to channel 1

[D23:D00] Input Signal Routing Configuration

For CH1, CH2, CH6

These bits are used to set which I2S input data is connected to which internal channel, and also switching mode selection, AD or BD mode.

For Single-ended channel, AD mode MUST be selected.

For BTL or PBTL channel, AD or BD mode both works.

Critical Register Setting ---- 0x20

0x20, INPUT MULTIPLEXER REGISTER

BTL Configuration

Table 19. Input Multiplexer Register (0x20) (continued)

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
0	–	–	–	–	–	–	–	**Reserved**
–	0	0	0	–	–	–	–	SDIN1-L to channel 3
–	0	0	1	–	–	–	–	SDIN1-R to channel 3
–	0	1	0	–	–	–	–	SDIN2-L to channel 3
–	0	1	1	–	–	–	–	SDIN2-R to channel 3
–	1	0	0	–	–	–	–	Reserved
–	1	0	1	–	–	–	–	Reserved
–	1	1	0	–	–	–	–	Ground (0) to channel 3
–	**1**	**1**	**1**	–	–	–	–	**Ch1 (BTL–) to channel 3—BTL pair for channel 1** (3)
		–						**ed** (3)

[D23:D00] Input Signal Routing Configuration

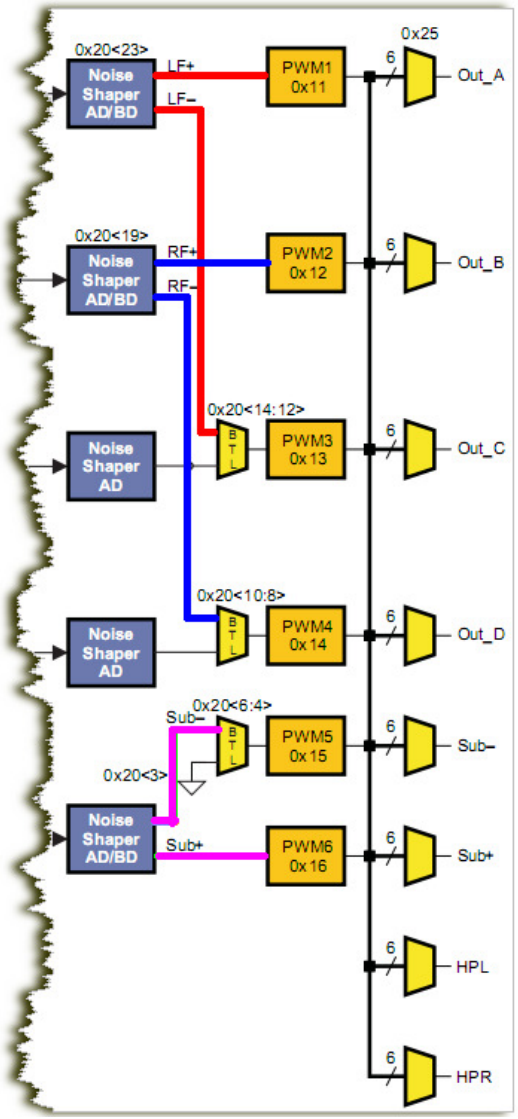
For CH3, CH4, CH5

Beside I2S data can be routed to CH3, CH4, CH5. The BTL- signal of CH1, CH2, CH6 are also can be routed to them, to form a BTL output.

Critical Register Setting ---- 0x20

0x20, INPUT MULTIPLEXER REGISTER

BTL Configuration



BTL Pair Channels Setting:

Source PWM CHs	BTL Pair PWM CHs
PWM1	PWM3
PWM2	PWM4
PWM6	PWM5

- BTL Channel signal flow are marked in left picture.
- PWM Channels can be routed to OUTA,B,C,D at random.

Example:

- Select option in red box to make PWM1 and PWM3 as BTL Pair.

Ground (0) to channel 3

Ch1 (BTL–) to channel 3—BTL pair for channel 1 (3)

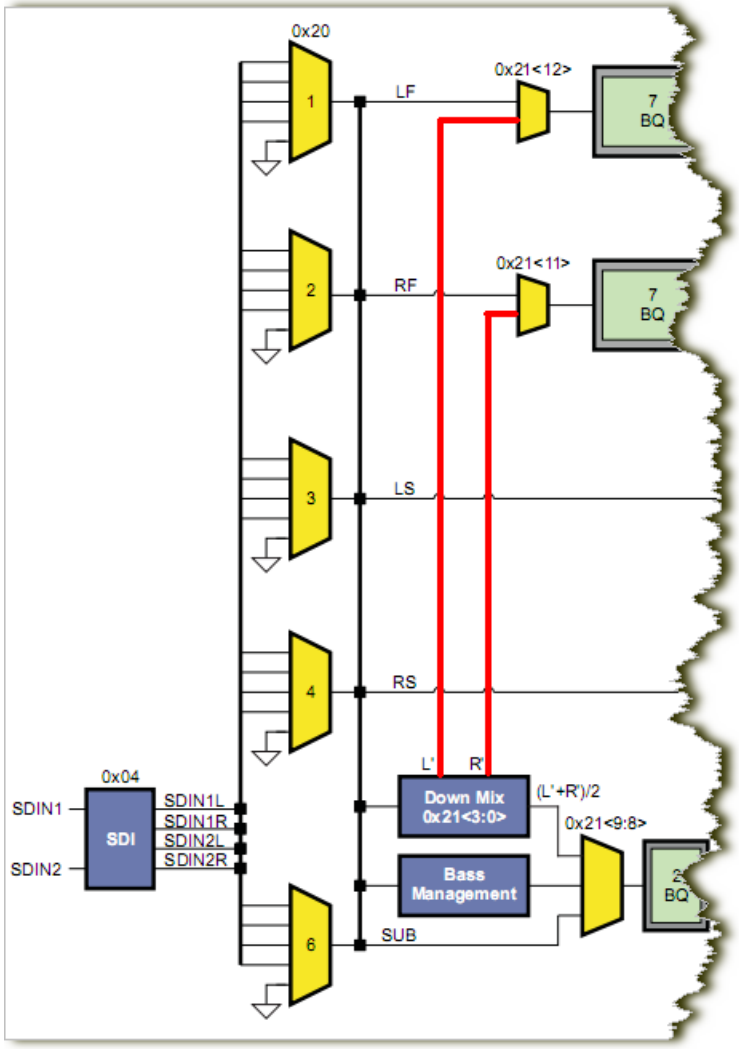
Reserved (3)

SDIN1-L to channel 4

Critical Register Setting ---- 0x21

0x21, DOWNMIX INPUT MUX REGISTER

What's Downmix



L' and R' are downmix from input CH1 ~ CH4. Below table shows formula for each configure.

Usually, no. 2 and 6 are often used in normal condition.

That's

L'=L=CH1 input

R'=R=CH2 input

NO.	Bits 3:0	Definition
1	X0X0	L' = (0.000 × Ls + 0.000 × L) / 1.000
2	**X0X1**	**L' = (0.000 × Ls + 1.000 × L) / 1.000**
3	X1X0	L' = (1.000 × Ls + 0.000 × L) / 1.000
4	X1X1	L' = (0.707 × Ls + 1.000 × L) / 1.707
5	0X0X	R' = (0.000 × Rs + 0.000 × R) / 1.000
6	**0X1X**	**R' = (0.000 × Rs + 1.000 × R) / 1.000**
7	1X0X	R' = (1.000 × Rs + 0.000 × R) / 1.000
8	1X1X	R' = (0.707 × Rs + 1.000 × R) / 1.707

Critical Register Setting ---- 0x21

0x21, DOWNMIX INPUT MUX REGISTER

Downmix Setting

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
0	**1**	**0**	–	–	–	–	–	**Reserved** (1)
–	–	–	1	–	–	–	–	Enable downmix data L' to channel 1
–	–	–	**0**	–	–	–	–	**Enable channel 1 data to channel 1** (1)
–	–	–	–	1	–	–	–	Enable downmix data R' to channel 2
–	–	–	–	**0**	–	–	–	**Enable channel 2 data to channel 2** (1)
–	–	–	–	–	**0**	–	–	Reserved
–	–	–	–	–	–	0	0	Enable channel 6 data to channel 6
–	–	–	–	–	–	0	1	Enable bass management on channel 6
–	–	–	–	–	–	**1**	0	**Enable (L'+R')/2 downmix data on channel 6** (1)
–	–	–	–	–	–	–	1	

[D15:D8] Select internal CH1, CH2, CH6 input source

These bits are used to choose input source for internal DAP channel 1, 2 and 6.

- DAP CH1 has two options: L' or Mux CH1
- DAP CH2 has two options: R' or Mux CH2
- DAP CH6 has three options: Mux CH6 or Bass management or (L'+R')/2

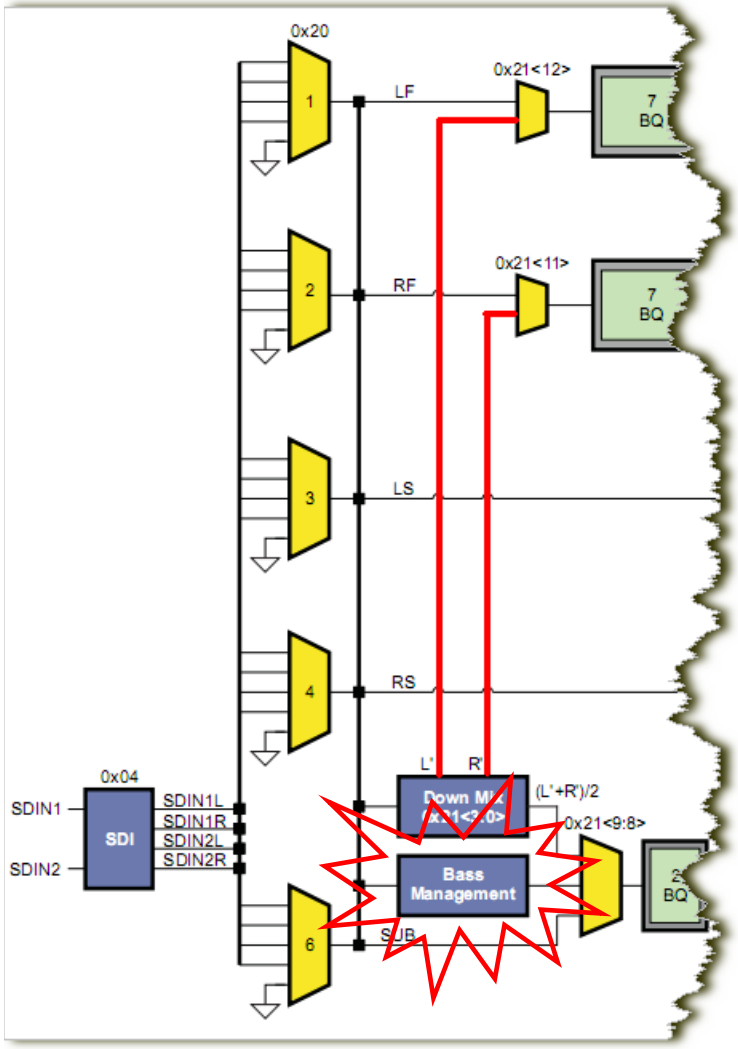
Usually:

- DAP CH1 = Mux CH1 for left channel
- DAP CH2 = Mux CH2 for right channel
- DAP CH6 = (L' + R')/2 for subwoofer channel. * Note: Usually used in 2.1CH configuration.

Critical Register Setting ---- 0x21

0x21, DOWNMIX INPUT MUX REGISTER

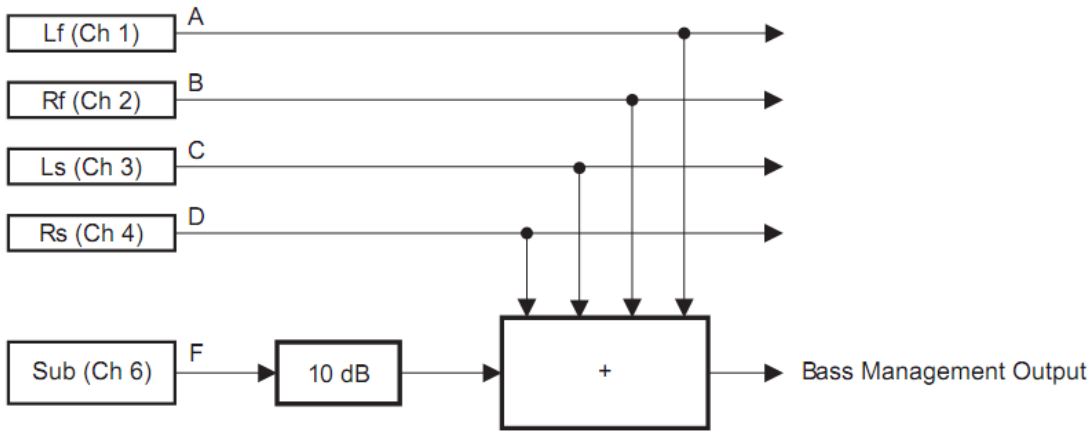
Bass Management for CH6



One of DAP CH6 Input Configuration is:

Bass Management

which is explained as below:



Bass Management Output = BS_Out (linear) = Ch 6 = F × 3.121 + (A + B + C + D)

Critical Registers Setting

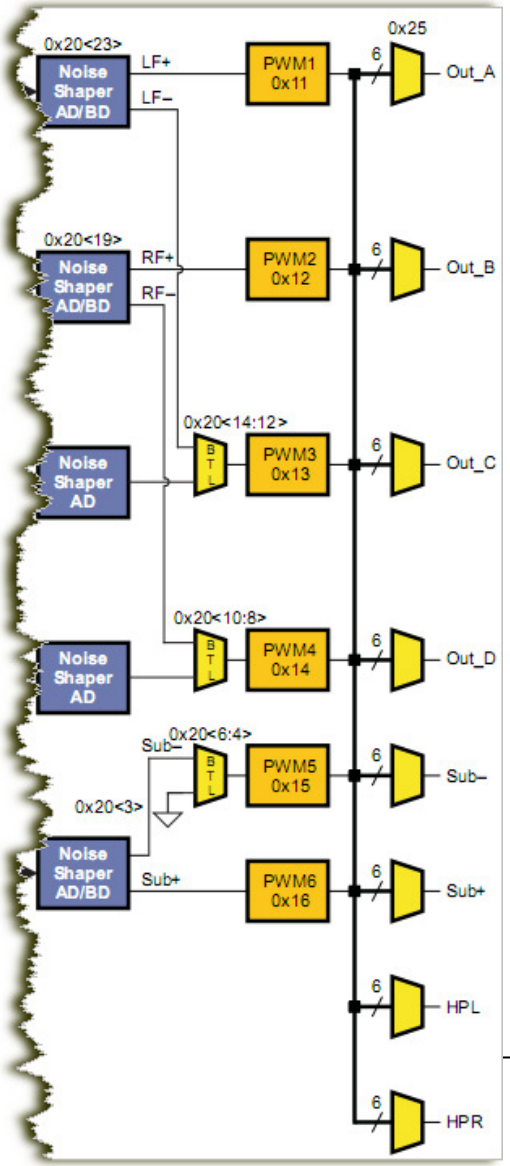
Register: 0x25

PWM OUTPUT MUX REGISTER

Critical Register Setting ---- 0x25

0x25, PWM OUTPUT MUX REGISTER

PWM Out Routing



Definition:

Internal Digital PWM: PWM 1 to PWM6

Half – Bridge Output: OUT_A to OUT_D

Logic PWM Output : Sub-, Sub+, HPL, HPR

PWM1 to PWM6 can be routed to any one of eight outputs.

Output A to D is Half-Bridge high power output, can drive speaker.

Sub-, Sub+, HPL, HPR are PWM signal outputs which used to drive external power stage or just for line out.

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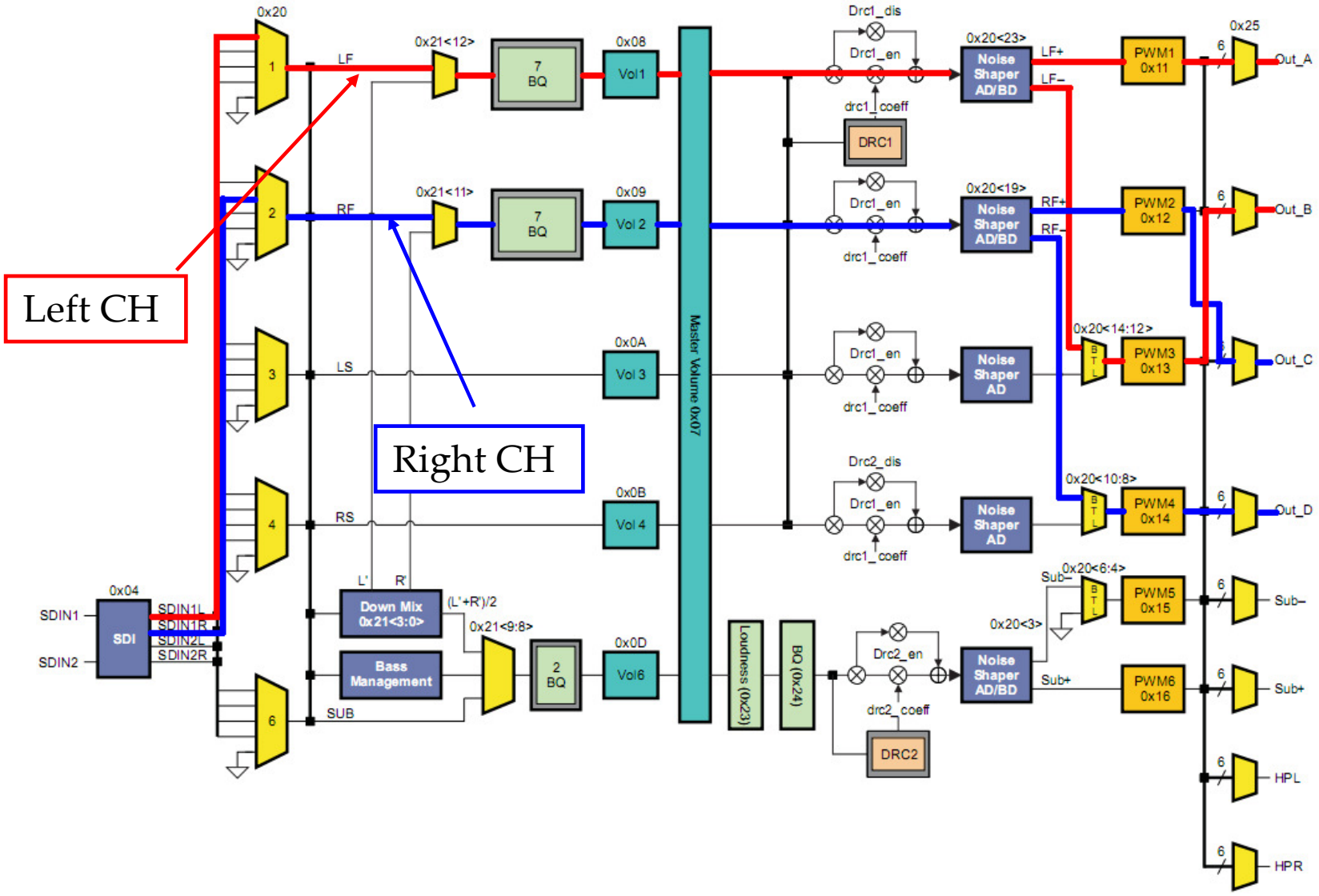
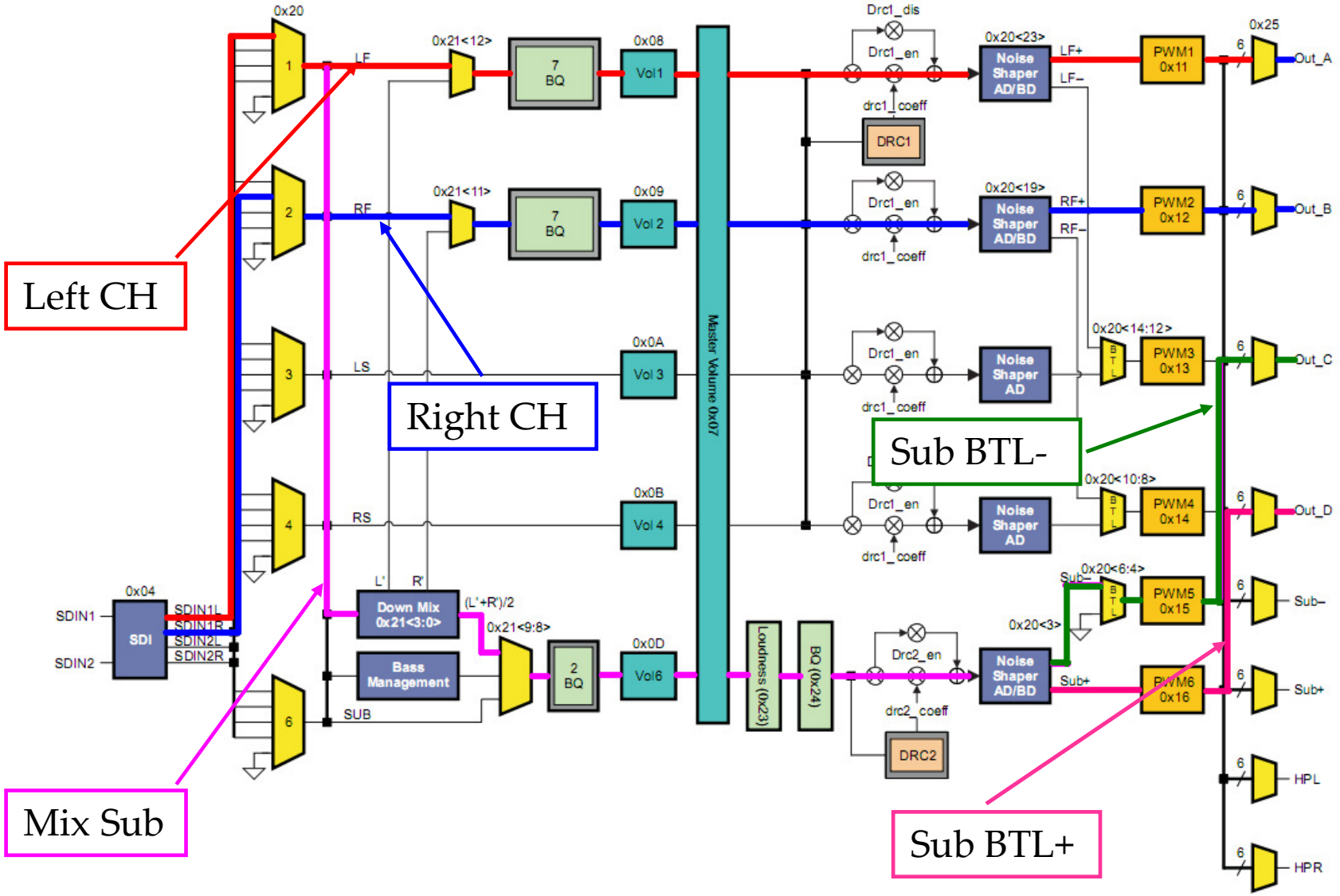
2.0 and 2.1 Output Default Configuration Signal Flow

Default 2.0 CH Signal Flow Chart



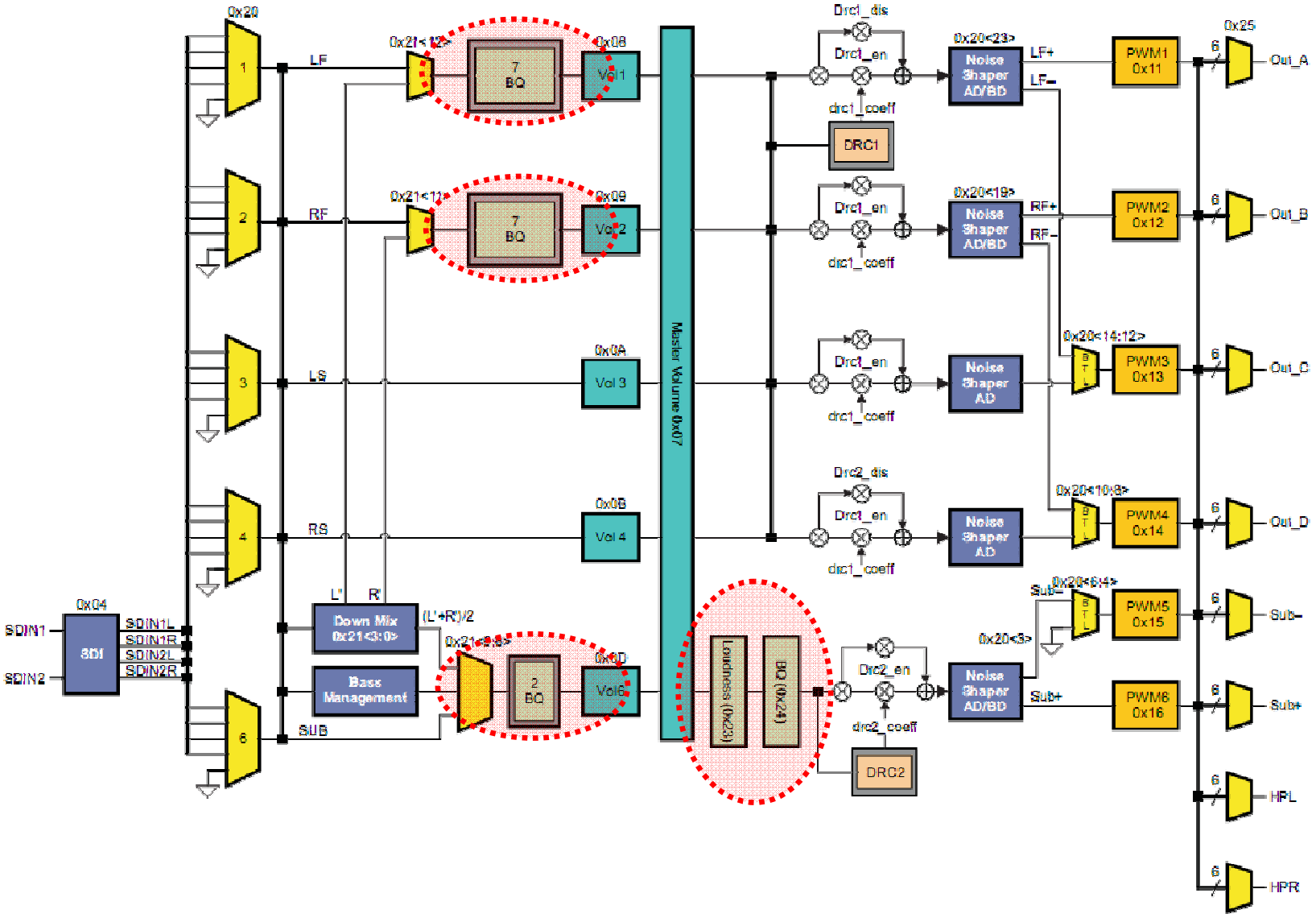
Default 2.1 CH Signal Flow Chart



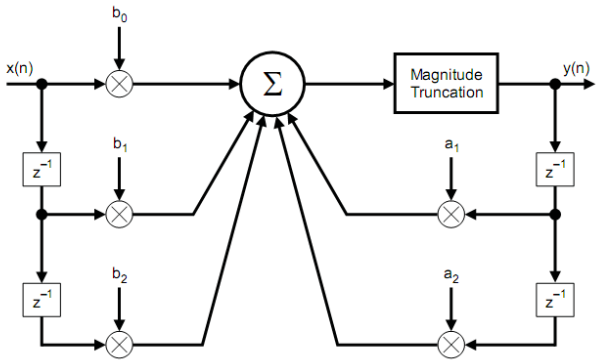
Digital Audio Processor Application

------- EQ

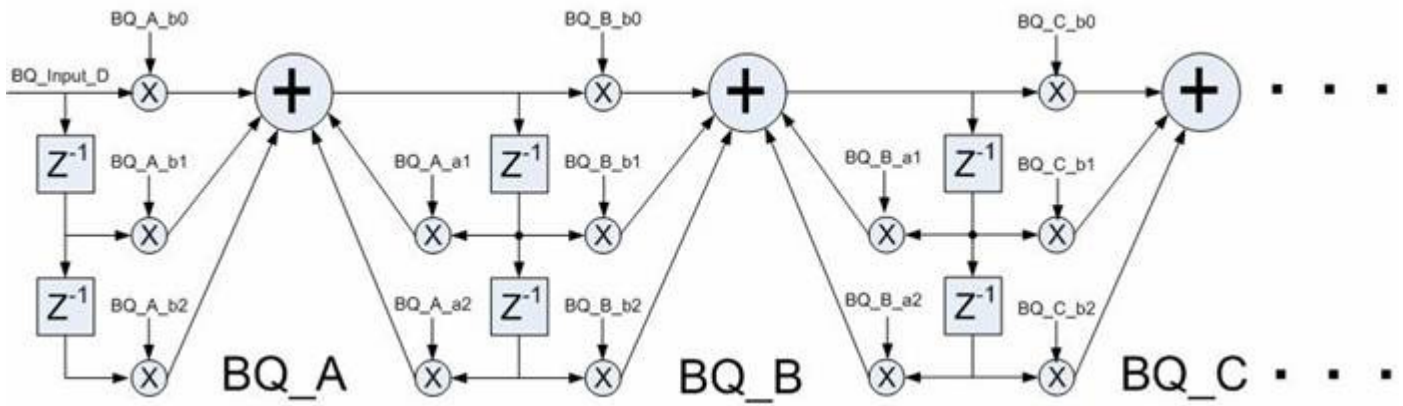
Signal Flow of TAS57xx --- EQ Channels



How EQ works?



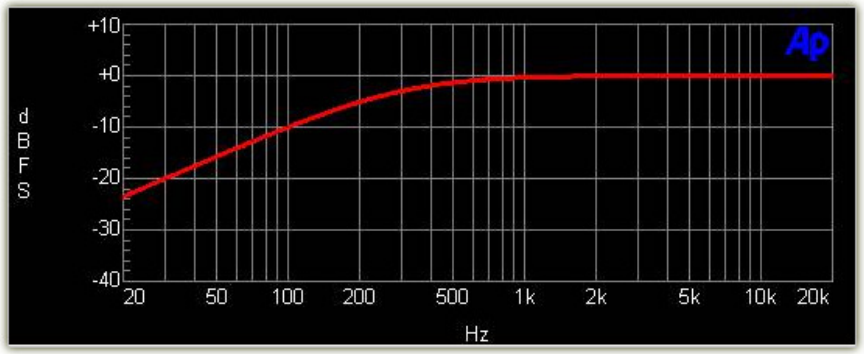
Single BQ filter provide Single filter, such as one HPF, LPF….



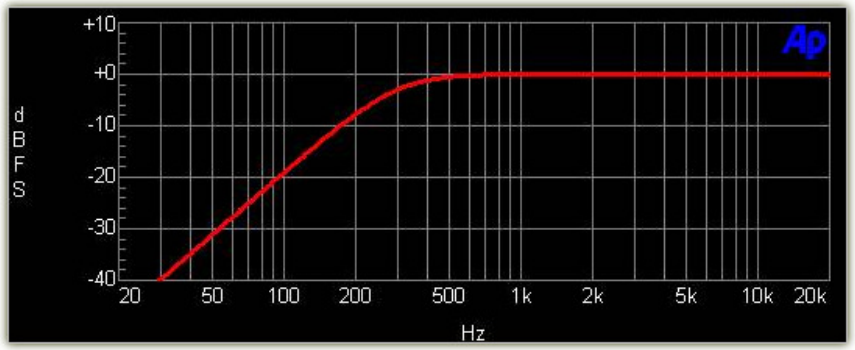
BQ filter can be linked in series to do several times filtering on input signal.

High Pass Filter Collection

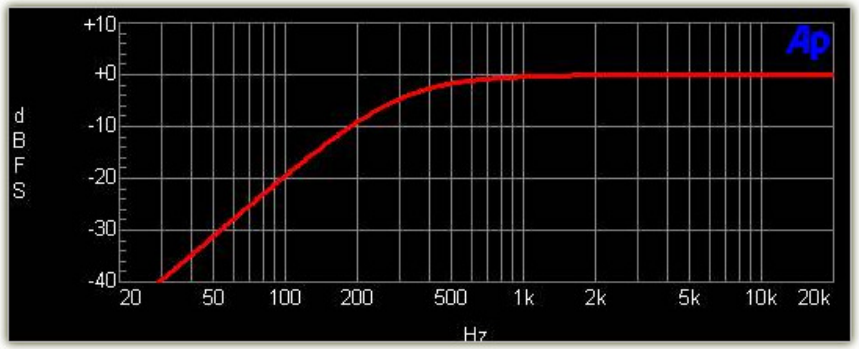
Type	SubType	FC(Hz)	Gain(dB)	BW(Hz)	Q(Hz)	PBR(dB)
High Pass	Butterworth 1	300				



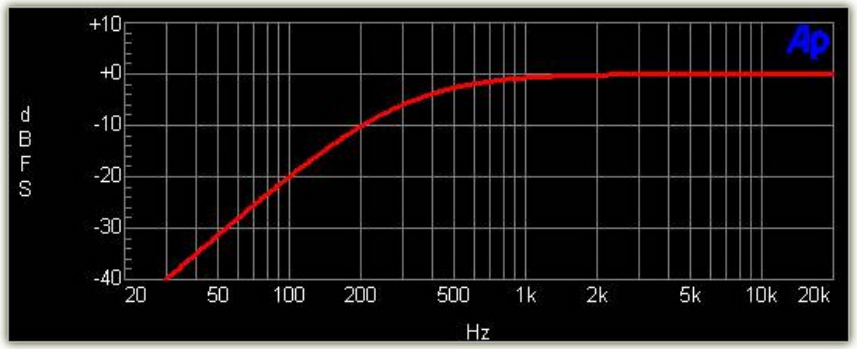
Butterworth HPF (1st order)



Butterworth HPF (2nd order)



Bessel HPF (2nd order)



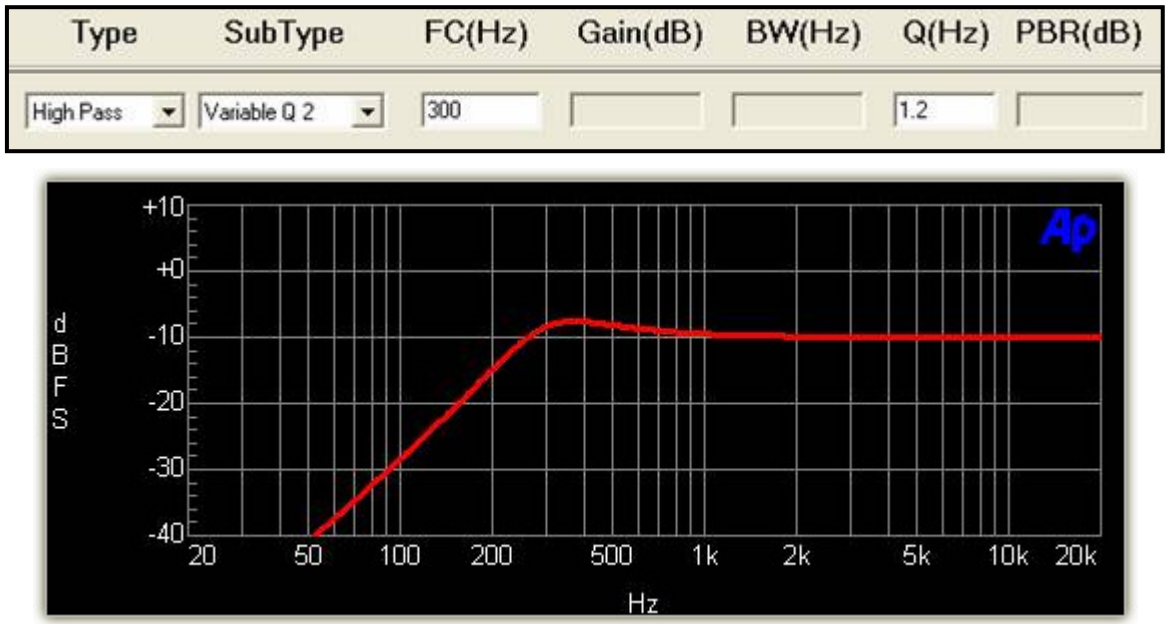
Linkwitz-Riley HPF (2nd order)

Variable Q High Pass Filter (2nd order)

The Variable Q High Pass Filter allows the user to specify the Filter Q which is defined as Fc / BW.

Properties

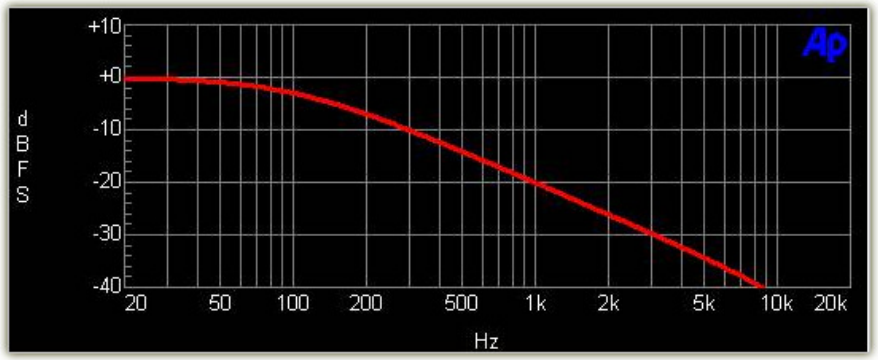
- Fc = -3dB Filter cutoff frequency in Hertz.
- Q = Peaking amplitude at Fc.



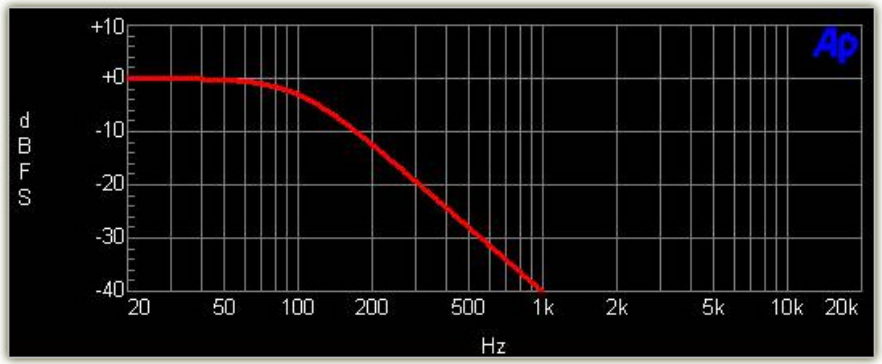
Variable Q High Pass Filter (2nd order)

Low Pass Filters Collection

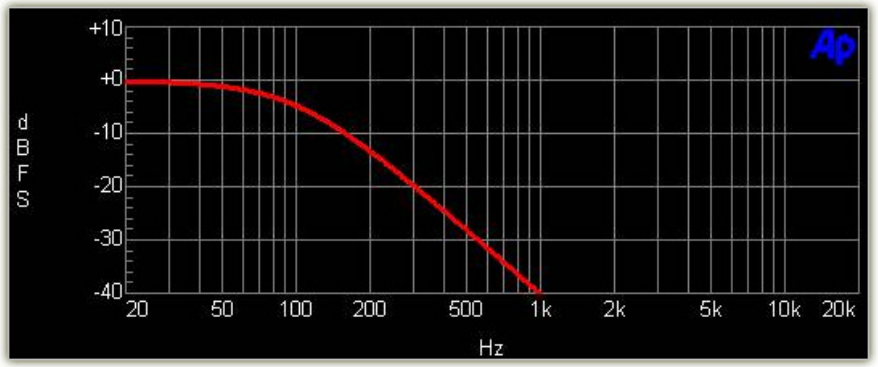
Type	SubType	FC(Hz)	Gain(dB)	BW(Hz)	Q(Hz)	PBR(dB)
Low Pass	Butterworth 1	100				



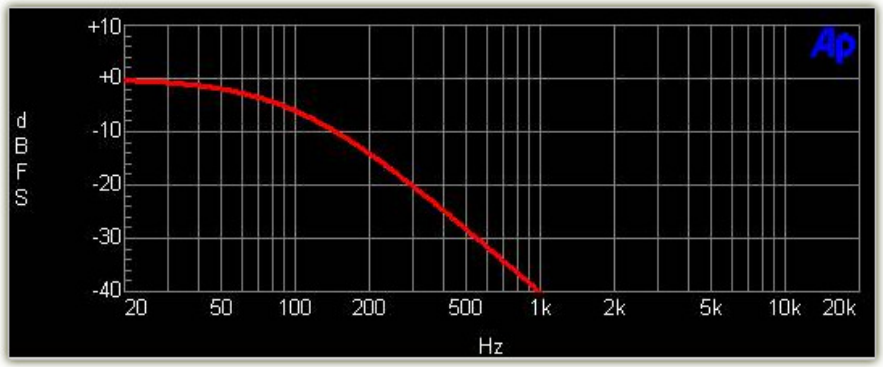
Butterworth LPF (1st order)



Butterworth LPF(2nd order)



Bessel LPF(2nd order)



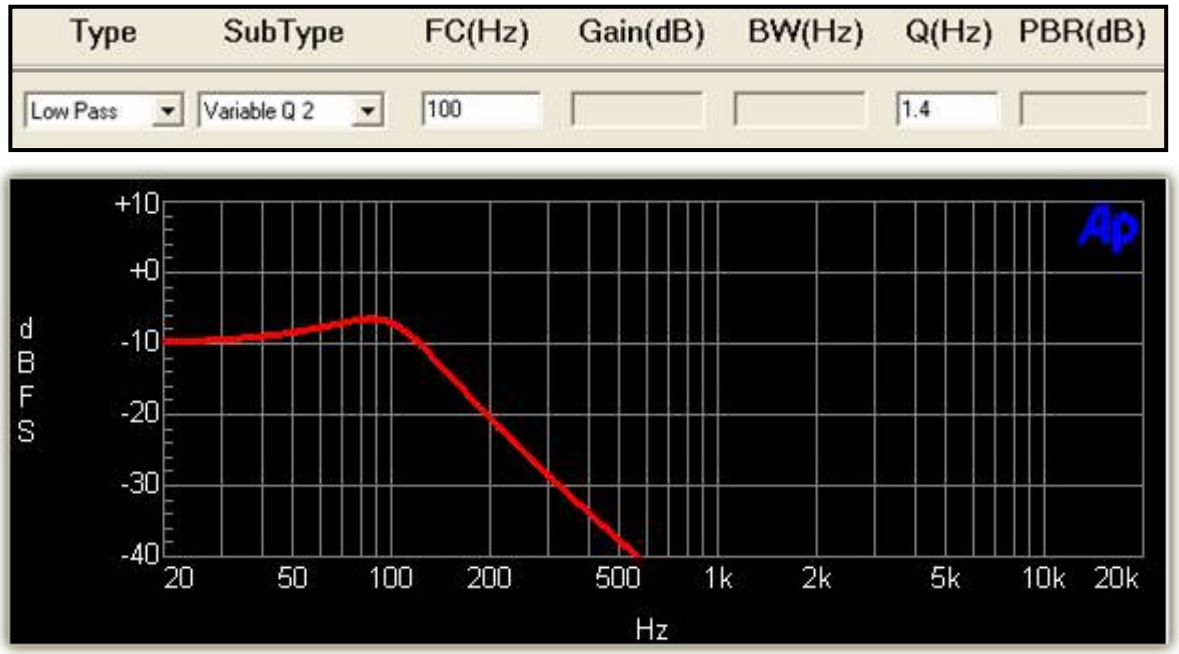
Linkwitz-Riley LPF(2nd order)

Variable Q Low Pass Filter (2nd order)

The Variable Q Low Pass Filter allows the user to specify the Filter Q, which is defined as Fc / BW.

Properties

- Fc = -3dB Filter cutoff frequency in Hertz.
- Q = Fc / BW

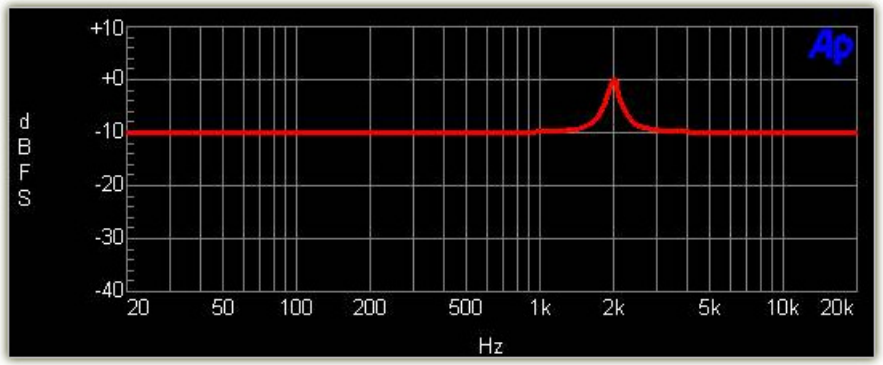


Variable Q Low Pass Filter (2nd order)

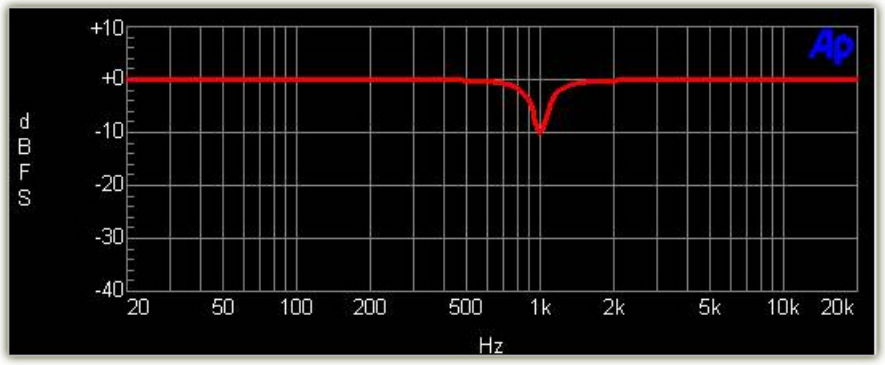
EQ Filters

One of the most common 2nd-order IIR filters is the bell-shaped parametric equalization (EQ) filter. This powerful filter is specified by Fc, Gain, and BW. Two examples are shown: one with a -10 dB cut and one with a +10 dB boost.

Properties
Fc = -3dB Filter cutoff frequency in Hertz.
Gain = Filter gain in dB
BW = Filter bandwidth



Type	SubType	FC(Hz)	Gain(dB)	BW(Hz)
EQ		2000	10	200



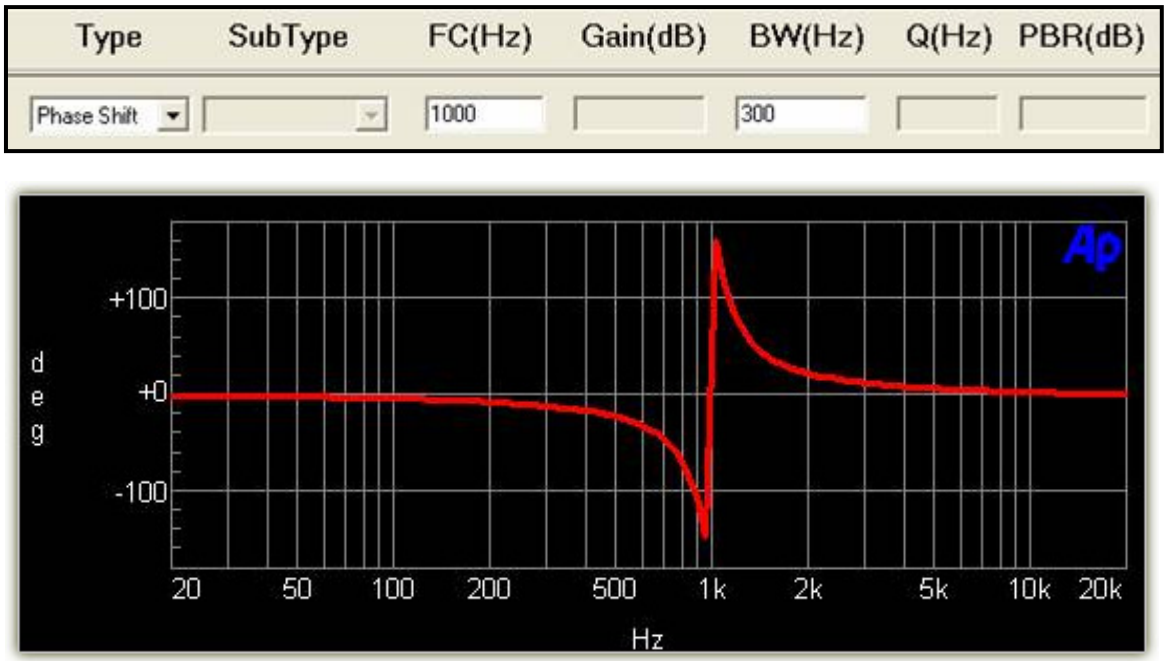
Type	SubType	FC(Hz)	Gain(dB)	BW(Hz)
EQ		1000	-10	100

Phase Shift

The Phase Shift Filter allows you to produce a phase shift in the audio, as can be seen in the example. Note that the gain plot for this filter is the same as an All Pass filter. That is, it produces a flat response throughout the audio band.

Properties

- Fc = Frequency of Maximum Phase deviation (Hertz).
- BW = Specifies the slope of the phase deviation



Note: This is Phase vs Frequency Curve

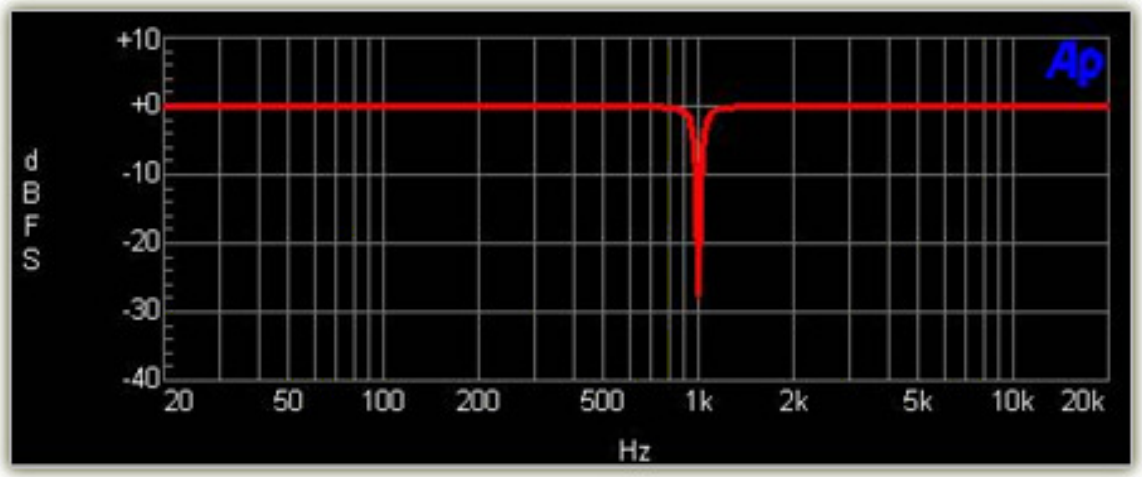
Notch Filter

The Notch Filter is also known as a band reject filter. This filter produces a deep cut at the center frequency (Fc).

Properties

- Fc = Notch center frequency in Hertz.
- BW = Bandwidth of notch

Type	SubType	FC(Hz)	Gain(dB)	BW(Hz)	Q(Hz)	PBR(dB)
Notch		1000		100		



Treble Shelf Filter

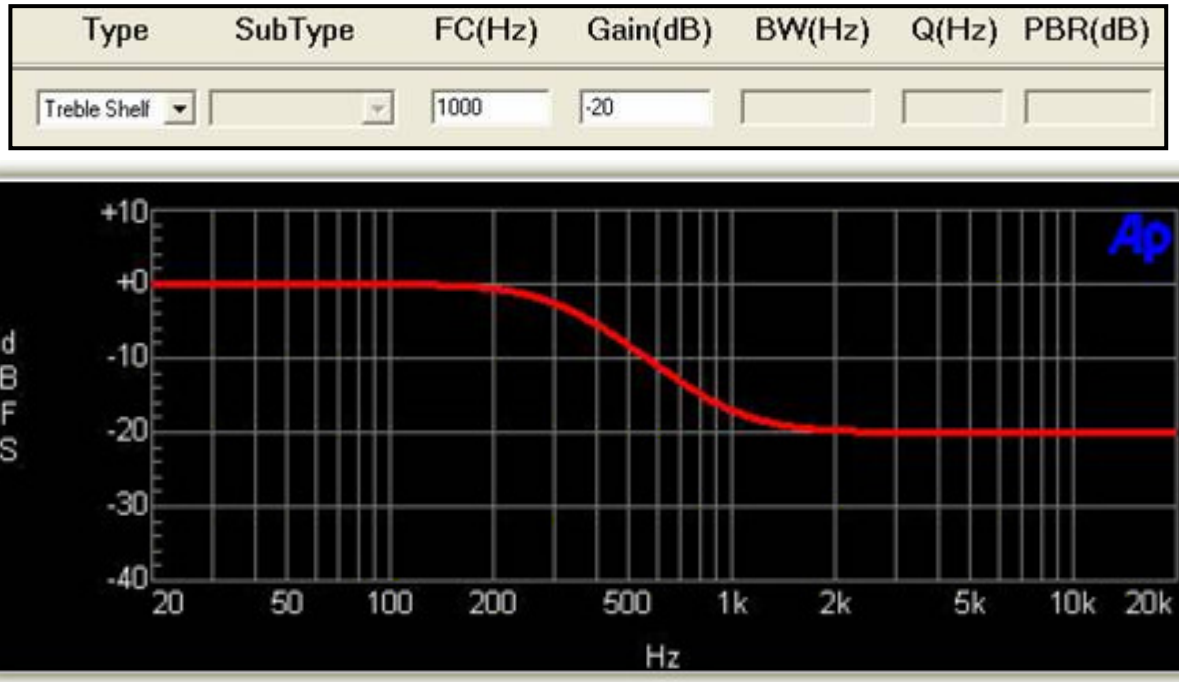
The Treble Shelf Filter is shown below. In this example, the treble is cut by -20 dB at -3 dB point from Fc = 1,000 Hz.

Properties

- Fc = Notch center frequency in Hertz.
- Gain (dB) = Filter Gain in DB

Note:

Treble and Bass Shelf filter also can do positive gain shelf, but it recommend to use negative gain shelf to prevent digital overflow.



Bass Shelf Filter

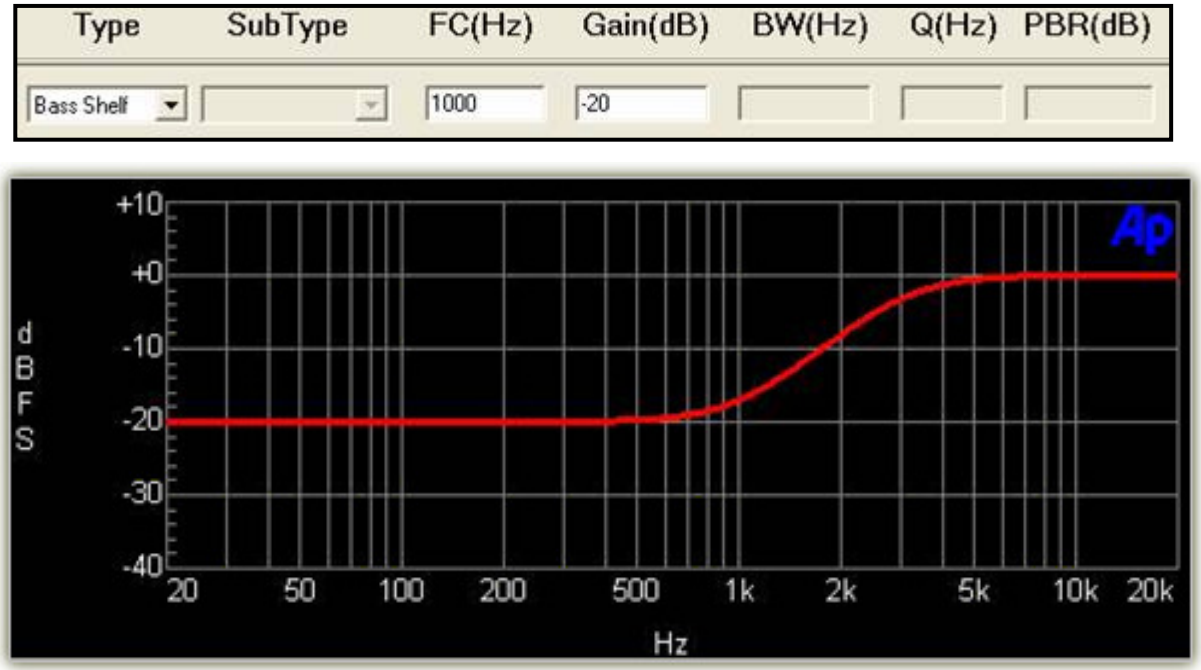
The Bass Shelf Filter is shown below. In this example, the bass is cut by -20 dB at -3 dB point from Fc = 1,000 Hz.

Properties

- Fc = Notch center frequency in Hertz.
- Gain (dB)

Note:

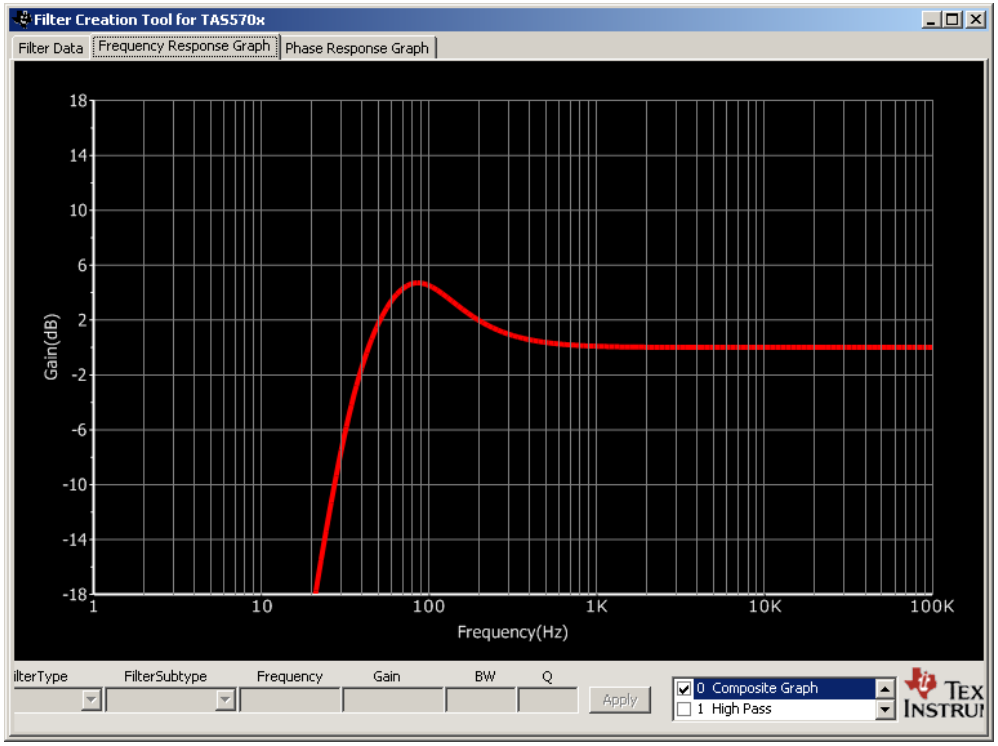
Treble and Bass Shelf filter also can do positive gain shelf, but it recommend to use negative gain shelf to prevent digital overflow.



EQ Design Example

Design Spec:

- 2.0 Channel Output, following EQ applied to both L/R channel
- Cut off audio signal below 35Hz by using two band Butterworth 2 filter
- Boost 5dB at 80Hz, band width is 100Hz



Curve in GDE

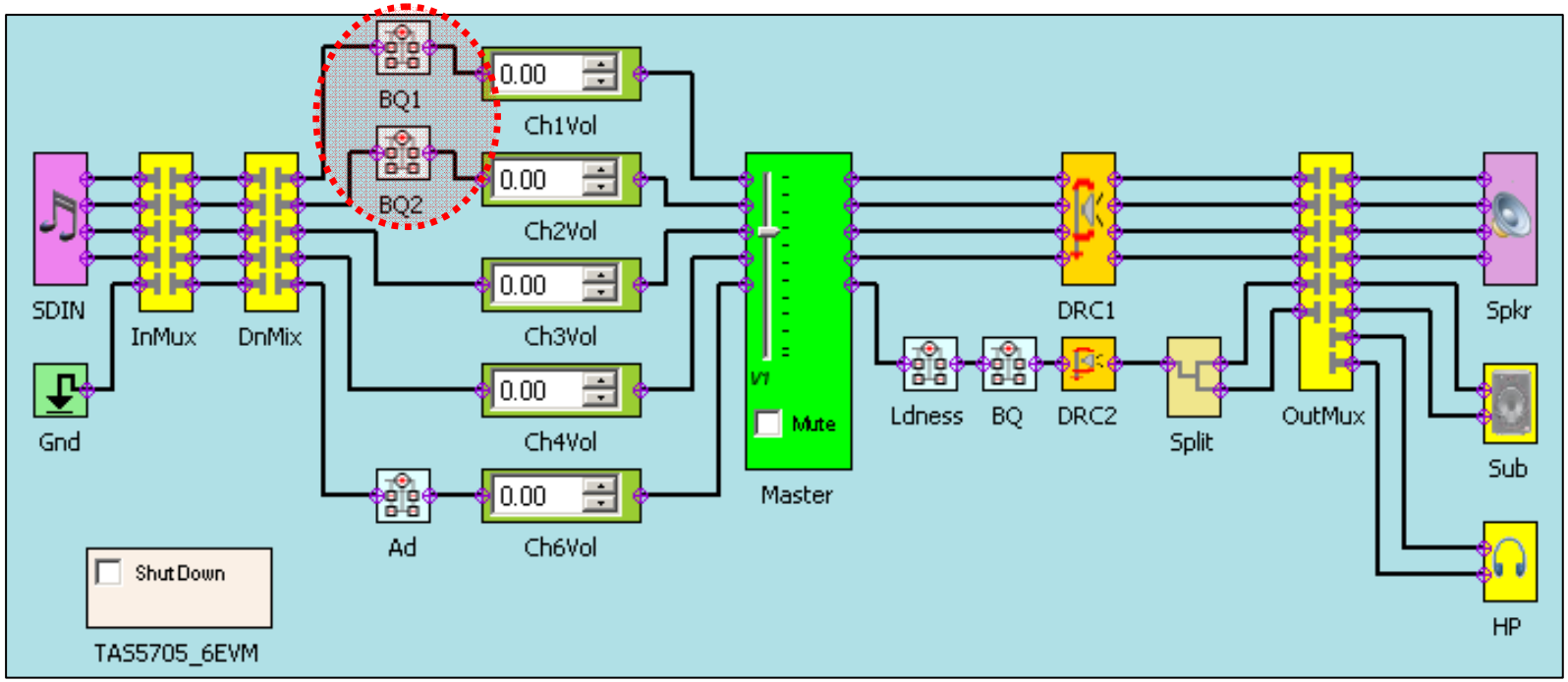
EQ Design Example

Step 1:

Generate EQ coefficient In GDE;

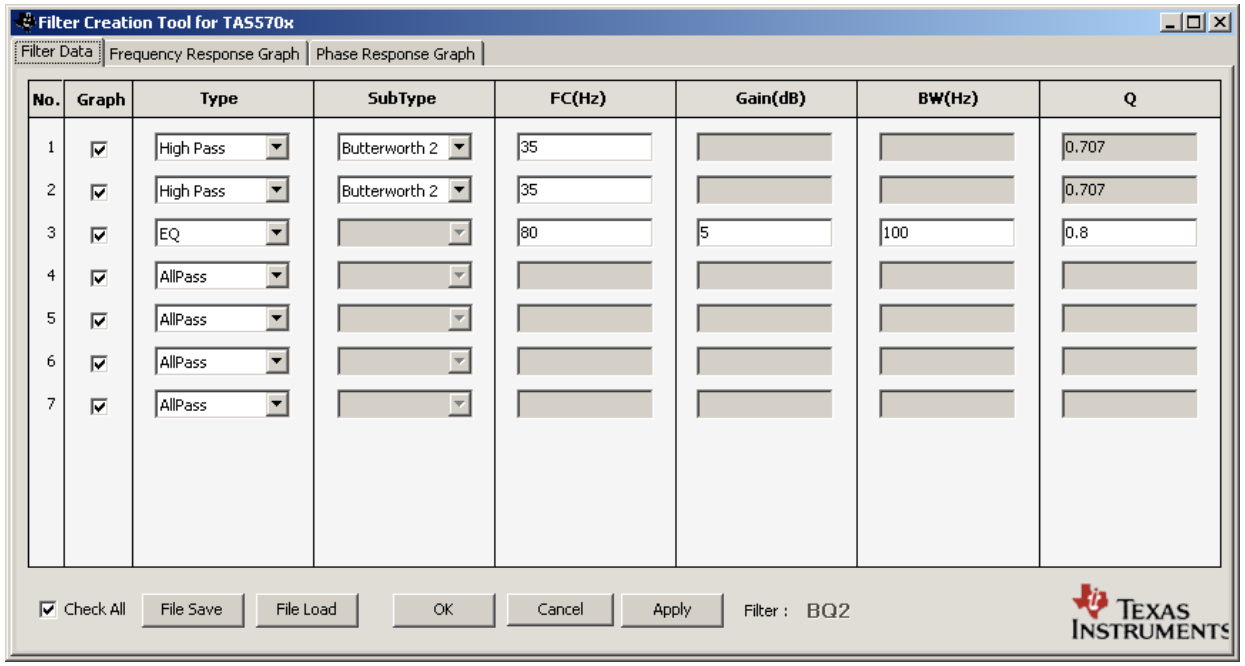
BQ1 is for Left channel, BQ2 is for Right channel.

Select BQ1 and BQ2 to modify EQ parameters.



EQ Design Example ---- Setting Guide

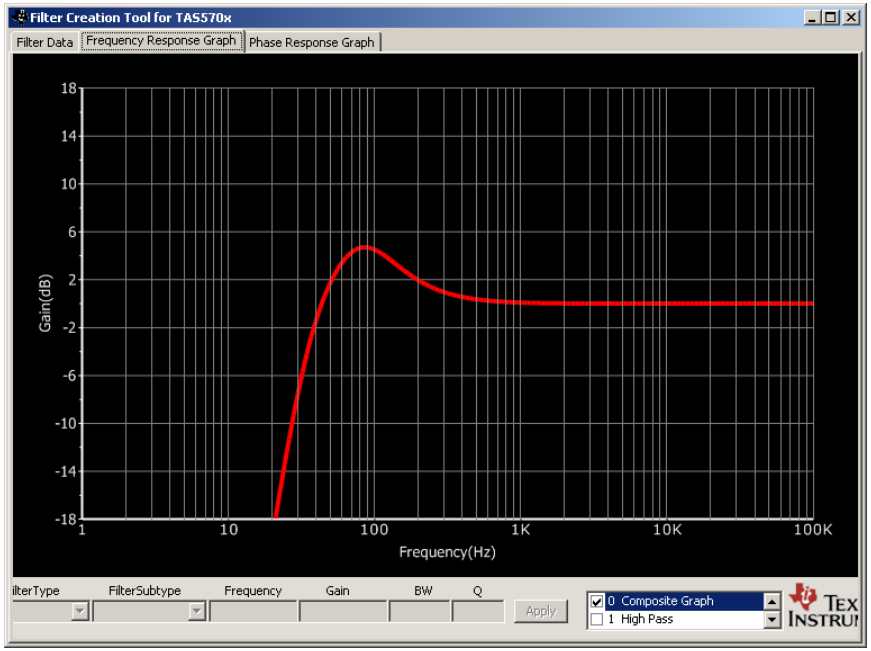
1. Add **Two High Pass filters** for bq1 and bq2, cut off frequency is set to 35Hz.
2. Add **EQ** filter for bq3, center frequency is 80Hz, Gain is 5dB, Band width is 100Hz.
3. Final table should looks like following picture:



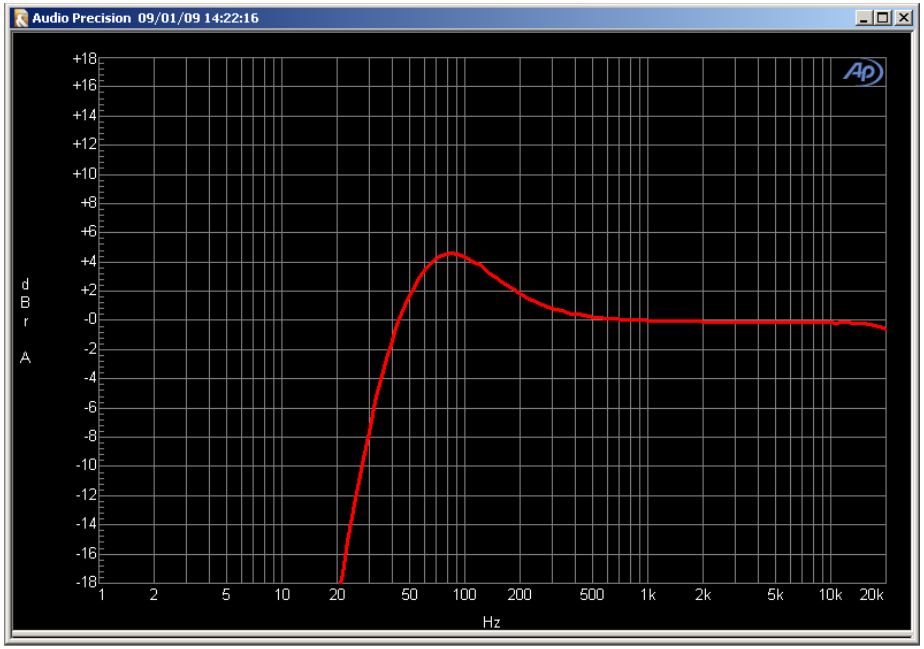
4. Click OK or Apply to send coefficient to devices for BQ1.
5. Do the same thing for BQ2, make sure Left and Right channels EQ are the same.

EQ Design Example ---- Test Results

Test Results are shown blow:



GDE Generated Curve



AP Test Curve

EQ Design Example ---- Register Map

Example EQ is programmed to device registers, here is register map for reference:

1.cfg - Notepad

File Edit Format View Help

```
! I2C Configuration file for TAS570x
X1B 00
X06 00
X19 30
X21 00  00  42  03
X20 00  89  77  7A
X11 B8
X12 60
X13 A0
X14 48
X15 F4
X16 0C
X04 05
X25 00  02  13  00
! Biquads
X50 00  00  00  00
X23 00  80  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00
X29 00  7F  96  00  0F  00  D4  00  00  7F  96  00  00  FF  2B  A8  0F  80  D3  A8
X2A 00  7F  96  00  0F  00  D4  00  00  7F  96  00  00  FF  2B  A8  0F  80  D3  A8
X2B 00  80  A5  D4  0F  01  AD  B9  00  7D  B0  04  00  FE  52  47  0F  81  AA  27
X2C 00  80  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00
X2D 00  80  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00
X2E 00  80  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00
X2F 00  80  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00
X30 00  7F  96  00  0F  00  D4  00  00  7F  96  00  00  FF  2B  A8  0F  80  D3  A8
X31 00  7F  96  00  0F  00  D4  00  00  7F  96  00  00  FF  2B  A8  0F  80  D3  A8
X32 00  80  A5  D4  0F  01  AD  B9  00  7D  B0  04  00  FE  52  47  0F  81  AA  27
X33 00  80  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00
X34 00  80  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00
X35 00  80  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00
X36 00  80  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00
X37 00  80  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00
X38 00  80  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00
X24 00  80  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00  00
! DRCs
X3A 00  7F  FF  03  00  00  00  FB
X3B 00  7F  FF  03  00  00  00  FB
X3C 00  7F  FF  03  00  00  00  FB
X40 FC  83  10  D4
```

CH1-bq1-HighPass
CH1-bq2-HighPass
CH1-bq3-EQ

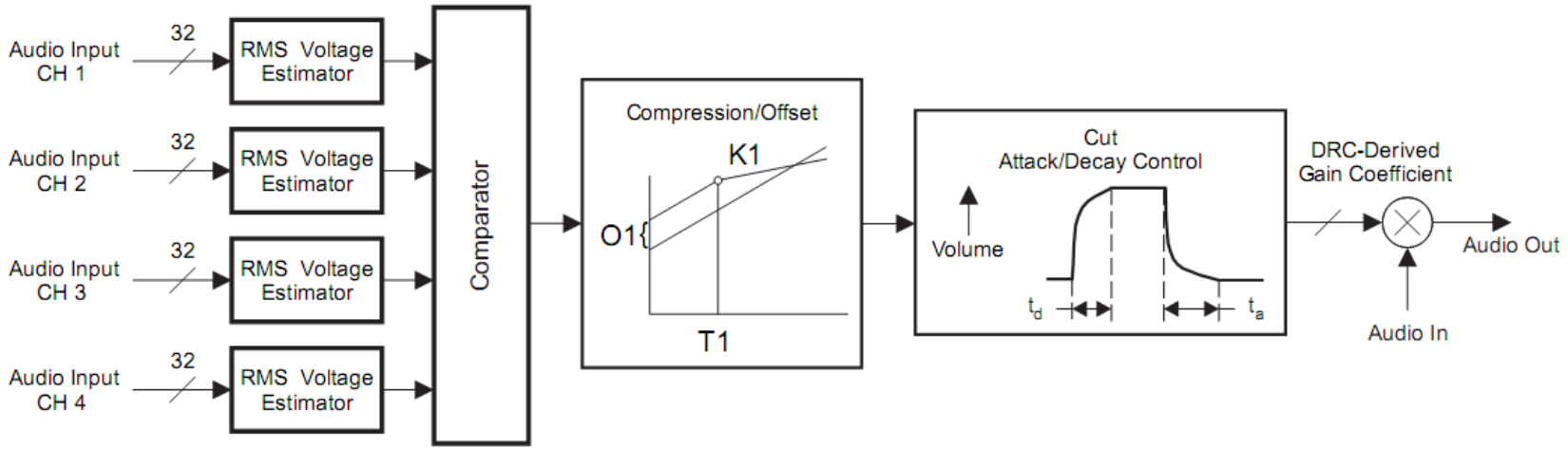
CH2-bq1-HighPass
CH2-bq2-HighPass
CH2-bq3-EQ

Digital Audio Processor Application

------- DRC

Fundamental of Dynamic Range Control

Dynamic Range Control (DRC) is an automatic signal amplitude control mechanism that can be used to contain or control the dynamic range of an audio signal to within specified limits.



DRC Signal Chart for TAS5706 (One – band DRC)

Fundamental of Dynamic Range Control

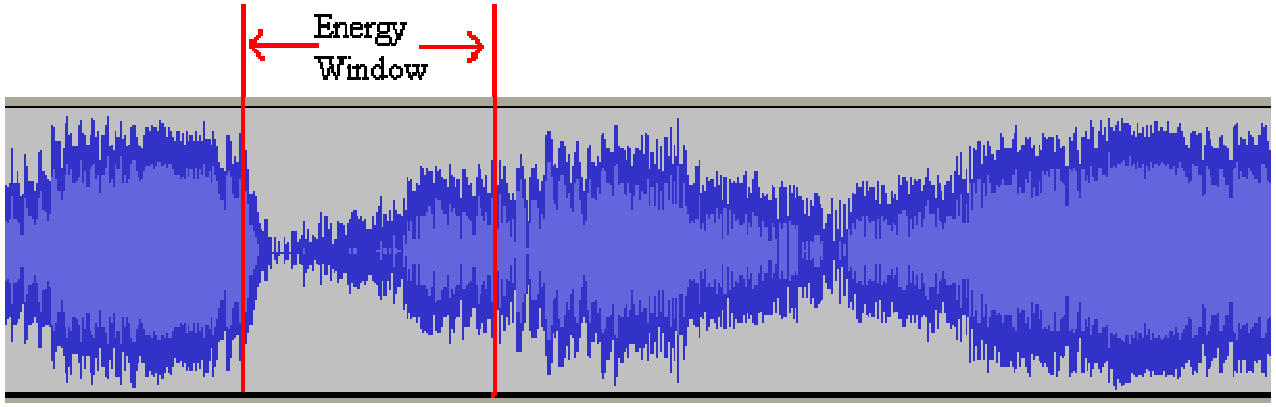
AAV estimator—This DRC element derives an estimate of the average absolute value (AAV) of the audio data stream into the DRC. A time constant, ***t_energy***, is used to control the effective time window over which the AAV estimate is made.

Compression coefficient computation—This DRC element converts the output of the AAV estimator to a logarithmic number, determines the region where the input resides, and then computes and outputs the appropriate gain coefficient to the attack/decay element. Parameters **K** define the slopes of the gain curve for these three regions. **T** specify the boundaries of the regions, in terms of input level. **O** specify offsets of the gain curve relative to a 1:1 transfer function at the thresholds.

Attack/decay control—This DRC element controls the transition time of changes in the coefficient computed in the compression/expansion coefficient computation element. User-specified parameters ***t_a*** and ***t_d*** are used to set the attack and decay time constants used in the gain adjustment.

DRC Timing Parameter --- Energy Time

Energy Time: DRC element derives an estimate of the average absolute value (AAV) of the audio data stream into the DRC. A time constant, t_energy, is used to control the effective time window over which the AAV estimate is made.

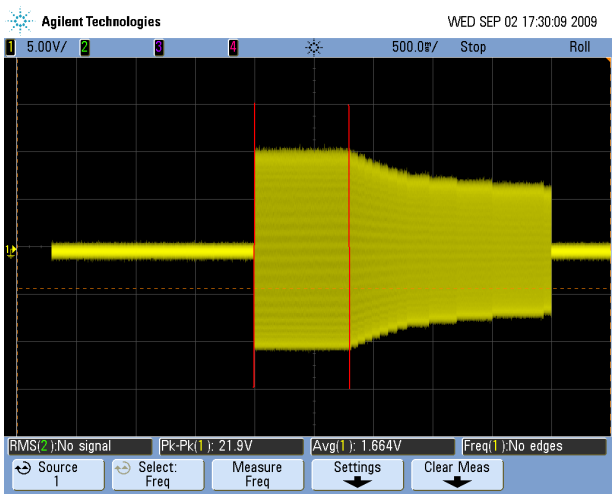


A reasonable minimum value for the energy time constant that would be used where **fast response is desired** is 10 times the period of the **lowest frequency** that is passed through the system.

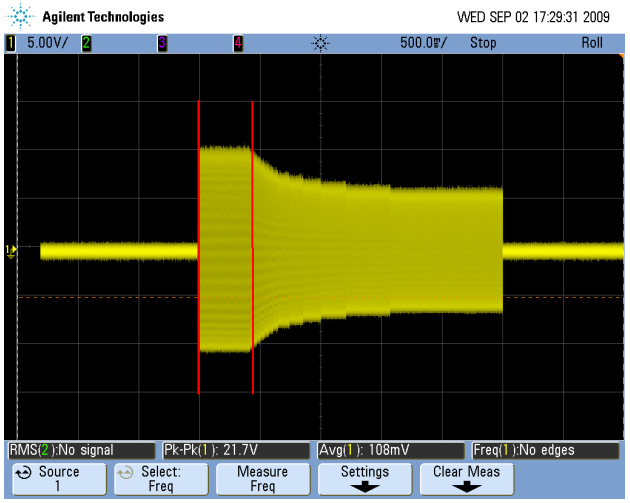
For example if the lowest frequency 40 Hz, the period of this is 25 ms.
The minimum energy time constant should be (10 * 25 ms = 250 ms).
Less than this time constant will produce a DRC control signal with significant ripple in it. We want to avoid ripple in the control signal because it produces modulation distortion in the output.

1. Larger Energy time will result slow action of DRC.
2. Smaller Energy time will make DRC act too often.

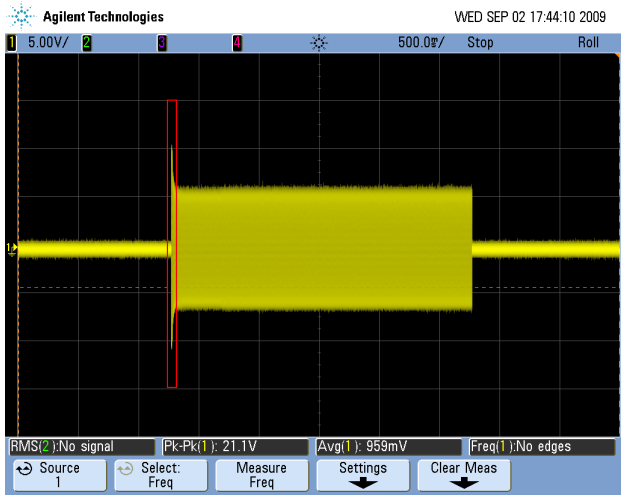
Energy Time Timing Example



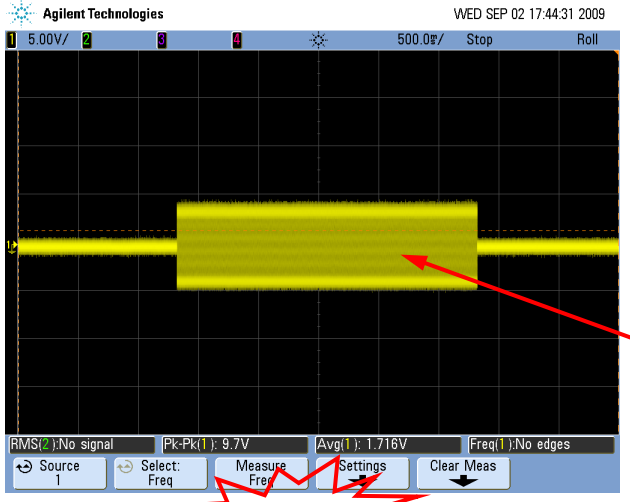
1000ms



500ms



10ms



0.01ms

Different Energy Time are tested, input is 1kHz Bust Sine Wave.

The minimum energy time should be 10ms for 1kHz single tone signal.

Too small Energy Time will bring DRC into unstable.

Amplitude Drop

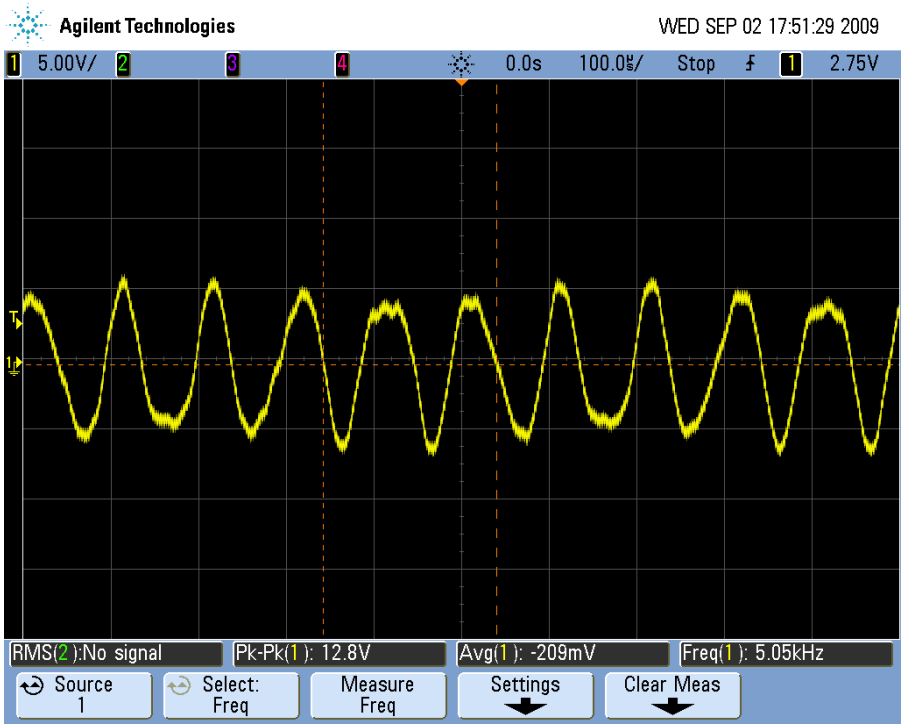
Unstable DRC

Error Energy Timing

Minimum value for the energy time constant is:

10 times the period of the **lowest frequency**

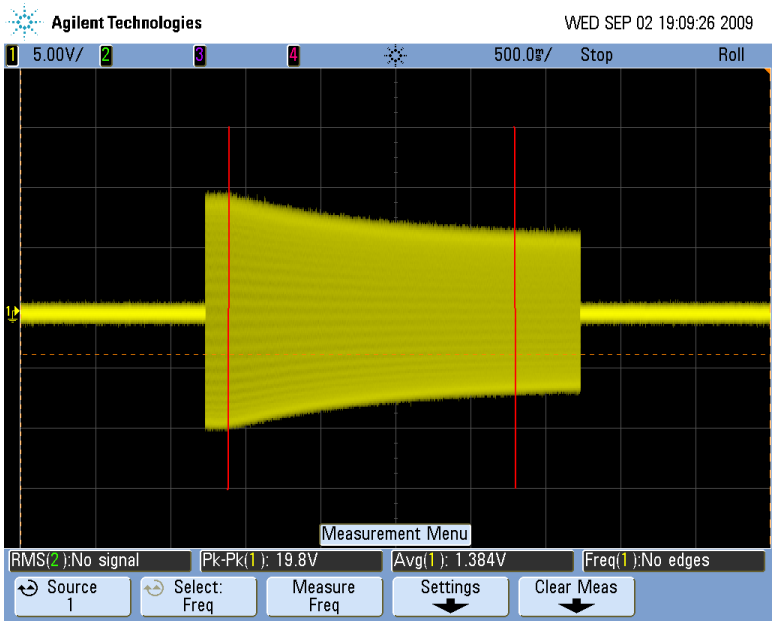
Otherwise, signal will have distortion after applied DRC.



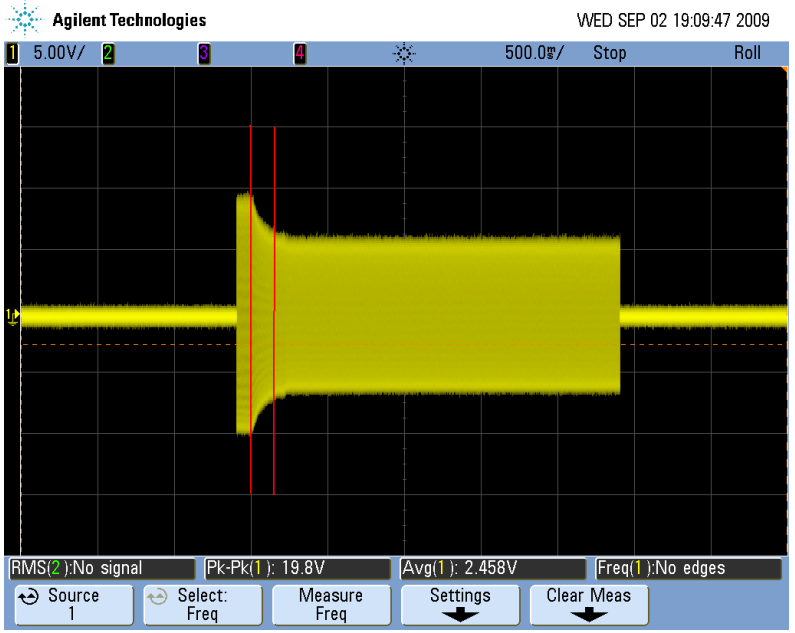
Distortion Wave after DRC

Input Sine 10kHz, Energy time 0.1ms.

Attack Time Example



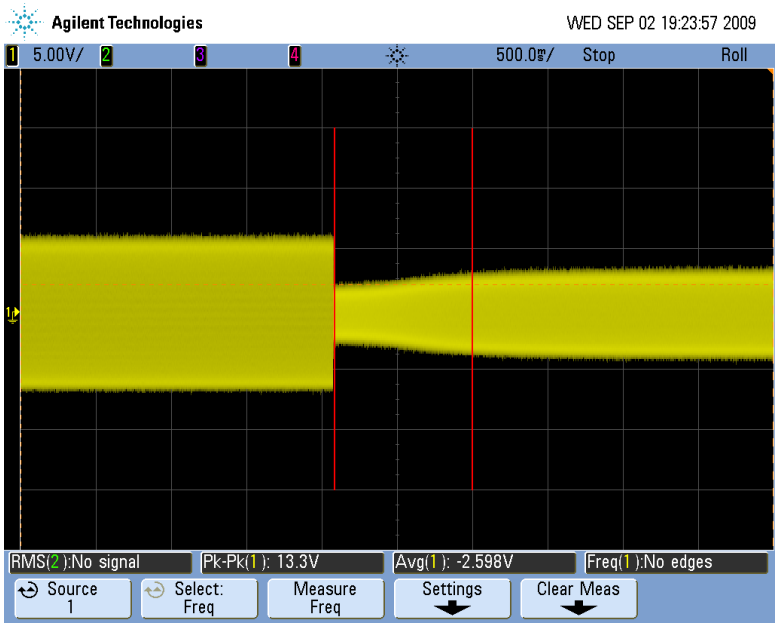
Attack time is 1000ms



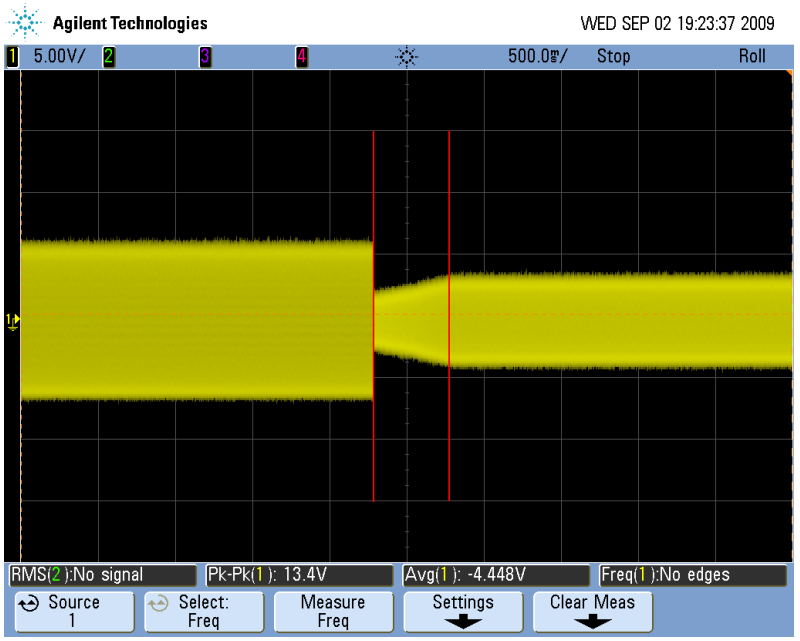
Attack time is 10ms

- Attack is defined as the application time of compression
- Typically set the minimum Attack time constant to between 3 and 5 times the period of the lowest frequency signal
- Longer attack time make sound volume change slowly
- Shorter attack time increase fast response when sound level changes
- Too short attack time will reduce Bass (Low frequency) content performance

Decay Time Example



Decay time is 500ms

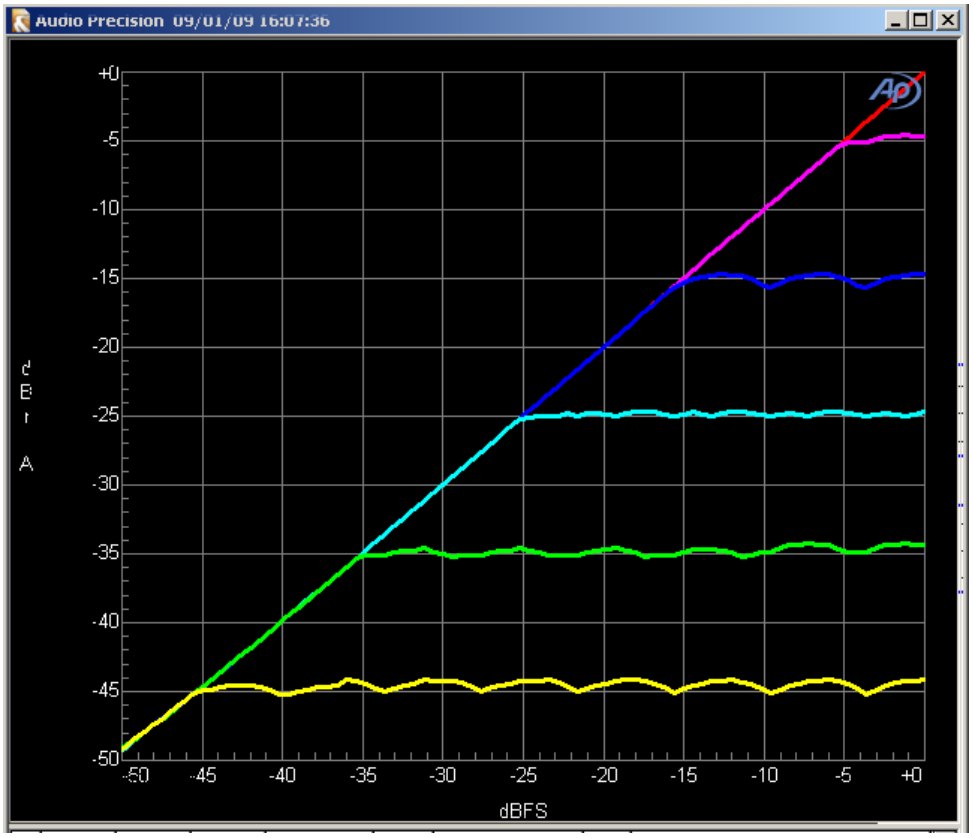


Decay time is 10ms

- Decay is defined as the release time of compression.
- Typically set the minimum Decay time constant to between 10 and 20 times the period of the lowest signal.
- Longer Decay time make sound volume change slowly.
- Shorter Decay time increase response speed when input sound level changes.

Use DRC as Power Limiter

DRC functions are mostly used as Power Limiter, in this kind of application, compression rate is set to more than 30 to reduce Gain to almost zero when input exceeds threshold.



Output vs Input
Vol = -10, input = 0db, 20/30/40/50db threshold

Time Constant Time Example

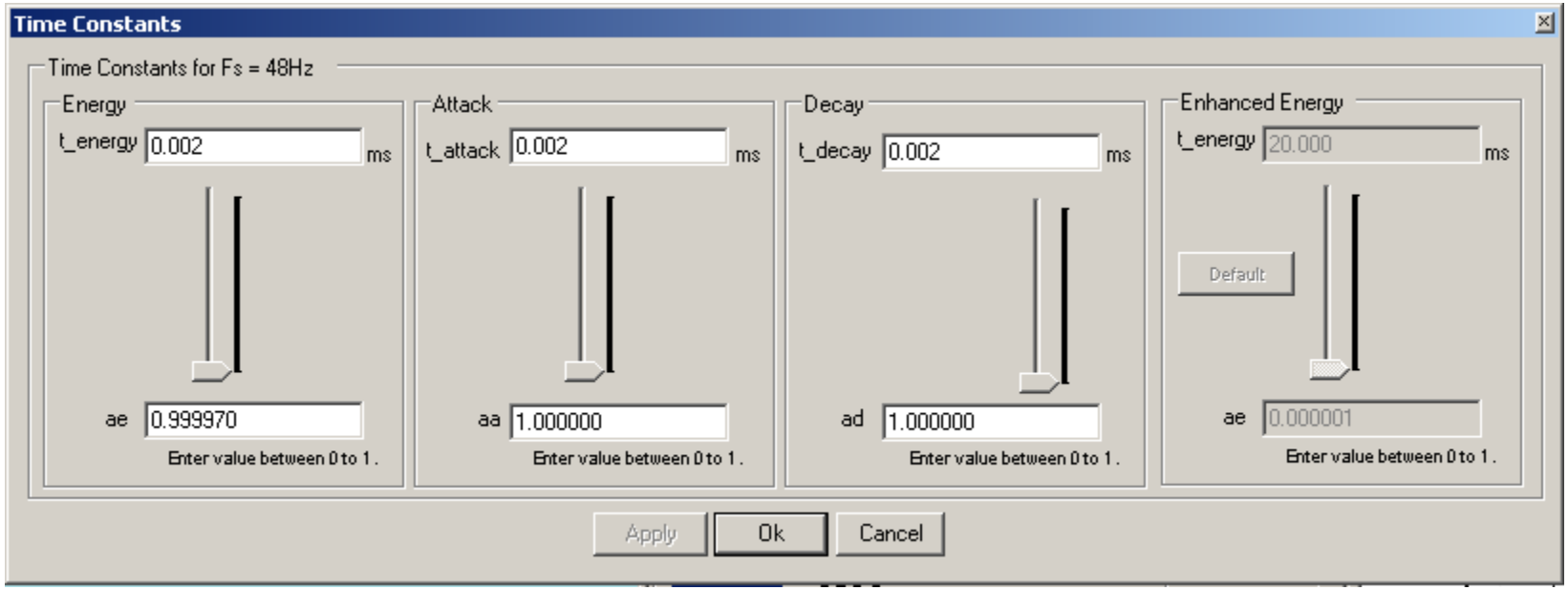
If the Lowest Frequency is Fs, the period is Ts. Suitable timing for DRC act as Power Limiter are list as blow:

Items	x Ts	Timing For 40Hz
Energy time	10x ~ 20x	250ms ~ 500ms
Attack time	3x ~ 5x	75ms ~ 125ms
Decay time	10x ~ 100x	250ms ~ 2500ms

Note : Customer may need to optimize above timing according to subjective listening test. Different music type, such as POP, Classic etc.. require different timing.

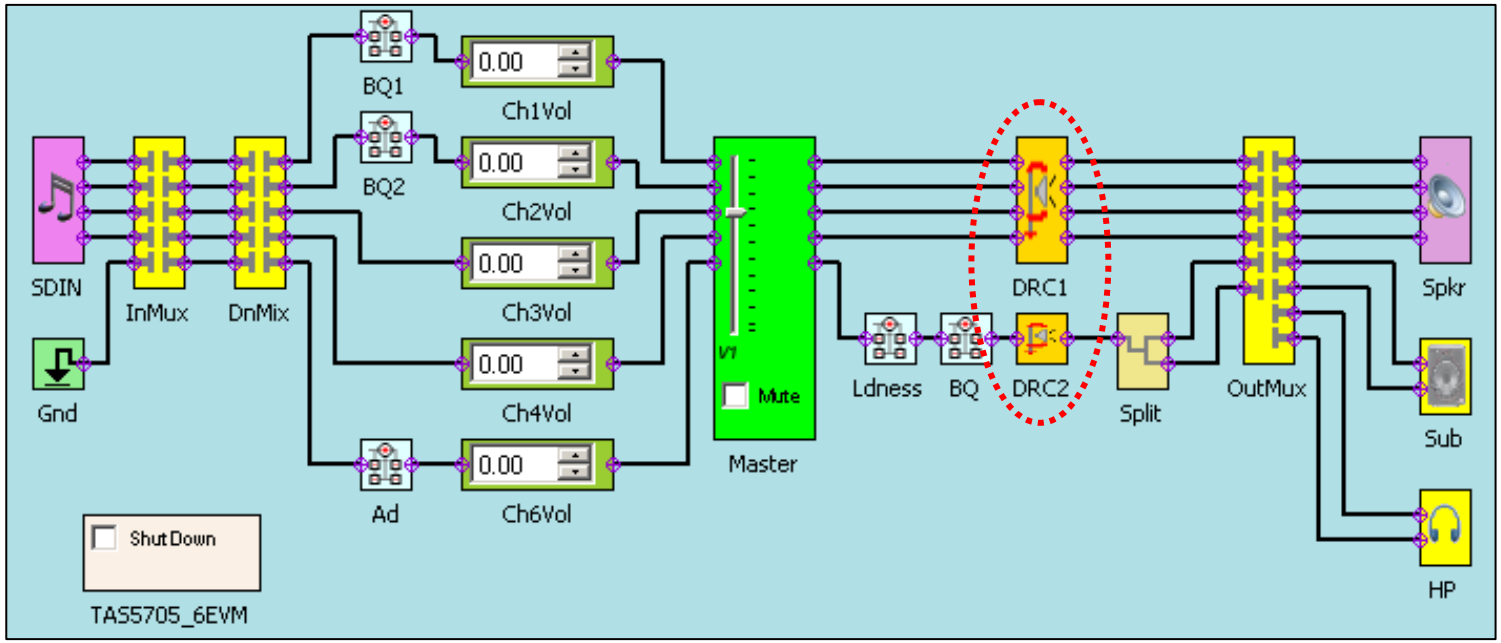
DRC Panel of TAS57XX GDE

GDE provide a panel for user to program special timing for DRC



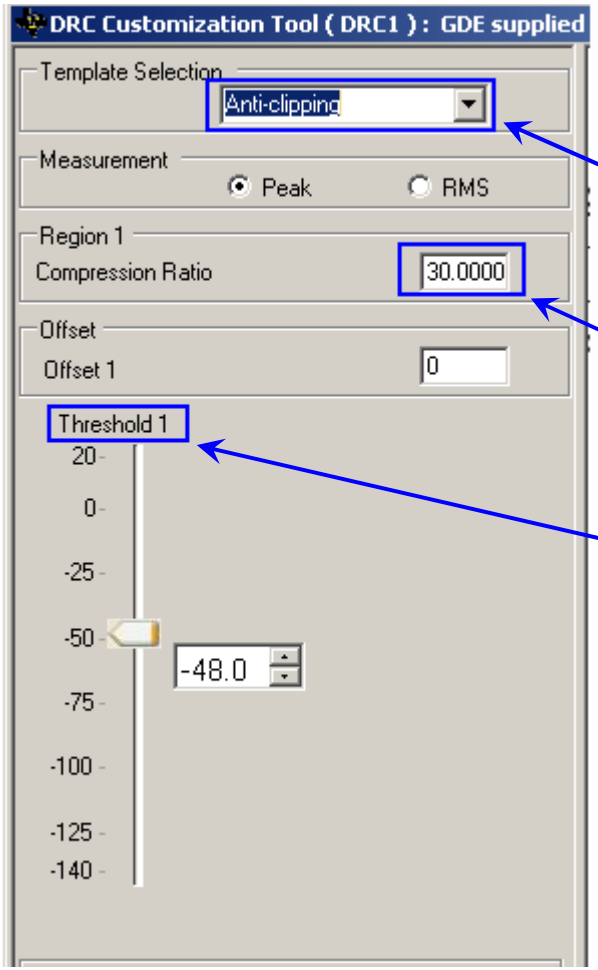
DRC Setting Example

Step 1. Generate coefficient in DRC panel:



- DRC1 is for CH1 CH2 CH3 CH4 ----------in charge of Left and Right channels DRC function
- DRC2 is for CH5 CH6 -------used only in 2.1 channels output. In charge of woofer DRC function

DRC Setting Panel

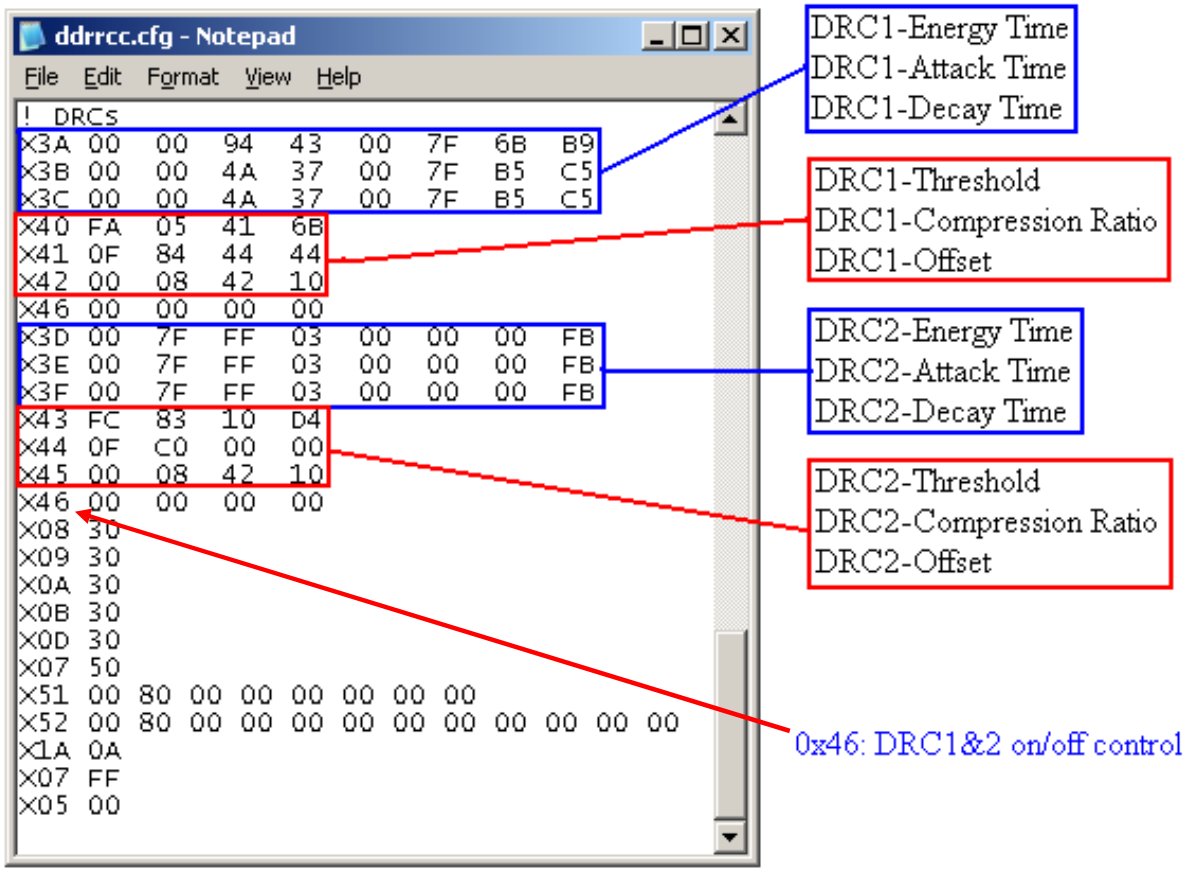


Note: This setting example is suitable for Power Limiter function, named Anti-Clipping in DRC Panel.

1. Select "Anti-clipping" Template, this helps to set correct time constants for "Attach time" "Decay time" "Energy time" automatically.
2. Compression Ratio has been set to 30 automatically. That's enough for Power limiting.
3. The only thing customer need to adjust is "Threshold" value. It depends on how much power after limitaion they want.

Note: Please select suitable value for "Threshold" according to experiment results. That's a "Try and Error" method.

DRC Register Map



1. Program DRC1 and DRC2 parameters at initiation.
2. 0x46 can be used to control DRC on/off
3. DRC adjustment is a “try and error” process, please try different Threshold value (0x40 and 0x43) to find what you want.

Digital Audio Processor Application

------- Auto Bank for EQ and DRC

EQ Auto Bank Switching

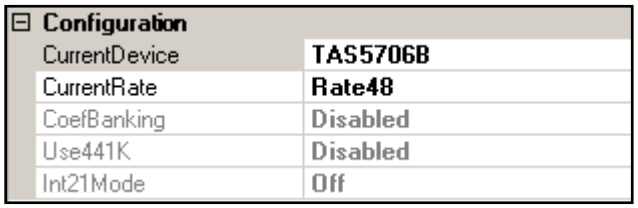
Bank switching allows the TAS57xx to detect automatically a change in the input sample rate and switch to the appropriate bank without any MCU intervention.

- TAS57xx has three banks to handle differential sampling frequency.
- For device ID is 0x28/0x2A parts: TAS5705/6/16:
  - Bank1 is for 32kHz
  - Bank2 is for 44.1/48kHz
  - Bank3 is for 96Hz and above
- For device ID is 0x68/0x70 parts: TAS5707/8/9/10/11:
  - More flexible setting provided to handle different sample-rate.
  - 0x50 can set which bank is for which sampling rate
  - EQ can be turn on/off by one bit change

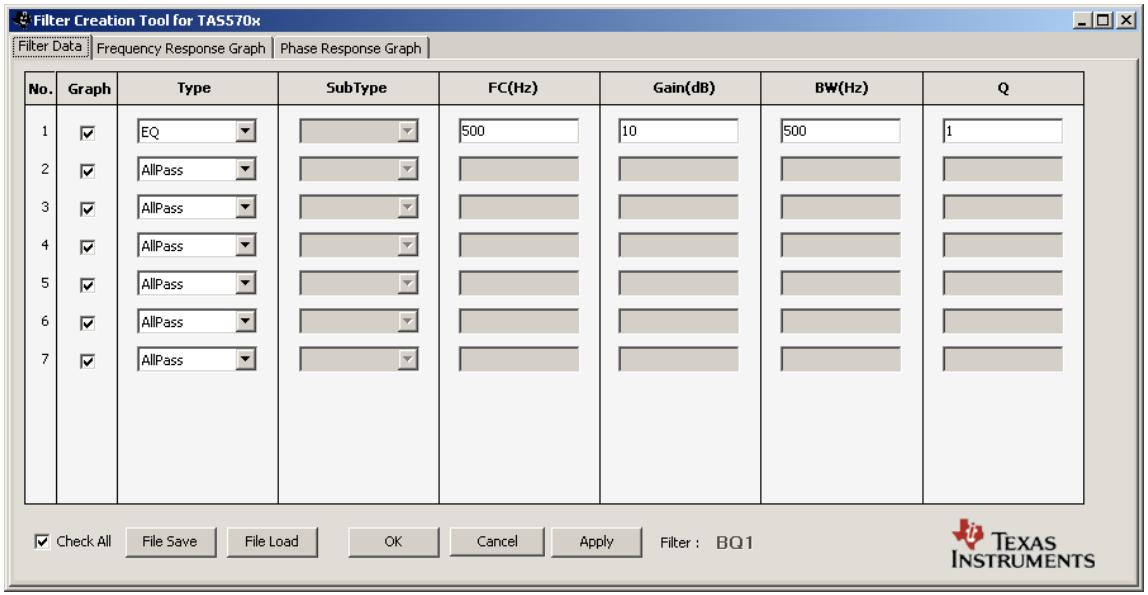
Why we need EQ Auto Bank Switching?

Example **Without Auto bank:**

1. Adding one EQ at 500Hz, 10dB boost, width is 200Hz.
2. Calculate 48kHz coefficient.

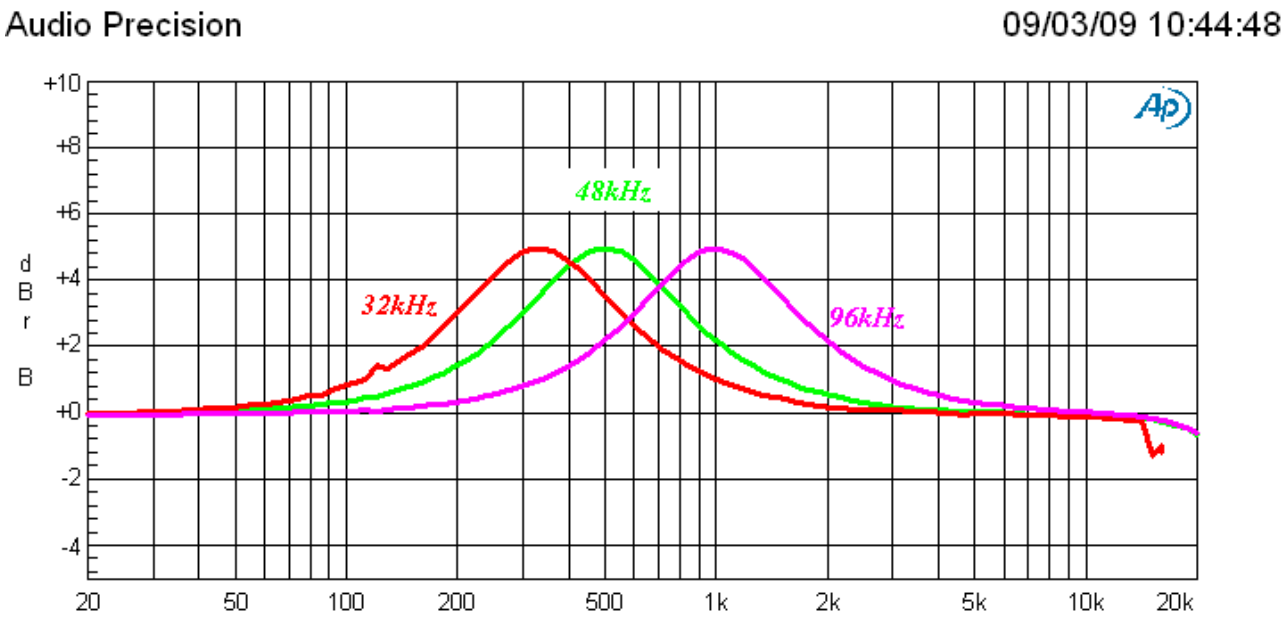


Set GDE Sample-Rate to Rate48



Set EQ

EQ Curve Without Auto Bank Switching



Frequency Response Curve **without Auto Bank Switching**

Without Bank switching, when input sampling frequency change to 32kHz or 96kHz, EQ curve shift.

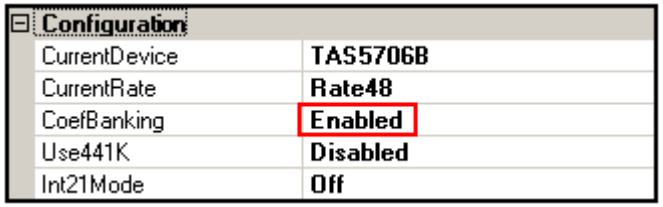
So we need Auto-Bank Switching to make sure correct EQ curve under different sample rate.

Enable Auto Bank Switching

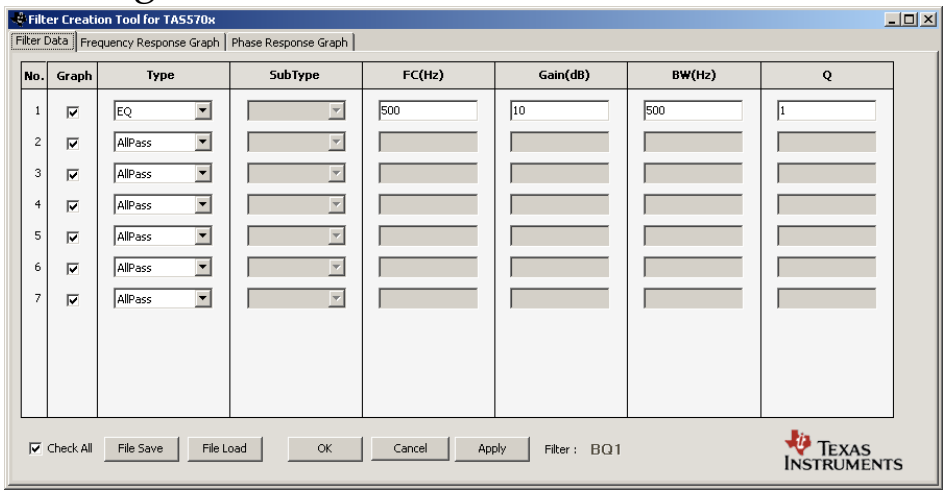
Follow these steps to turn on Auto Bank Switching Function

Step1: Calculate all coefficient under different sampling frequency.

Enable **Coefbank** in GDE, this enabled GDE to store all coefficients for different sample frequency in Configure File.



Step: Go to EQ Panel, regenerate EQ coefficient.



Regenerate EQ in EQ panel

EQ Register Map with Auto Bank Switching

Configure file with Auto Bank On

CoeffBank.cfg - Notepad

File Edit Format View Help

```
! Biquads
X50 00 00 00 01
X23 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X29 00 84 AA 32 0F 0D 29 9D 00 6F 58 FC 00 F2 D6 63 0F 8B FC D1
X2A 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X2B 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X2C 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X2D 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X2E 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X2F 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X30 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X31 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X32 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X33 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X34 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X35 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X36 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X37 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X38 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X24 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X50 00 00 00 02
X23 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X29 00 83 28 67 0F 08 A5 4A 00 74 BA 2C 00 F7 5A B6 0F 88 1D 6C
X2A 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X2B 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X2C 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X2D 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X2E 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X2F 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X30 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X31 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X32 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X33 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X34 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X35 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X36 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X37 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X38 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X24 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X50 00 00 00 03
X23 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X29 00 81 9A 9A 0F 04 41 AF 00 7A 46 3C 00 FB BE 51 0F 84 1F 29
X2A 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X2B 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X2C 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X2D 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X2E 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X2F 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X30 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X31 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X32 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X33 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X34 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X35 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X36 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X37 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X38 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
X24 00 80 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
```

Coeff. for Bank1

Coeff. for Bank2

Coeff. for Bank3

Configure file will content all bank coeff. When you turn on auto bank.

a . Enable bank-1 write mode: Write to register 0x50 with 0x01. Load the 32-kHz coefficients.

b . Enable bank-2 write mode: Write to register 0x50 with 0x02. Load the 48-kHz coefficients.

c . Enable bank-3 write mode: Write to register 0x50 with 0x03. Load the other coefficients.

d . Enable automatic bank switching by writing to register 0x50 with 0x04.

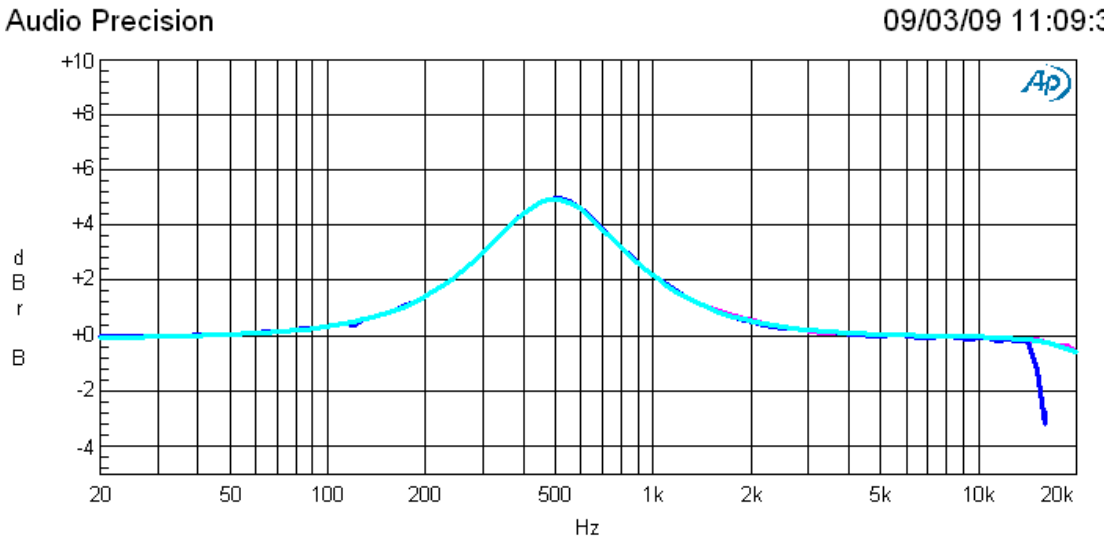
e. Bring the system out of all-channel shutdown: Write 0 to bit 6 of register 0x05.

f. Issue master volume: Write to register 0x07 with the volume value (0 db = 0x30)

Now, EQ Auto Bank has been turned on.

When input frequency change, correct coeff. will be loaded for them. Let's see results

EQ Curve with Auto Bank Switching



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Magenta	Solid	3	Anlr.Ampl	Left	48kHz
2	1	Blue	Solid	3	Anlr.Ampl	Left	32kHz
3	1	Cyan	Solid	3	Anlr.Ampl	Left	96kHz

Under different sample rate, frequency response of EQ is correct now.

EQ Advanced Function of 0x68/70 firmware

Devices with 0x68/0x70 ID provide some advanced functions:

BANK SWITCH AND EQ CONTROL (0x50)

Table 21. Bank Switching Command

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	–	–	–	–	–	–	–	**32 kHz, does not use bank 3** (1)
1	–	–	–	–	–	–	–	32 kHz, uses bank 3
–	0	–	–	–	–	–	–	Reserved
–	–	0	–	–	–	–	–	Reserved
–	–	–	**0**	–	–	–	–	**44.1/48 kHz, does not use bank 3** (1)
–	–	–	1	–	–	–	–	44.1/48 kHz, uses bank 3
–	–	–	–	0	–	–	–	16 kHz, does not use bank 3
–	–	–	–	**1**	–	–	–	**16 kHz, uses bank 3** (1)
–	–	–	–	–	0	–	–	22.025/24 kHz, does not use bank 3
–	–	–	–	–	**1**	–	–	**22.025/24 kHz, uses bank 3** (1)
–	–	–	–	–	–	0	–	8 kHz, does not use bank 3
–	–	–	–	–	–	**1**	–	**8 kHz, uses bank 3** (1)
–	–	–	–	–	–	–	0	11.025 kHz/12, does not use bank 3
–	–	–	–	–	–	–	**1**	**11.025/12 kHz, uses bank 3** (1)

0x68/70 firmware allow user to assign sample rate to any bank.
More sample rates are supported compared to 0x28 version

EQ Advanced Function of 0x70 firmware

More functions are provided to simplify EQ setting and control.

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0								**EQ ON**
1	–	–	–	–	–	–	–	EQ OFF (bypass BQ 0-6 of channels 1 and 2)
–	**0**	–	–	–	–	–	–	**Reserved** (2)
–	–	**0**	–	–	–	–	–	**Ignore bank-mapping in bits D31–D8.Use default mapping.** (2)
		1						Use bank-mapping in bits D31–D8.
–	–	–	**0**	–	–	–	–	**L and R can be written independently.** (2)
–	–	–	1	–	–	–	–	L and R are ganged for EQ biquads; a write to Left channel BQ is also written to Right channel BQ. (0X29-2F is ganged to 0X30-0X36.Also 0X58-0X5B is ganged to 0X5C-0x5F)
–	–	–	–	**0**	–	–	–	**Reserved** (2)
–	–	–	–	–	**0**	**0**	**0**	**No bank switching. All updates to DAP** (2)
–	–	–	–	–	0	0	1	Configure bank 1 (32 kHz by default)
–	–	–	–	–	0	1	0	Configure bank 2 (44.1/48 kHz by default)
–	–	–	–	–	0	1	1	Configure bank 3 (other sample rates by default)
–	–	–	–	–	1	0	0	Automatic bank selection
–	–	–	–	–	1	0	1	Reserved
–	–	–	–	–	1	1	X	Reserved

D7: EQ on/off control bit

D5: Enable/disable bank-mapping function for custom bank mapping

D4: Ganged EQ1 and EQ2

D2-D0 : Update bank function

Auto Bank for DRC Timing Parameters

- Not only EQ needs bank switching, DRC timing parameters are also related to input sampling frequency.
- DRC also use Auto Bank to deal with input sample rate changing.
- Only DRC timing parameters will be auto banked. Threshold, compress ratio, offset value don't need to be auto banked.

Step1: Generate Coefficient for different sampling frequency

- Choose Sample Rate in GDE.

Configuration	
CurrentDevice	TAS5705
CurrentRate	Rate96
CoefBanking	Disabled
Use441K	Disabled
Int21Mode	Off

- Generate DRC timing coeff. for this sample rate in DRC panel.
- Collect all three banks coeff. for programming.

Register Map for DRC Auto Bank Switching

Step 2: Follow this process to program all data to each bank.

T, K, O parameters are not related to Fs, so they are not bankable.

GDE now don't support generate all data at once, it will support later.

```
! DRCs
X50 00  00  00  01                          ---- Choose Bank1
X3A 00  00  22  1C  00  7F  DD  E1          ---- Write DRC1 AE for Bank1(32kHz)
X3B 00  00  22  1C  00  7F  DD  E1          ---- Write DRC1 AA for Bank1(32kHz)
X3C 00  00  22  1C  00  7F  DD  E1          ---- Write DRC1 AD for Bank1(32kHz)
X3D 00  00  66  3D  00  7F  99  C2          ---- Write DRC2 AE for Bank1(32kHz)
X3E 00  00  66  3D  00  7F  99  C2          ---- Write DRC2 AA for Bank1(32kHz)
X3F 00  00  66  3D  00  7F  99  C2          ---- Write DRC2 AD for Bank1(32kHz)
X50 00  00  00  02                          ---- Choose Bank2
X3A 00  00  22  1D  00  7F  DD  E2          ---- Write DRC1 AE for Bank2(48kHz)
X3B 00  00  22  1D  00  7F  DD  E2          ---- Write DRC1 AA for Bank2(48kHz)
X3C 00  00  22  1D  00  7F  DD  E2          ---- Write DRC1 AD for Bank2(48kHz)
X3D 00  00  44  32  00  7F  BB  CD          ---- Write DRC2 AE for Bank2(48kHz)
X3E 00  00  44  32  00  7F  BB  CD          ---- Write DRC2 AA for Bank2(48kHz)
X3F 00  00  44  32  00  7F  BB  CD |        ---- Write DRC2 AD for Bank2(48kHz)
X50 00  00  00  03                          ---- choose Bank3
X3A 00  00  22  1D  00  7F  DD  E2          ---- Write DRC1 AE for Bank3(96kHz)
X3B 00  00  22  1D  00  7F  DD  E2          ---- Write DRC1 AA for Bank3(96kHz)
X3C 00  00  22  1D  00  7F  DD  E2          ---- Write DRC1 AD for Bank3(96kHz)
X3D 00  00  44  32  00  7F  BB  CD          ---- Write DRC2 AE for Bank3(96kHz)
X3E 00  00  44  32  00  7F  BB  CD          ---- Write DRC2 AA for Bank3(96kHz)
X3F 00  00  44  32  00  7F  BB  CD          ---- Write DRC2 AD for Bank3(96kHz)
!DRC1 T K O                                 ---- T,K,O are the same for all banks
X40 FC  58  8B  89
X41 0F  84  44  45
X42 00  08  42  10
!DRC2 T K O
X43 FC  83  10  D4
X44 0F  C0  00  00
X45 00  08  42  10
X46 00  00  00  00                          ---- DRC1,2 ON/OFF Control
! Automatic bank selection
X50 00  00  00  04                          ---- Turn On Auto-Bank
```

Note: If you use EQ auto bank function, You must update DRC timing parameters in each bank

Digital Audio Processor Application

------- Loudness

Loudness Function for Good Listening

The loudness compensation function compensates for the Fletcher-Munson loudness curves.

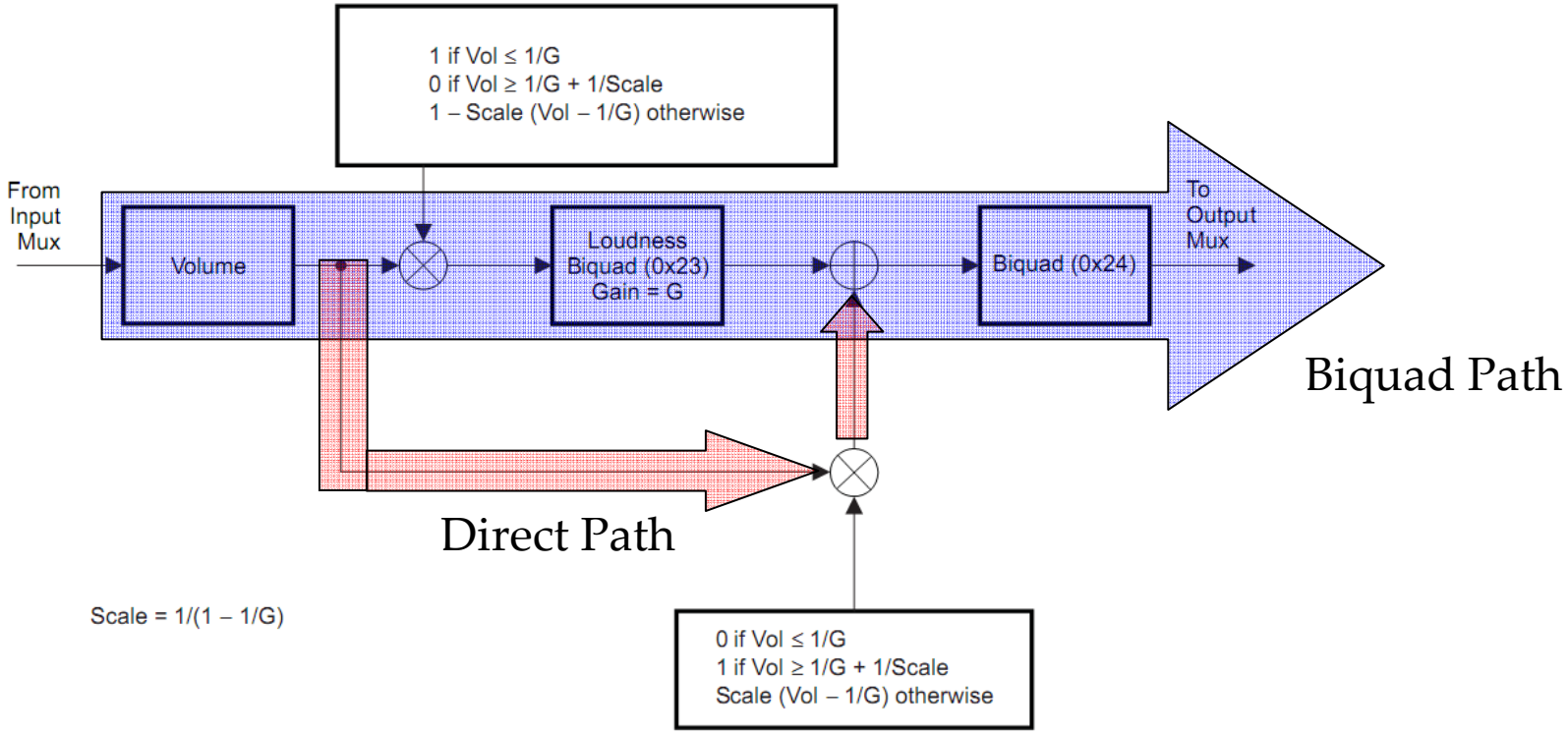
Loudness compensation employs a coefficient-programmable Biquad filter and the loudness gain, G, whose output is a function of only the volume control setting.

The following steps are involved in using a loudness Biquad with the volume compensation feature:

- Program the Biquad with a “Loudness Filter”.
- Program 0x26(1/G) and 0x28(Scale).
- Enable volume compensation in register 0x0E.

Note: “Loudness Filter” can be set as any type EQ filter, but in order to compensate Fletcher-Munson loudness curves, Bass Boost filter usually be used here. (See next page for details)

Example for Loudness Function



Loudness Table Example for Gain = 4, 1/G = 0.25, Scale = 1.33

Volume	0.125	0.25	0.375	0.5	0.625	0.75	0.875	1	1.125	1.25	1.375	1.5	1.625	1.75	1.875	2
Biquad path	1	1	0.833	0.666	0.5	0.333	0.166	0	0	0	0	0	0	0	0	0
Direct path	0	0	0.166	0.333	0.5	0.666	0.833	1	1	1	1	1	1	1	1	1
Total gain	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

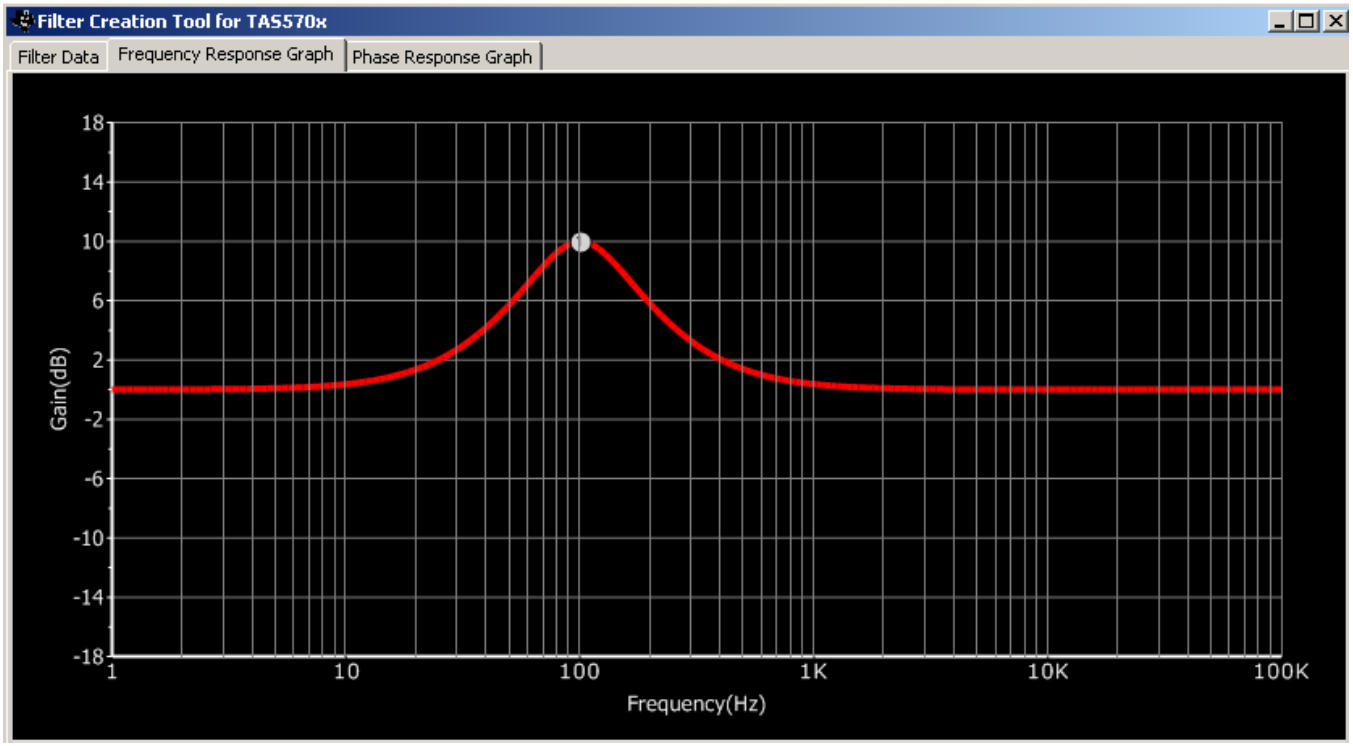
Example for Loudness Function

Step 1 : Program Loudness Filter

EQ filter with boost around bass frequency is used as “Loudness Filter”.

Example curve shows EQ filter with following parameters:

Fc:100Hz Gain:10dB band width:100Hz



Loudness Filter

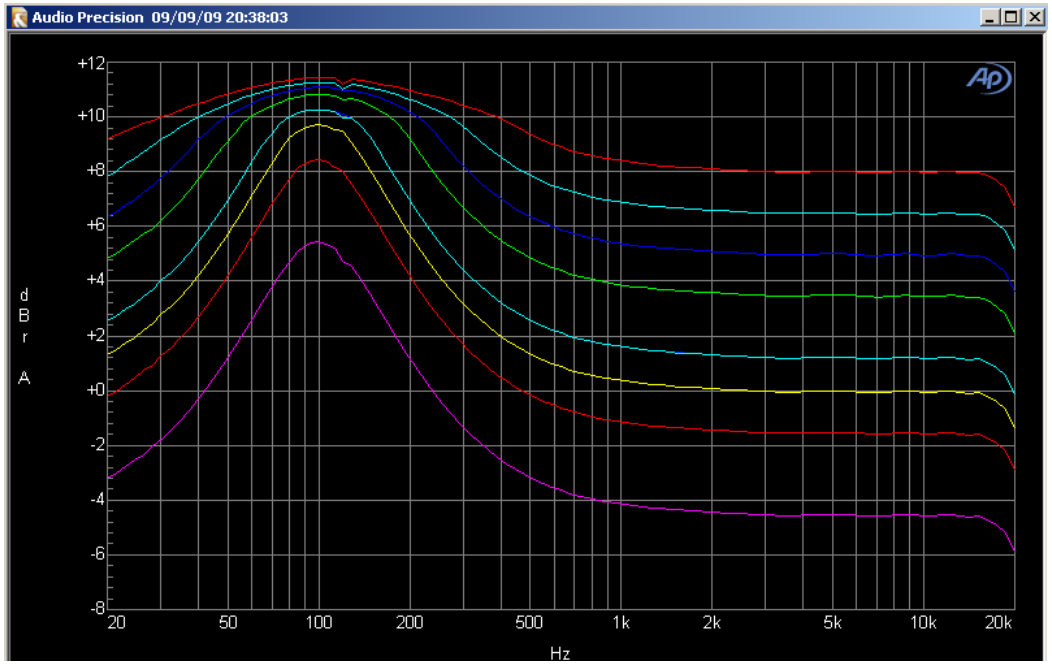
Example for Loudness Function

Step2: Enable Loudness Function by writing 1/G and Scale to device

a) 1/G is set to 0.25 (HEX:00200000) Scale is 1.33(HEX:00AA3D70)

b) Program 0x00200000 to 0x26, 0x00AA3D70 to 0x28

c) Set bit6 of 0x0E to enable Loudness compensation.



Loudness Example Test Curve

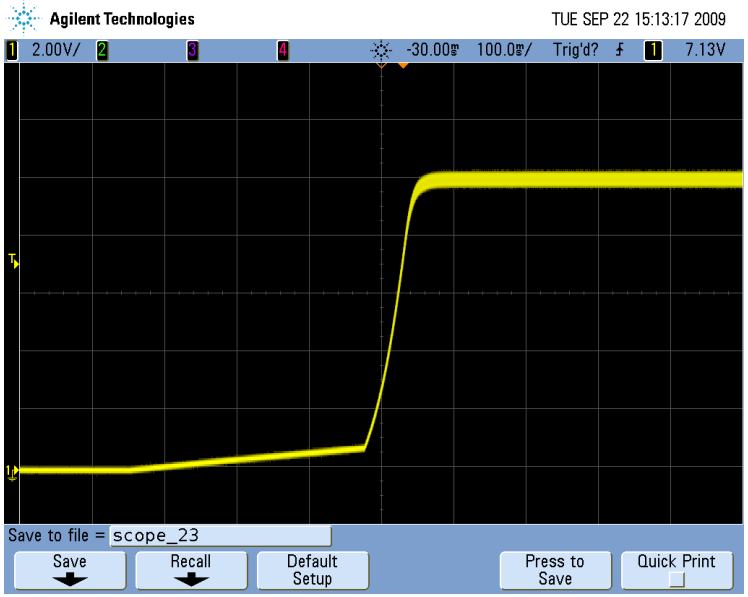
When the volume is low: EQ filter shows 100% gain as pre-set value.

When the volume is high: EQ filter shows reduced gain applied to signal.

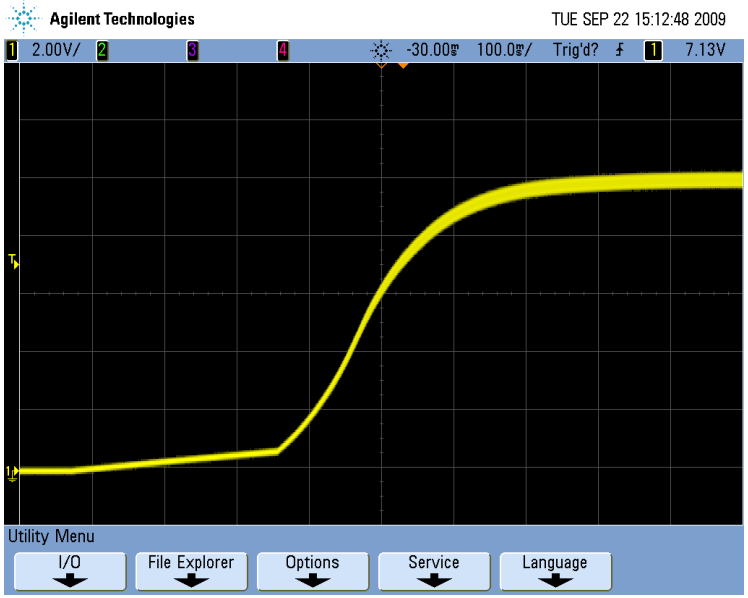
Other Critical Registers

Soft Start Up Register ---- 0x1A

Bit D7 : BTL or SE mode



0x0A --- BTL Mode



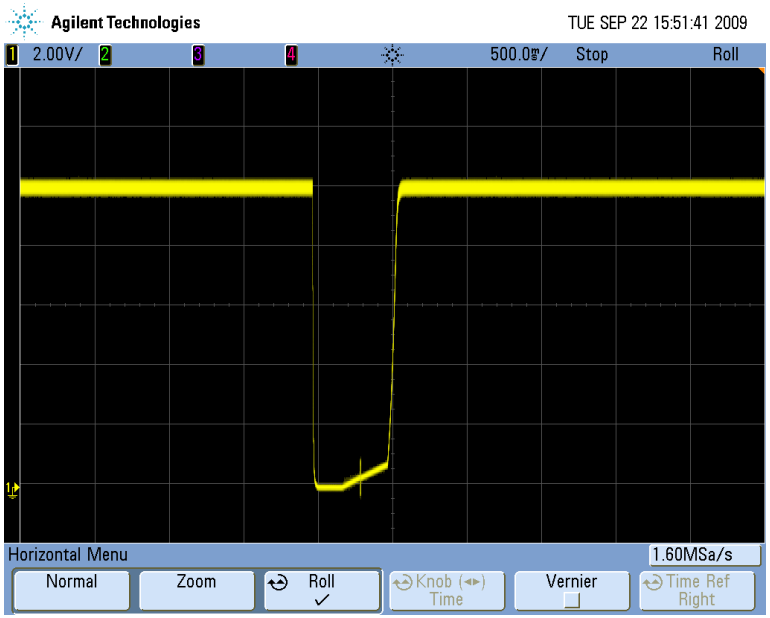
0x8A --- SE Mode

Note: Ramp up time for SE configuration is set by SSTIMER or BYPASS pin capacitance, see following Pin description:

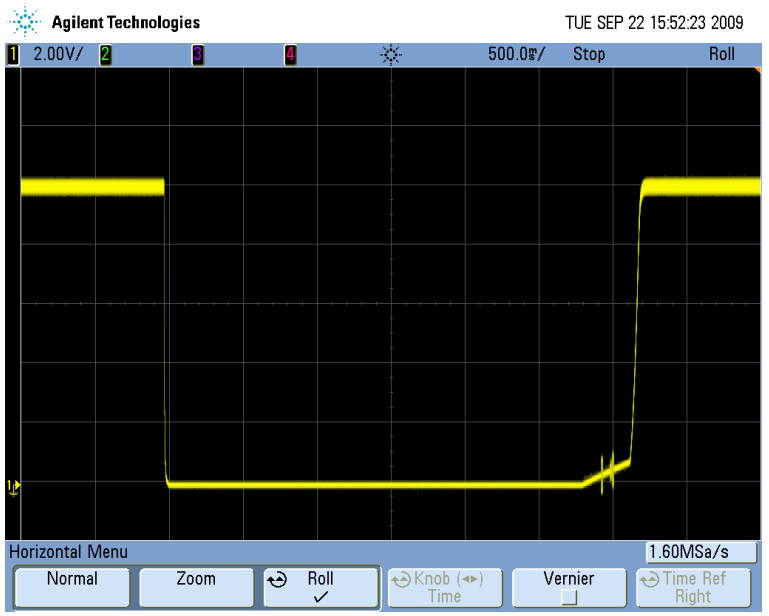
SSTIMER	Controls ramp time of OUT_X to minimize pop. Leave this pin floating for BD mode. Requires capacitor of 2.2 nF to GND in AD mode. The capacitor determines the ramp time.			
t_{ON}	Turnon time (SE mode) (Set Reg 0x1A bit 7 to 1)	$C_{(BYPASS)}$ = 1 µF, Time required for the $C_{(BYPASS)}$ to reach its final value	500	ms
	Turnon time (BTL mode) (Set Reg 0x1A bit 7 to 0)		30	
t_{OFF}	Turnoff time (SE mode) (Set Reg 0X1A bit 7 to 1)		500	ms
	Turnoff time (BTL mode) (Set Reg 0X1A bit 7 to 0)		30	

Soft Start Up Register ---- 0x1A

Bit D4 – D0 : Delay between Power OFF and ON (Blank Time)



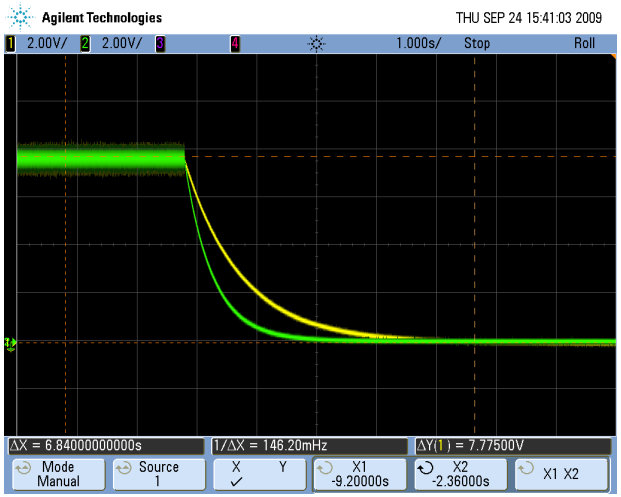
0x0A



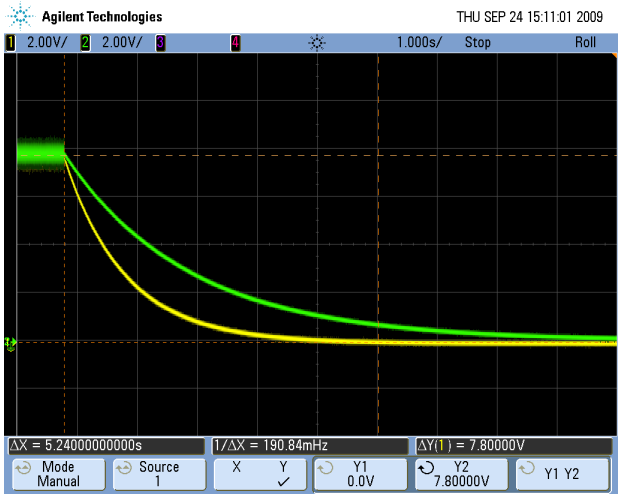
0x1A

These Bits determine the delay time between Power OFF and next time Power On. It can be used to avoid POP noise due to DC block capacitor discharge in single ended configuration.

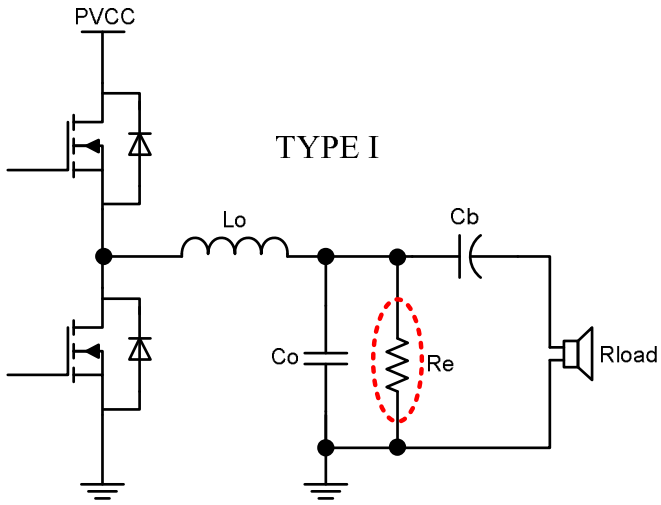
Turn ON POP noise for SE output



Cap:220uF, Yellow: 2.2K; Green: 4.7K;



Cap: 470uF, Yellow: 2.2K; Green: 4.7K;



Turn On must be issued after DC Blocking cap fully discharge, reduce capacitance and discharge resistor can reduce discharge time.

Due to TAS5706B has Hi-Z output during shut down, discharge speed will be lower than TAS5706A.

Recommended Configuration					
TAS5706A			TAS5706B or Hi-Z Parts		
C(uF)	R(kΩ)	T(mS)	C(uF)	R(kΩ)	T(mS)
470	2.2	4.5	220	1	1

TAS5711 Section

3D Effect Overview

- Supported Products : TAS5716, TAS5709/10
- Basic formula for implementing 3D Surround

$$L_{3D} = L - hpf\{\tfrac{1}{2}(R-L)\}$$

$$R_{3D} = R - hpf\{\tfrac{1}{2}(L-R)\}$$

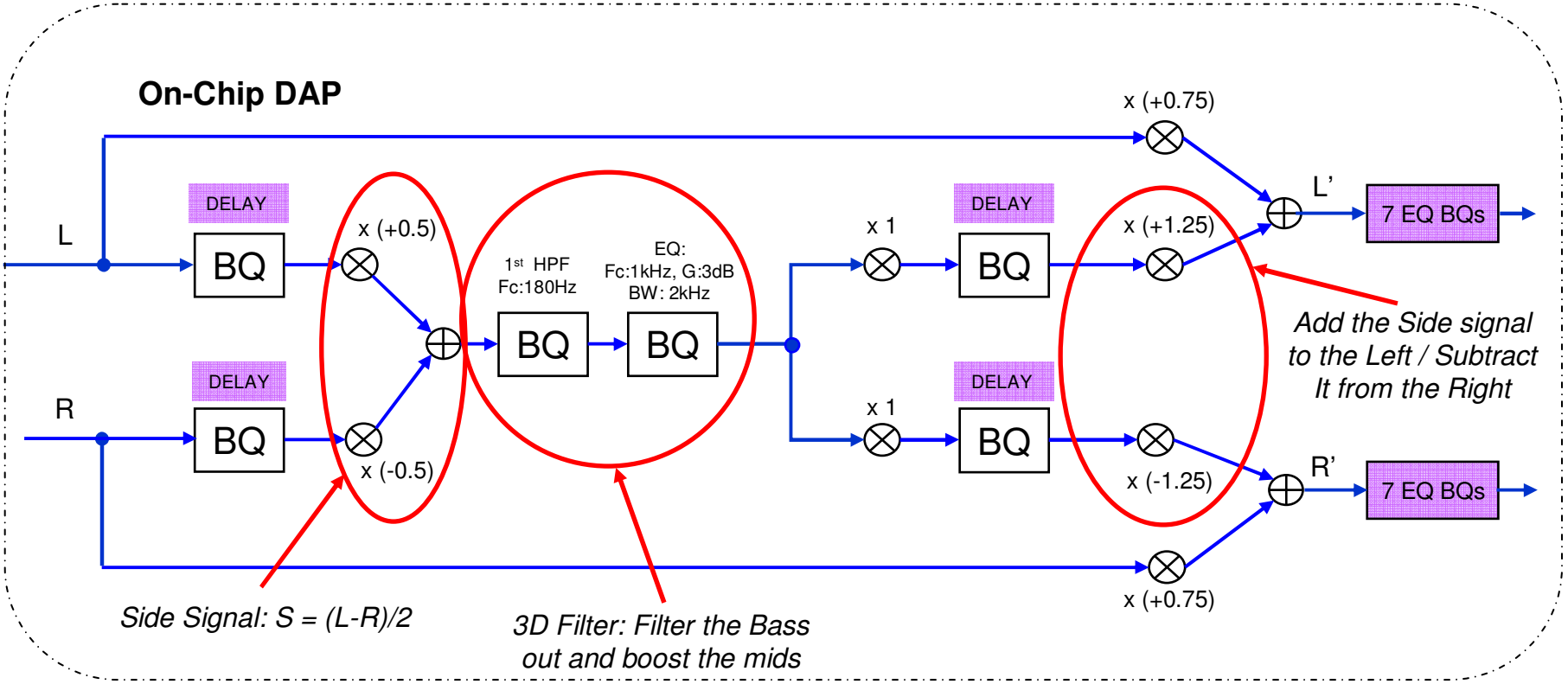
- Low-frequency energy in the music of most stereo audio tracks is monaural (i.e., left and right channels are the same) and non-directional.

- We can easily vary the amount of 3D effects

$$L_{3D} = a \cdot L - b \cdot hpf\{\tfrac{1}{2}(R-L)\}$$

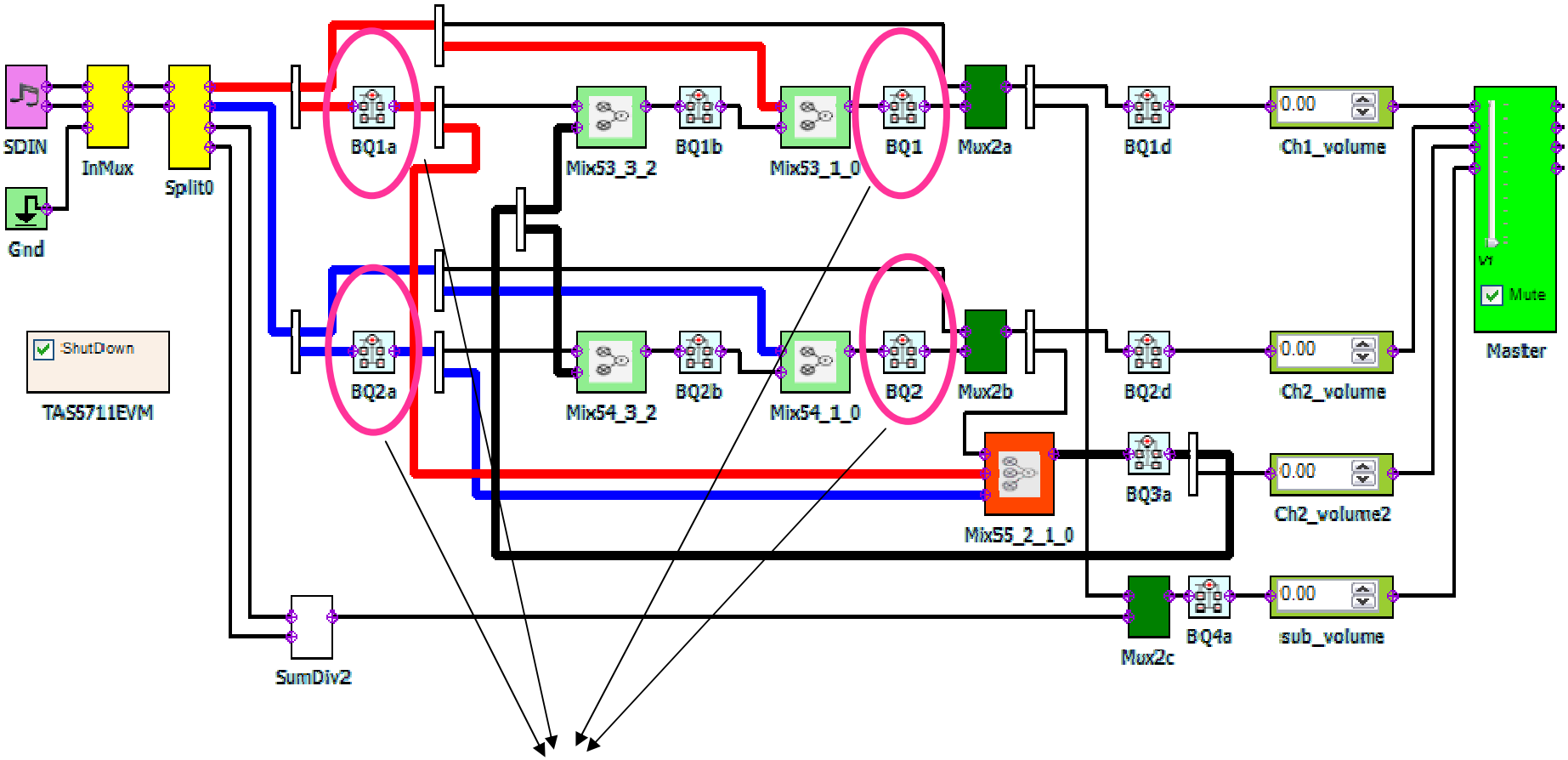
$$R_{3D} = c \cdot R - d \cdot hpf\{\tfrac{1}{2}(L-R)\}$$

3D Overview



- Enhanced Audio Experience with soundstage widening
- 3D algorithm can be fine tuned. The mixers, Biquad filters, etc. are programmable.
- Audio Processing Supported
  - 3D Effects + Speaker EQ (7 BQ per L/R) + Bass Boost

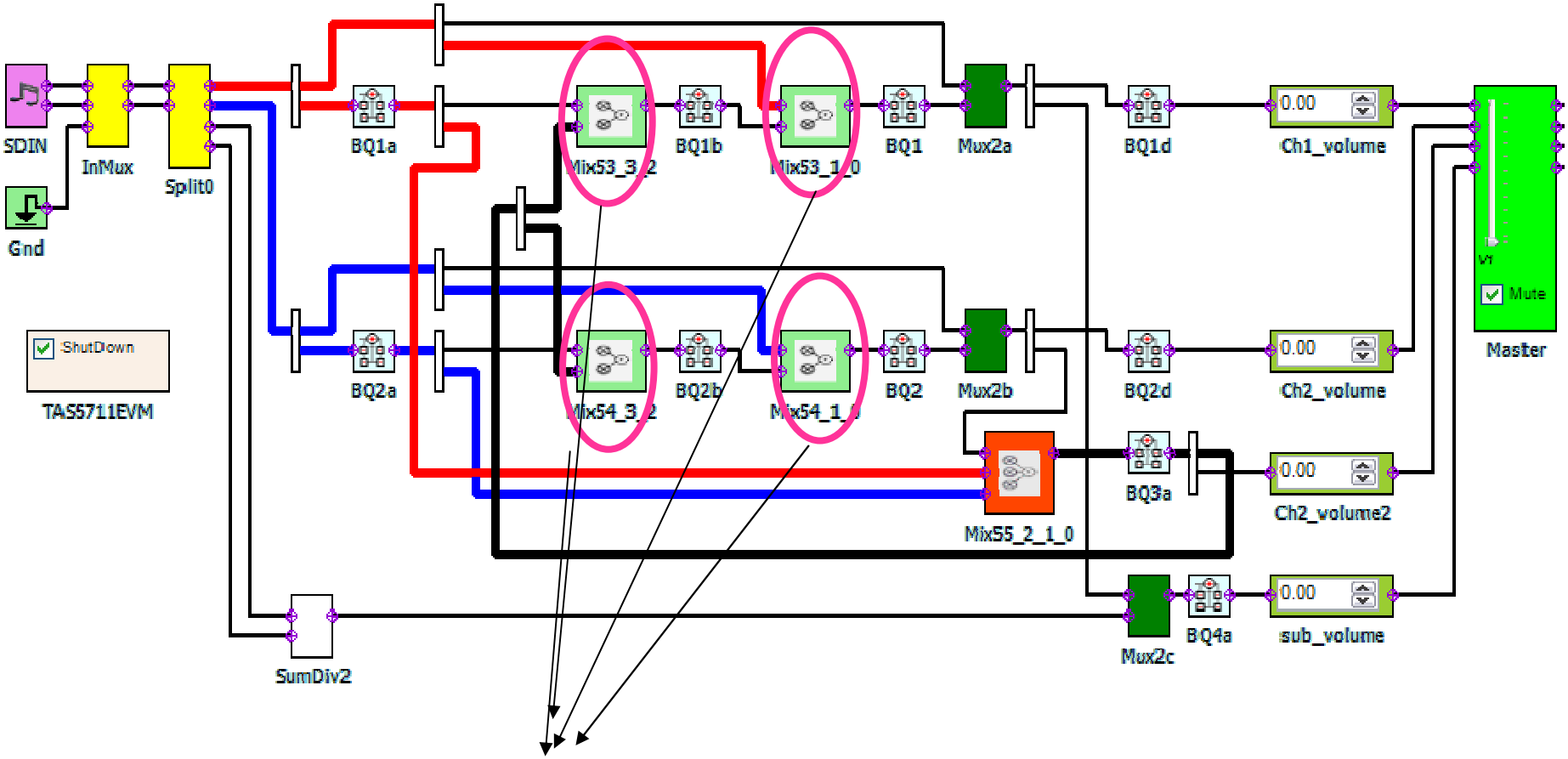
3D Effect ----- Delay EQ



Delay Registers: 0x29, 0x2A, 0x30, 0x31

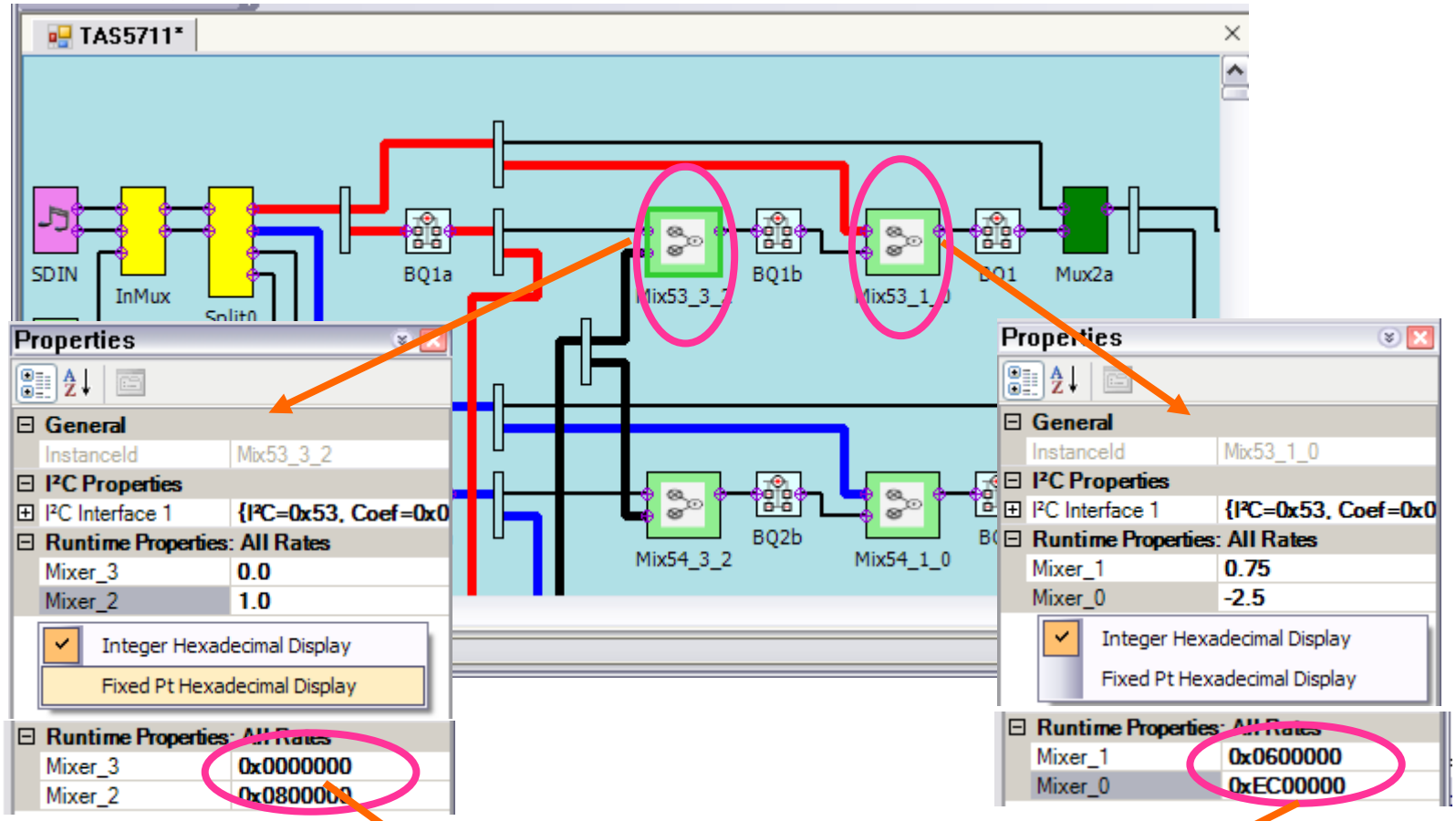
Value: bq_3D_delay[]={0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x80, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00};

3D Effect ---- Mixer



Registers: 0x53, 0x54, 0x55

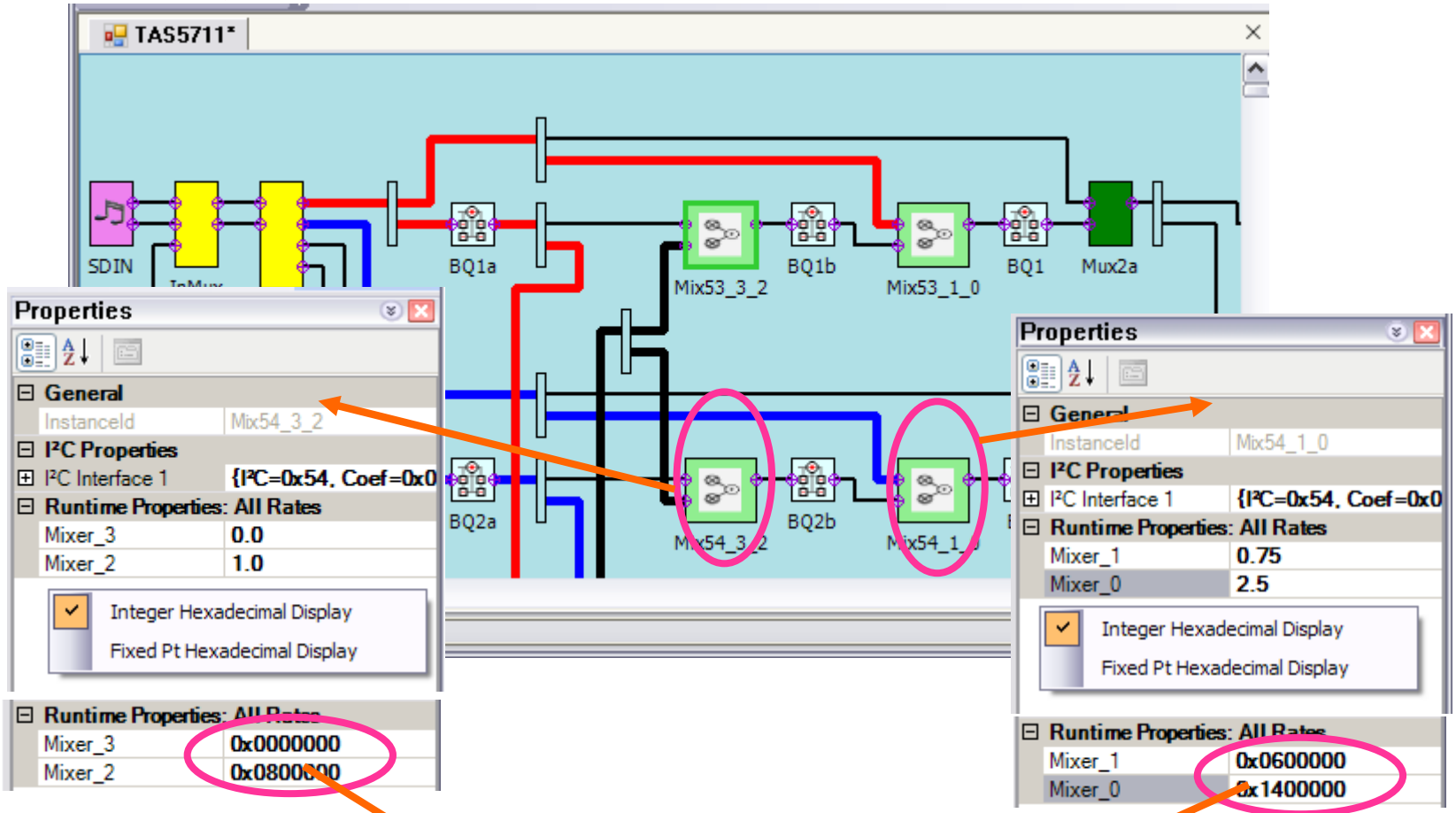
Mixer53, Parameters



Right Click to change display between Hex and Oct

Set mixer gain for each input, then switch to Hex display to get value as below:
Mixer53[]={0x00, 0x00, 0x00, 0x00, 0x00, 0x80, 0x00, 0x00, 0x00, 0x60, 0x00, 0x00, 0x0E, 0xC0, 0x00, 0x00 };

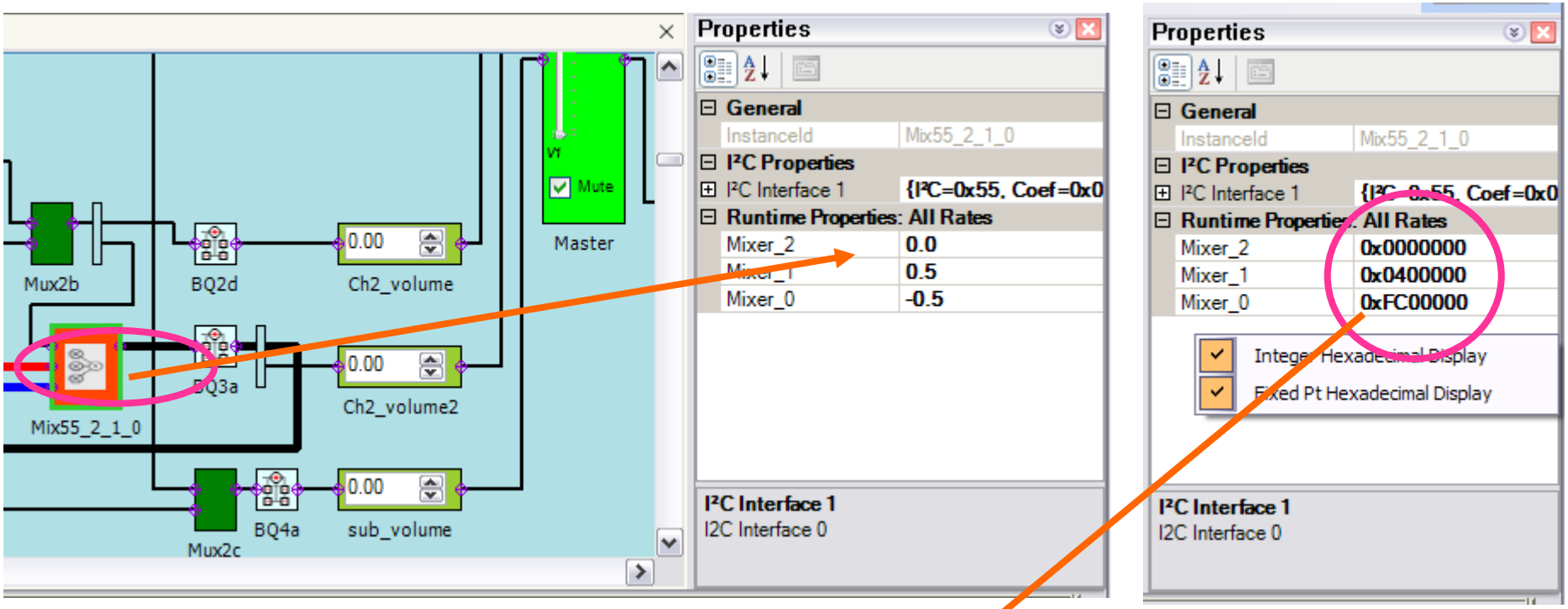
Mixer54, Parameters



Right Click to change display between Hex and Oct

Set mixer gain for each input, then switch to Hex display to get value as below:
Mixer54[]={0x00, 0x00, 0x00, 0x00, 0x00, 0x80, 0x00, 0x00, 0x00, 0x60, 0x00, 0x00, 0x01, 0x40, 0x00, 0x00 };

Mixer54, Parameters



Set mixer gain for each input, then switch to Hex display to get value as below:
Mixer55[]={0x00, 0x00, 0x00, 0x00, 0x00, 0x40, 0x00, 0x00, 0x0F, 0xC0, 0x00, 0x00 };