INTERNATIONAL STANDARD

ISO/IEC 14443-3

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AMENDMENT 1
2005-06-01

Identification cards — Contactless integrated circuit(s) cards — Proximity cards —

Part 3: Initialization and anticollision —

AMENDMENT 1: Bit rates of *fc*/64, *fc*/32 and *fc*/16

Cartes d'identification — Cartes à circuit(s) intégré(s) sans contact — Cartes de proximité —

Partie 3: Initialisation et anticollision

AMENDEMENT 1: Débits binaires de fc/64, fc/32 et fc/16

Reference number
ISO/IEC 14443-3:2001/Amd.1:2005(E)

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Identification cards — Contactless integrated circuit(s) cards — Proximity cards —

Part 3: Initialization and anticollision

AMENDMENT 1: Bit rates of *fc*/64, *fc*/32 and *fc*/16

Page 2, term number 3.5

Replace the existing definition with the following:

"**elementary time unit**
etu
time unit calculated by the following formula:

1 etu = 128 / (D x *fc*)

where

D ∈ {1,2,4,8}

fc is the carrier frequency as defined in ISO/IEC 14443-2.

The initial value of the divisor D is 1, giving the initial etu as follows: 1 etu = 128 / *fc*.

Page 3, Clause 4

Add the following new abbreviations:

"D Divisor

TR2 Frame delay Time PICC to PCD, Type B"

Page 5, Clause 5

Replace the existing Clause 5 title with the following:

"

5 Alternating between Type A and Type B commands,

5.1 Polling

"

Add the following at the end of the new subclause 5.1:

"EXAMPLE 3 When a PICC Type A is exposed to field activation it shall be able to accept a REQA within 5 ms of unmodulated operating field.

EXAMPLE 4 When a PICC Type B is exposed to field activation it shall be able to accept a REQB within 5 ms of unmodulated operating field.

5.2 Influence of Type A commands on PICC Type B operation

A PICC Type B should either go to IDLE state (be able to accept a REQB) or be able to continue a transaction in progress after receiving any Type A command.

5.3 Influence of Type B commands on PICC Type A operation

A PICC Type A should either go to IDLE state (be able to accept a REQA) or be able to continue a transaction in progress after receiving any Type B command.

5.4 Transition to Power OFF state

The PICC shall be in the Power OFF state no later than 5 ms after the operating field is switched off."

Page 5, Clause 6

Insert the following new subclause before the existing subclause 6.1 and renumber all subsequent subclauses.

"**6.1 Bit rates**

Communication between PCD and PICC can be achieved with four different bit rates (see Table Amd.1-1).

Bit rates of *fc*/64, *fc*/32 and *fc*/16 are optional and may be independently supported by PCD and PICC.

Table Amd.1-1 — Bit rates

Divisor D	etu	Bit rate
1	128/*fc* (~9,4 µs)	*fc*/128 (~106 kbit/s)
2 (optional)	128/(2*fc*) (~4,7 µs)	*fc*/64 (~212 kbit/s)
4 (optional)	128/(4*fc*) (~2,4 µs)	*fc*/32 (~424 kbit/s)
8 (optional)	128/(8*fc*) (~1,2 µs)	*fc*/16 (~847 kbit/s)

NOTE The initial bit rate is fc/128. This applies for the whole initialization and anticollision sequence."

Page 6, subclause 6.1.2 (renumbered to 6.2.2)

Replace Figure 1 with the following:

"

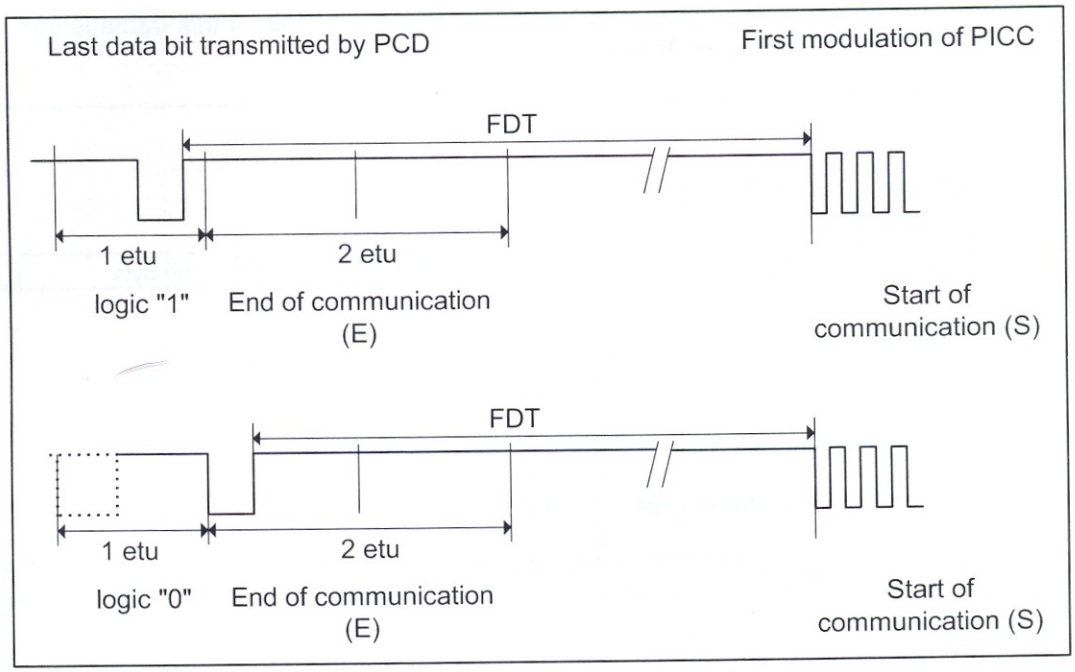

Figure 1 — Frame delay time PCD to PICC"

Replace Table 1 and the last two sentences of subclause 6.1.2 (renumbered to 6.2.2) with the following:

"Table 1 — Frame delay time PCD to PICC

Command type		n (integer value)	FDT	
			last bit = (1)b	last bit = (0)b
REQA Command WUPA Command ANTICOLLISION Command SELECT Command		9	(*n**128+84)/*fc* [= 1236/*fc*]	(*n**128+20)/*fc* [= 1172/*fc*]
All other commands at bit rates				
PCD to PICC	PICC to PCD			
fc/128	*fc*/128	≥ 9	(*n**128+84)/*fc*	(*n**128+20)/*fc*
fc/64		≥ 8	(*n**128+148)/*fc*	(*n**128+116)/*fc*
fc/32		≥ 8	(*n**128+116)/*fc*	(*n**128+100)/*fc*
fc/16		≥ 8	(*n**128+100)/*fc*	(*n**128+92)/*fc*
fc/128 or *fc*/64 or *fc*/32 or *fc*/16	*fc*/64 or *fc*/32 or *fc*/16	Not applicable	≥ 1116/*fc*	≥ 1116/*fc*
All PICCs in the field shall respond in a synchronous way to the commands REQA, WUPA, ANTICOLLISION and SELECT. This is needed for anticollision.				

The FDT tolerance is in the range of -0 to +0,4 µs (derived from t4 defined in ISO/IEC 14443-2:2001, Figure 3)."

Page 7, subclause 6.1.5.2 (renumbered to 6.2.5.2)

Add the following text and figure after Figure 3:

"

As an exception the last parity bit of a PICC standard frame shall be inverted if this frame is transmitted with bit rate of *fc*/64, *fc*/32 or *fc*/16 (see Figure Amd.1-1).

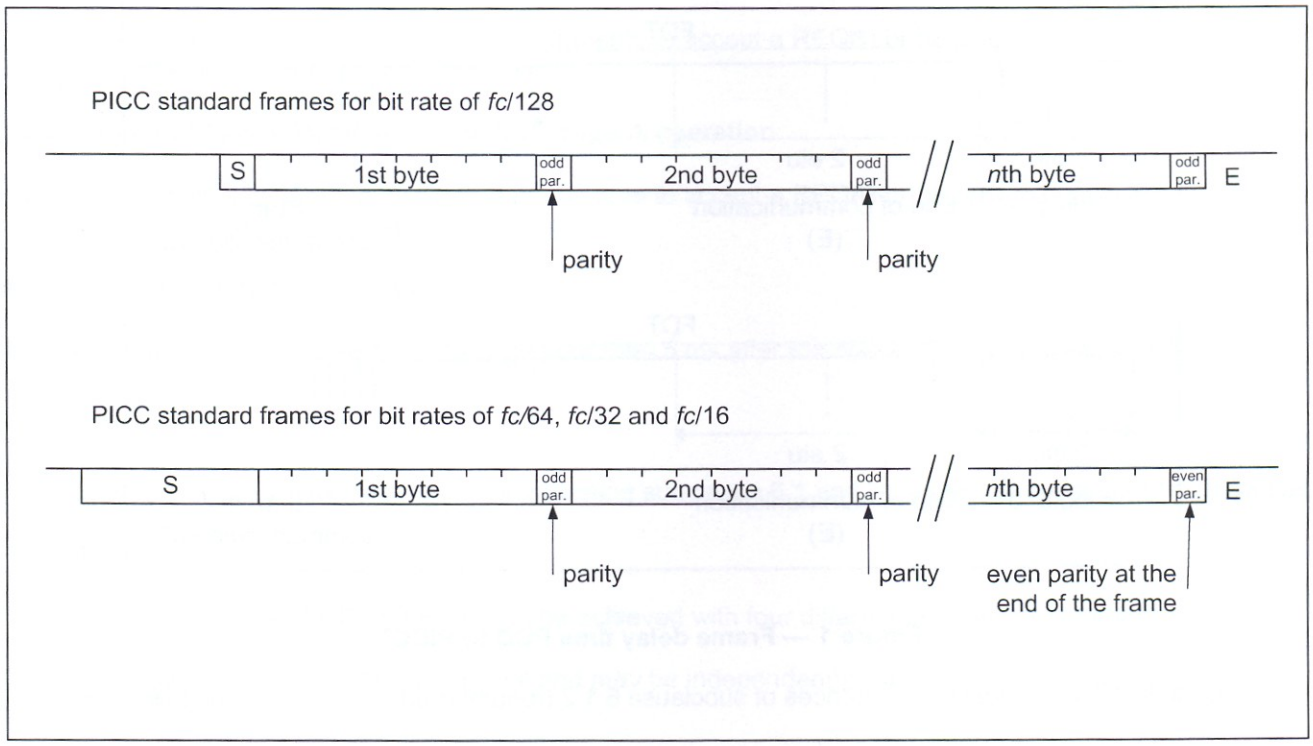

Figure Amd.1-1 — PICC standard frames"

Page 10, subclause 6.2 (renumbered to 6.3)

Add the following text between the lines beginning DESELECT and Error:

"RATS RATS Command defined in ISO/IEC 14443-4"

Page 10, Figure 6

Replace the text "ISO/IEC 14443-4" in the state bubble with "PROTOCOL state" and replace the text "Enter ISO/IEC 14443-4" between the arrows with "RATS".

Page 14, Clause 6.4.1 (renumbered to 6.5.1)

Replace Figure 8 with the following figure:

"

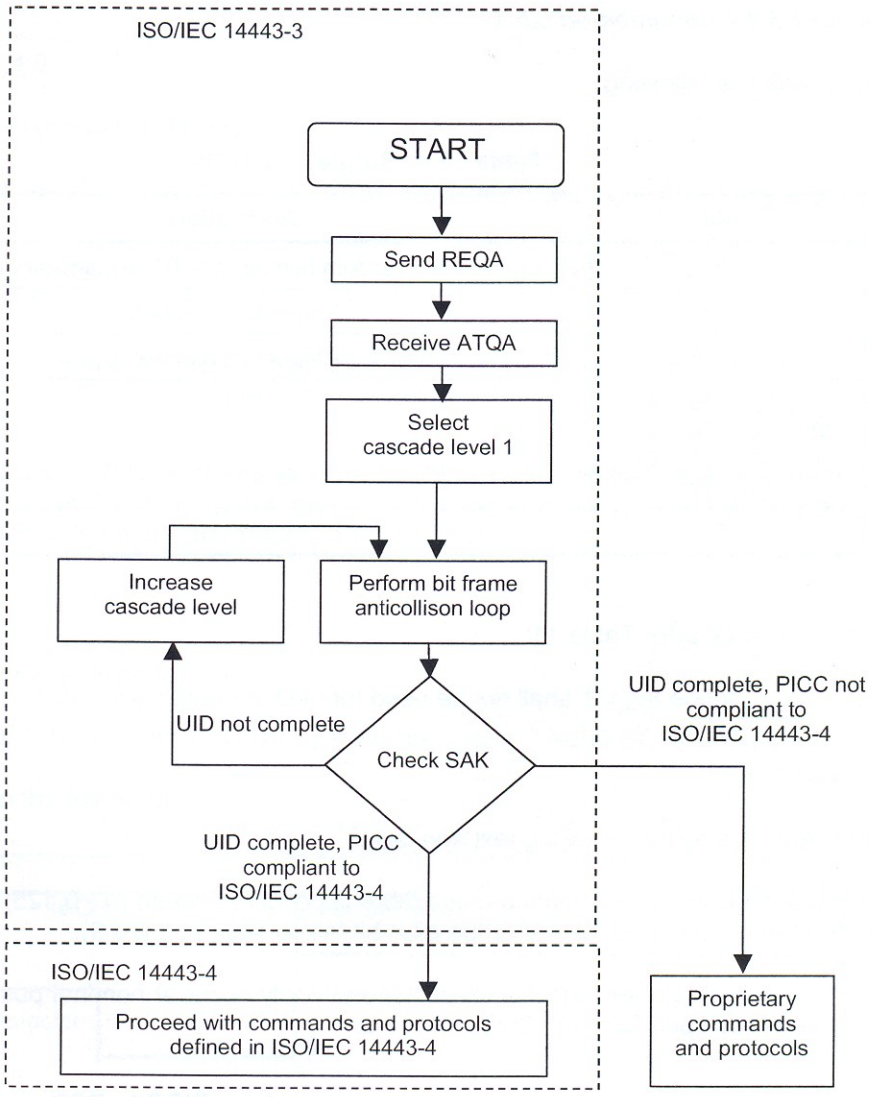

Figure 8 — Initialization and anticollision flowchart for PCD"

Page 14, subclause 6.4.1 (renumbered 6.5.1)

Add the following note and text after modified Figure 8:

"NOTE PICCs may use ATQA bit combinations of b9 to b12 for indication of proprietary methods.

PICCs that do not support the mandatory bit frame anticollision are not compliant with this standard."

Page 15, subclause 6.4.2.2 (renumbered 6.5.2.2)

Delete "NOTE Bit 9 to bit 12 indicate additional and proprietary methods"

Page 18, subclause 6.4.3.4 (renumbered 6.5.3.4)

Add the following note after Table 8:

"NOTE x represents a proprietary value"

Page 19, subclause 6.4.4 (renumbered 6.5.4)

Replace Table 10 with the following:

"Table 10 — Single size UIDs

uid0	Description
'08'	uid1 to uid3 is a random number which is dynamically generated
'x0' - 'x7'	Proprietary number
'x9' - 'xE'	Proprietary number
'18', '28', '38', '48', '58', '68', '78', '98', 'A8', 'B8', 'C8', 'D8', 'E8', 'F8'	RFU
'xF'	RFU

"

Add the following sentence after Table 11:

"The value '88' of the cascade tag CT shall not be used for uid3 in double size UID."

Page 21, subclause 7.1.1

Replace the last sentence by the following text and table.

"From PCD to PICC, bit boundaries within a character shall occur between (n - 0,125) etu and (n + 0,125) etu where n is the number of bit boundaries after the start bit falling edge ($1 \leq n \leq 9$).

From PICC to PCD, bit boundaries within a character shall only occur at nominal positions of rising or falling edges of the subcarrier as specified in ISO/IEC 14443-2:

Table Amd.1-2 — Bit boundaries from PICC to PCD

	PICC to PCD bit rate			
	***fc*/128** (1 etu = 8/*fs*)	***fc*/64** (1 etu = 4/*fs*)	***fc*/32** (1 etu = 2/*fs*)	***fc*/16** (1 etu = 1/*fs*)
Bit boundaries from PICC to PCD	n etu $\pm$ 1/*fs*	n etu $\pm$ 1/(2*fs*)	n etu	n etu

"

Page 21, subclause 7.1.2

Replace the existing text by the following:

"A character is separated from the next one by the extra guard time EGT.

The EGT between 2 consecutive characters sent by the PCD to the PICC shall be between 0 and 6 etu (not necessarily an integer number of etu).

The EGT between 2 consecutive characters sent by the PICC to the PCD shall be between 0 and 2 etu (not necessarily an integer number of etu)."

Page 22, subclause 7.1.6

Replace the third paragraph with the following:

"The maximum value of TR0 is 256/*fs* for ATQB only and $(256/fs)*2^{FWI}$ – TR1 for all other frames (see 7.9.4.3)."

Page 22, subclause 7.1.6

Insert the following warning notice after the new third paragraph for consistency with ISO/IEC 14443-4:2001, 7.2, Frame waiting time:

"WARNING — The value of TR0 is changed from ISO/IEC 14443-3:2001. TR0 is reduced by TR1 in the new definition of TR0. PCDs waiting no more than this new value of TR0 may not communicate properly with Type B PICCs based on ISO/IEC 14443-3:2001."

Page 23, subclause 7.1.7

Replace the last sentence with the following:

"The minimum value of TR2 is coded in ATQB by Protocol_type in "Protocol Info" field (see 7.9.4.4)."

Replace Figure 17 with the following: "

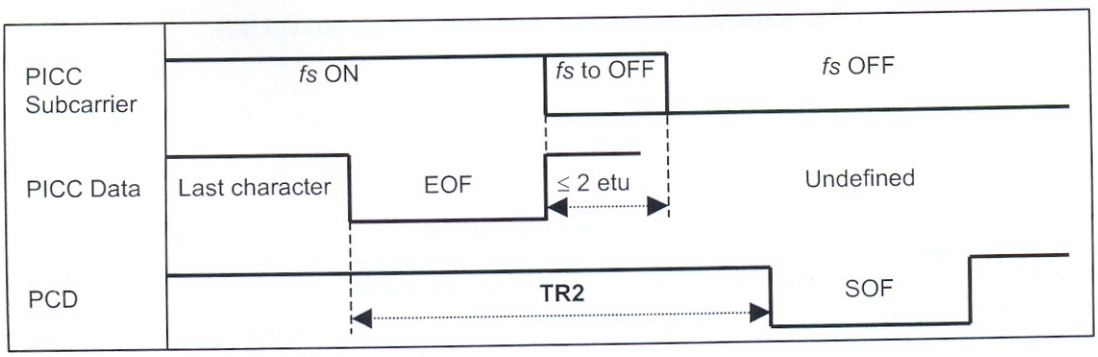

Figure 17 — PICC to PCD EOF"

Page 33, subclause 7.9.4.4

Replace 7.9.4.4 with the following.

"**7.9.4.4 Protocol_Type**

Table Amd.1-3 — Compliance with ISO/IEC 14443-4

b1	Meaning
1	PICC compliant with ISO/IEC 14443-4
0	PICC not compliant with ISO/IEC 14443-4

The minimum value of TR2 (delay between PICC EOF start and PCD SOF start) is defined by Protocol_Type bits (b3,b2) as specified in Table Amd.1-4.

Table Amd.1-4 — Minimum TR2 coding

b3	b2	Minimum TR2 for PICC to PCD bit rate of			
		***fc*/128** (1 etu = 8/*fs*)	***fc*/64** (1 etu = 4/*fs*)	***fc*/32** (1 etu = 2/*fs*)	***fc*/16** (1 etu = 1/*fs*)
0	0	10 etu + 32/*fs*	10 etu + 32/*fs*	10 etu + 32/*fs*	10 etu + 32/*fs*
0	1	10 etu + 32/*fs*	10 etu + 32/*fs*	10 etu+ 32/*fs*	26 etu
1	0	10 etu + 32/*fs*	10 etu+ 32/*fs*	18 etu	18 etu
1	1	10 etu + 32/*fs*	14 etu	14 etu	14 etu

The bit b4 is RFU and shall be set to 0."

Page 33, subclause 7.10

Add the following sentence before 7.10.1:

"The parameters selected in the ATTRIB command shall apply after the Answer to ATTRIB."

Page 34, subclause 7.10.3.1

Replace Table 20 with the following:

"Table 20 — Minimum TR0 coding

b8	b7	Minimum TR0 for PCD to PICC bit rate of			
		***fc*/128**	***fc*/64**	***fc*/32**	***fc*/16**
0	0	64/*fs*	64/*fs*	64/*fs*	64/*fs*
0	1	48/*fs*	32/*fs*	16/*fs*	16/*fs*
1	0	16/*fs*	8/*fs*	4/*fs*	4/*fs*
1	1	RFU	RFU	RFU	RFU

"

Page 34, subclause 7.10.3.2

Replace Table 21 with the following:

"**Table 21 — Minimum TR1 coding**

b6	b5	Minimum TR1 for PCD to PICC bit rate of			
		***fc*/128**	***fc*/64**	***fc*/32**	***fc*/16**
0	0	80/*fs*	80/*fs*	80/*fs*	80/*fs*
0	1	64/*fs*	32/*fs*	32/*fs*	32/*fs*
1	0	16/*fs*	8/*fs*	8/*fs*	8/*fs*
1	1	RFU	RFU	RFU	RFU

"

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