

## RemoTI™ IR Signal Generation Application Note

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### Keywords

- *RemoTI™*
- *CC2530*
- *CC2531*
- *CC2533*
- *Infrared (IR)*
- *ZigBee RF4CE*
- *ZigBee Remote Control*
- *Target Board*

### 1 Introduction

Although ZigBee RF4CE based remote controllers are replacing traditional IR remote controllers at a fast pace, manufacturers of RF4CE remote controllers may still want to support IR to control legacy consumer electronics equipment. Additionally, manufacturers of consumer electronics equipment may want to enable RF4CE with minimal changes to their current system. This can be accomplished by an RF4CE-to-IR bridge solution.

The CC253x devices used in RF4CE remote control systems provide hardware resources for generation of IR signals to enable minimal CPU intervention. This enables RF4CE remote control and manufacturers with a cost effective approach to support legacy consumer electronics equipment.

This application note provides information for how use this hardware capability in the RemoTI software environment and also a sample implementation of three different IR encoding formats.

The objective of this application note is not to provide the command database for the different IR formats, rather, to educate the reader to be able to use the hardware resources for their desired format based on the provided sample implementations.

RemoTI is Texas Instrument's implementation of the ZigBee RF4CE network protocol standard. You can find more information about RF4CE at [www.zigbee.org/rf4ce](http://www.zigbee.org/rf4ce) and [www.ti.com/rf4ce](http://www.ti.com/rf4ce), and RemoTI at [www.ti.com/RemoTI](http://www.ti.com/RemoTI).

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## 2 Abbreviations

EM	Evaluation module
LED	Light Emitting Diode
IR	Infrared
ISR	Interrupt Service Routine
LSB	Least Significant Bit
MAC	Medium Access Control
MSB	Most Significant Bit
RAM	Random Access Memory
RF	Radio Frequency
RF4CE	Radio Frequency for Consumer Electronics
OSAL	Operating System Abstraction Layer
HAL	Hardware Abstraction Layer
NV	Non-Volatile (memory)
ZRC	ZigBee Remote Control

### 3 Introduction to IR Signals

A wide variety of both standard and proprietary IR signal formats is used in consumer electronics equipment. The IR formats can be divided into three main categories or combinations of these;

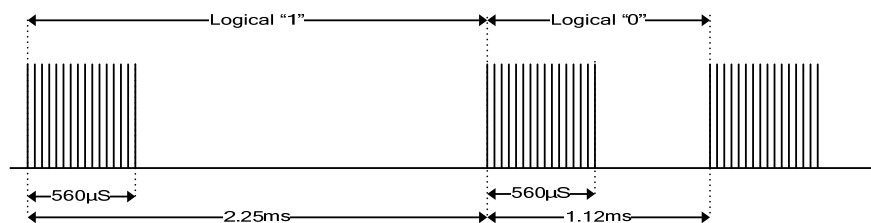
- Pulse distance modulation
- Pulse width modulation
- Manchester (bi-phase) modulation

The pros and cons of the different modulation techniques will not be discussed in this application note; however, we will discuss their differences and how to use the CC253x family of devices to generate the IR formats. The NEC, RC5 and SIRC formats are used as examples of the different formats and the sample drivers and applications accompanying this application note implements these three formats. [1] is used as the reference for the details of the modulation formats.

#### 3.1 NEC IR Format

##### 3.1.1 Modulation

The NEC format uses the pulse distance modulation technique. Pulse distance modulation is based on varying the pulse duty cycle for a logical "1" and "0" while keeping the pulse active period constant. Figure 1 below illustrates the principle of pulse distance modulation.



**Figure 1 NEC Format - Pulse Distance Modulation**

NEC format timing information:

- Carrier: 38 kHz with 1/3 or 1/4 duty cycle
- Active period: 560 µS
- Duty Cycle
  - Logical "1": 2.25 ms
  - Logical "0": 1.12 ms

##### 3.1.2 Protocol

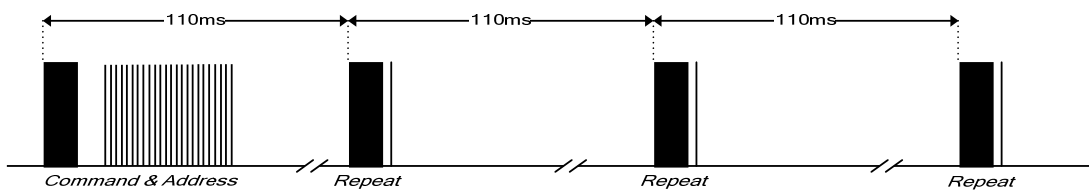
The NEC protocol uses a 8-bit command and a 8-bit address length for each transfer. The command and address bits are preceded by a preamble with active period of 9 ms and duty cycle of 13.5 ms. The command and address bits are transfer a second time with all bits inverted for increased reliability. Each command and data byte are transferred with the LSB first. A trailing stop bit is used to indicate the end of frame. See Figure 2 below for an illustration of the protocol.



**Figure 2 NEC Protocol**

### 3.2 Repeat Sequence

The protocol described in Figure 2 is transmitted once. A repeat pattern consisting of a preamble of active period 9 ms and duty cycle 11.5 ms, and a stop bit is transmitted every 110 ms as long as the key remains pressed. Note that the preamble duty cycle of the repeat pattern is shorter than the preamble of the first command and data frame. See Figure 3 below for an illustration of the repeat sequence.

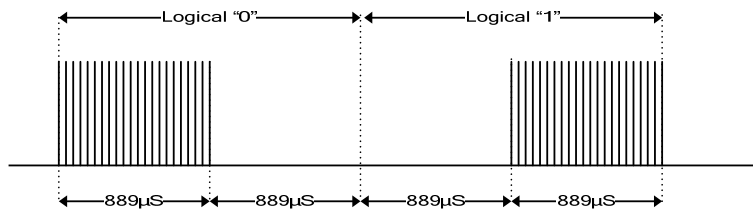


**Figure 3 NEC Repeat Sequence**

### 3.3 RC5 Format

#### 3.3.1 Modulation

The RC5 format uses the Manchester (bi-phase) modulation technique. Manchester modulation is based on keeping the pulse active period and duty cycle constant while positioning the pulse at the beginning or the end of the duty cycle to distinguish between a logical "1" and "0". Figure 4 below illustrates the principle of Manchester modulation.



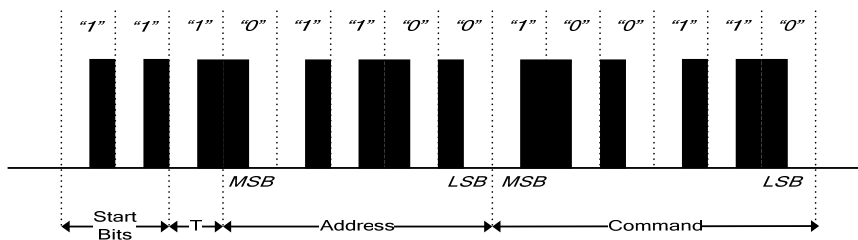
**Figure 4 RC5 Format - Manchester (Bi-phase) Modulation**

RC5 format timing information:

- Carrier: 36 kHz with 1/3 or 1/4 duty cycle
- Active period: 889 μs
- Duty Cycle: 2 \* Active Period: 1.778 ms
  - Logical "0": Active burst first half of duty cycle
  - Logical "1": Active burst in second half of duty cycle

### 3.3.2 Protocol

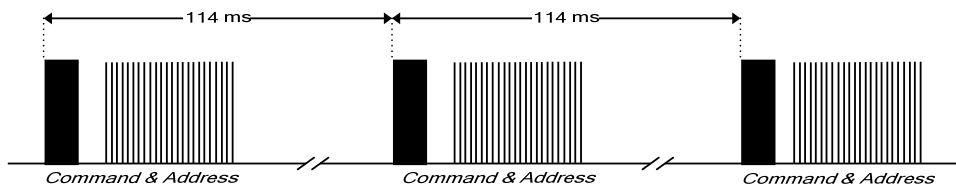
The RC5 protocol uses a 6-bit command and a 7-bit address length for each transfer. Other versions with different command and address length also exist. The RC5 protocol is not using a preamble; instead two start bits of logical "1" are used to identify the start of a frame. The third bit is a toggle bit that is inverted every time a key is pressed. This way the receiver can distinguish between a key pressed command and repeated commands. The command and data bits are transferred with the MSB first. See Figure 5 below for an illustration of the protocol.



**Figure 5 RC5 Protocol**

### 3.3.3 Repeat Sequence

The protocol described in Figure 5 is also used as the repeat pattern. This means initial frame and repeat frames are identical. The frame is repeated every 114 ms as long as the key remains pressed. See Figure 6 for an illustration of the repeat sequence.

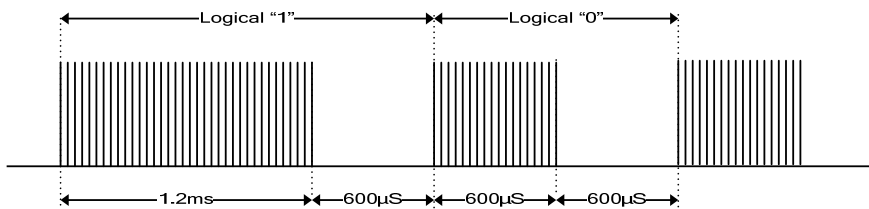


**Figure 6 RC5 Repeat Sequence**

### 3.4 SIRC Format

#### 3.4.1 Modulation

The SIRC format uses a combination of the pulse distance and pulse width modulation technique. SIRC modulation is based on varying both the active period and duty cycle to distinguish between a logical “1” and a logical “0”. Note that the non-active period for both logical “1” and logical “0” is constant. Figure 7 below illustrates the principle of a combined pulse distance and pulse width modulation.



**Figure 7 SIRC format - Pulse Distance and Pulse Width Modulation**

SIRC format timing information:

- Carrier: 40 kHz with 1/3 or 1/4 duty cycle
- Active period:
  - Logical “0”: 600  $\mu$ S
  - Logical “1”: 1.2 ms
- Duty Cycle
  - Logical “0”: Active Period Logical “0” + 600  $\mu$ S: 1.8 ms
  - Logical “1”: Active Period Logical “1” + 600  $\mu$ S: 1.2 ms

### 3.4.2 Protocol

The SIRC protocol uses a 7-bit command and a 5-bit address length for each transfer. Other versions with different command and address length also exist. The command and address bits are preceded by a preamble with active period of 2.4 ms and duty cycle of 3 ms. The command and data bits are transferred with LSB first. See Figure 8 below for an illustration of the protocol.

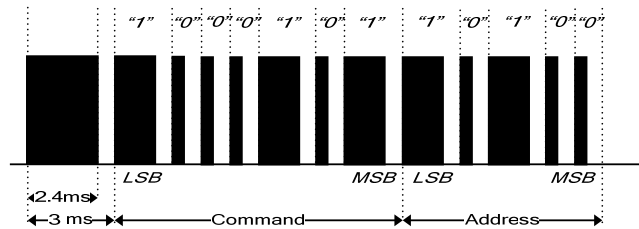


Figure 8 SIRC Protocol

### 3.4.3 Repeat Sequence

The protocol described in Figure 8 is also used as the repeat pattern. This means initial frame and repeat frames are identical. The frame is repeated every 45 ms as long as the key remains pressed. See Figure 9 for an illustration of the repeat sequence.

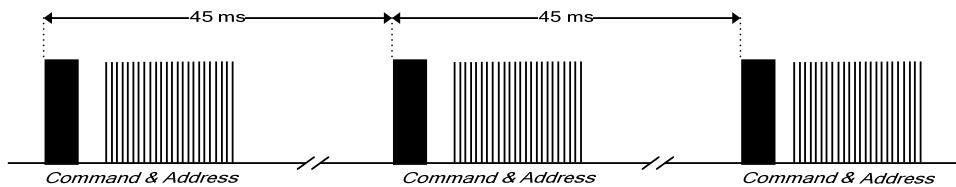


Figure 9 SIRC Protocol Repeat Sequence

## 4 IR signal generation with CC253X

The CC253x family of devices contains hardware resources that enable generation of IR signals with minimal CPU interaction. The following resources are available;

- Timers



- Timer 1 (16 bit)
- Timer 3 (8 bit)
- Timer 4 (8 bit)
- DMA
  - Multiple DMA channels for transfer of IR signal timing data to the timers
- IR generation AND circuit
  - Logical AND circuit used to combine two timer outputs to generate a modulated IR signal. Note that only Timer 3 and Timer 1 can be used for this purpose

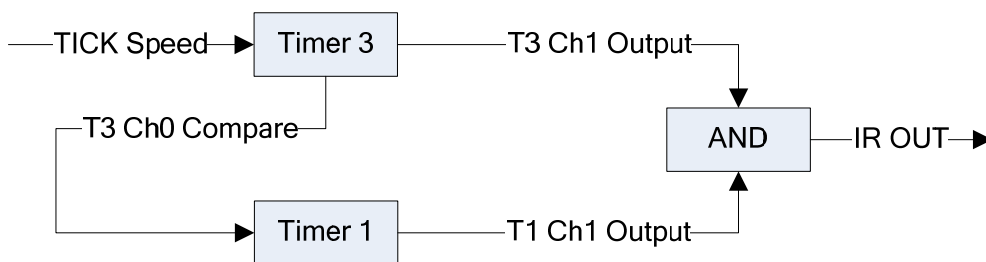
Note that Timer 2 (MAC timer) isn't available for this purpose since it's reserved for the RemoTI system.

#### 4.1 Non-modulated Signals

Non-modulated signals can be generated using either Timer 1 (T1), Timer 3 (T3) or Timer 4 (T4) together with DMA channels for minimal CPU interaction. Which timer to use depends on the timing specification of the IR signal and the output pin requested for the generated signal. See [2] for details of output pin assignments for the different timer channels.

#### 4.2 Modulated Signals

Modulated signals are generated using both Timer 1 (T1) and Timer 3 (T3). T1 is used to modulate the IR signal on top of the carrier generated by T3. Note that only Timer 1 channel 1 output and T3 channel 1 output can be combined with the logical AND circuit to generate a modulated IR signal. The IR OUT pin is controlled by the T1 channel 1 output pin and is as such limited to P1.1 or P0.3. See the peripheral I/O section of [2] for details. P1.1 has 20 mA drive strength while P0.3 has 4 mA drive strength. Figure 10 below illustrates the logic for generation of modulated IR signals.



**Figure 10 CC253x IR Generation HW for Modulated Signals**

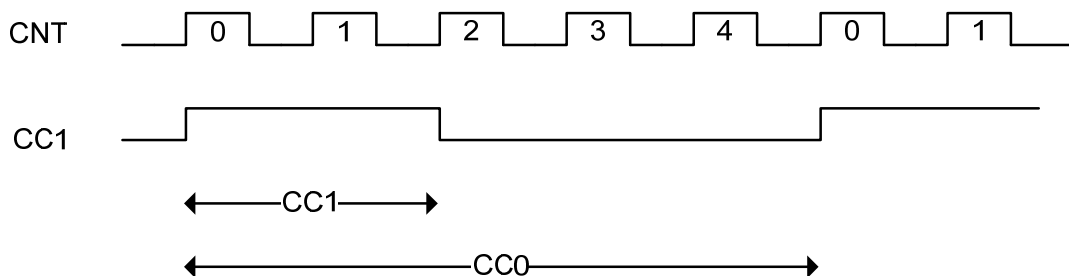
NOTE that the IR OUT is active high. This means that external circuitry for increased drive strength must be designed with active high logic.

### 4.3 Timer and DMA Interaction Examples

The modulo mode and output compare mode feature of Timer 1 (T1), Timer 3 (T3) and Timer 4 (T4) are used to the control pulse generation comprising the IR signal. These features are described in details in the chapter for each timer in [2]; however, here is a short description of these important features.

- **Timer modulo mode**  
Timers can be configured as free running, up/down or modulo mode. The modulo mode basically configures the timer to count upwards from 0x0 to the value configured in the timer channel 0 compare register. The timer wraps around to 0x0 again when the timer channel 0 compare register value is reached. This feature is used to control the duty cycle of each pulse in the IR signal pattern.
- **Timer output compare mode**  
Timer channel 1-n (n dependent on timer) is associated with an output pin in output compare mode. The output on this pin is controlled by the selected output compare mode and current timer value. This application note and sample code is using output compare mode 4; the pin is set when timer counter is 0x0 and cleared when the timer counter value equals the timer channel 1-n compare value. This feature is used to control the active period of each pulse in the IR signal pattern.

An example is shown in Figure 11 where the timer channel 0 compare (CC0) is set to 4 and timer channel 1 output compare (CC1) is set to 2. The timer is furthermore configured to run in modulo and compare mode 4.



**Figure 11 Timer Modulo and Compare Mode 4**

It can be seen from Figure 11 that the pulse on Timer Channel 1 (CC1) is set when the timer counter (CNT) = 0x0 and cleared when it the CNT = CC1. The CNT also wraps around and starts counting upwards from 0x0 when CNT = CC0.

It is important to note the effect of the 0<sup>th</sup> counter cycle on the generated signal. One may expect a 50% duty cycle when CC1 is configured to CC0 /2, however, the generated signal duty cycle is actually  $CC1 / (CC0 + 1)$ . It is therefore important to configure the CC0 value with the 0<sup>th</sup> counter cycle in mind for correct timing.

The timer CC0 and CC1 values can be programmed manually or by using dedicated DMA channels. DMA channels are used to avoid CPU interaction from the time the signal

generation is started until an interrupt is generated at the end of the complete IR signal generation. The DMA channels are configured to feed the CC0 and CC1 register from a buffer in RAM with the timing information for each pulse. The RAM buffers are configured depending on the IR generation signal format timing and the address and data information for the command or repeat sequence.

The DMA channels are furthermore configured to trigger on the CC1 value of the timer. This means the next CC0 and CC1 value is transferred from RAM to the respective timer CC0 and CC1 registers when the timer CNT = current CC1 value. It is important to notice that these new DMA'd CC0 and CC1 values are not latched into the timer until the timer CNT = 0x0.

The DMA is configured to operate in variable length mode and the length, i.e. the number of CC0 and CC1 values to be transferred, is set for each IR command depending on the signal pattern. The DMA will generate an interrupt immediately after the last value is DMA'd from RAM to the timer CC0 and CC1 register. In order to ensure generation of the last pulse, a last value in the RAM buffers are included as don't care. Basically, the ISR will be called and the timers will be stopped after the last DMA. As such, the timing information of the last value in the RAM buffers will never be generated.

### 4.3.1 Pulse Distance Encoding

Figure 12 below illustrates the sequence of events for the timer and DMA channels for pulse distance encoding

- CNT shows the timer counter values
- The mid section shows the DMA's trigger when  $CNT=CC1$  and the DMA transfer from buffer a and b to the CC0 and CC1 timer registers respectively
- The latch arrow shows the point in time when the new CC0 and CC1 values are latched into the timers
- IR OUT is the generated signal

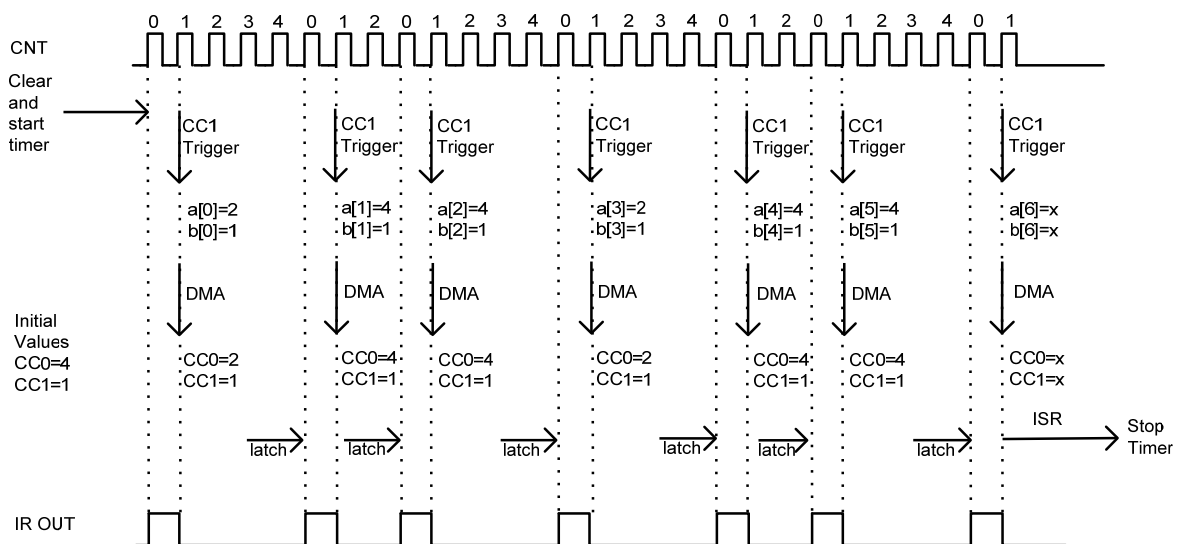


Figure 12 Pulse Distance Encoding: DMA and Timer Details

As seen from Figure 12, the CCO and CC1 register must be programmed with initial values to control the timing of the first pulse. The subsequent pulses are controlled with the timing information DMA'd from the RAM buffers.

This illustration uses one DMA channel each for the CCO and CC1 timing information. It can be observed that the CC1 value is constant. This is expected for pulse distance encoding where the pulse active period is constant while the pulse duty cycle period varies to distinguish between a logical "0" and "1". As such, only one DMA channel is really necessary for pulse distance coding formats since CC1 doesn't need to be re-programmed. Note, however, that IR coding formats that include a preamble must use a DMA channel for the CC1 timing information as well due to different active period timing of the preamble and the individual pulse. This is in fact the case for the NEC format described and implemented in the sample code for this application note.

### 4.3.2 Pulse Width Encoding

Figure 13 below illustrates the sequence of events for the timer and DMA channels for pulse distance encoding

- CNT shows the timer counter values
- The mid section shows the DMA's trigger when  $CNT=CC1$  and the DMA transfer from buffer a and b to the CCO and CC1 timer registers respectively
- The latch arrow shows the point in time when the new CC0 and CC1 values are latched into the timers
- IR OUT is the generated signal

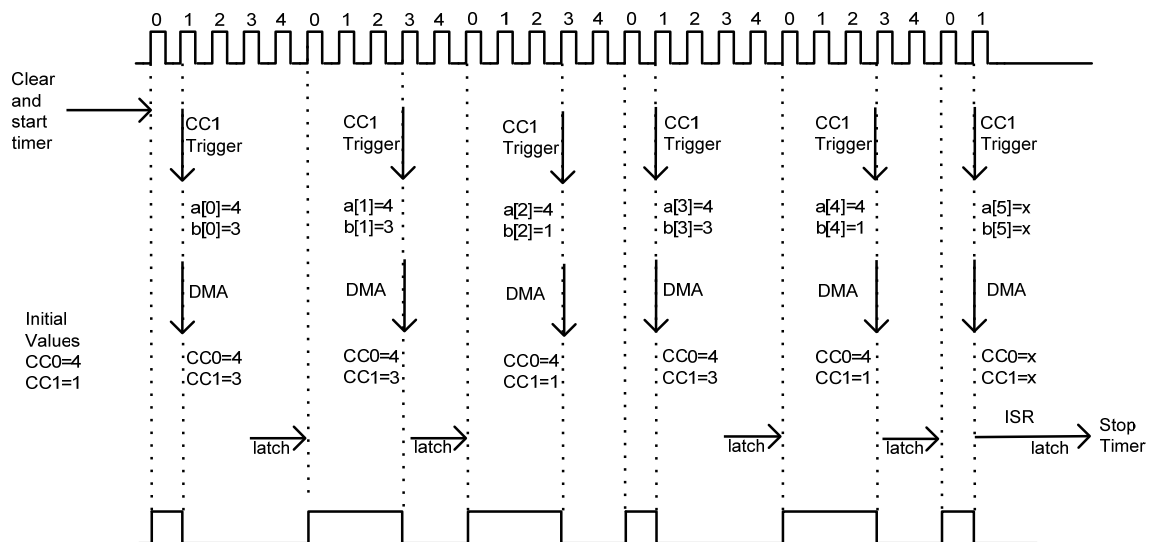


Figure 13 Pulse Width Encoding: DMA and Timer Details

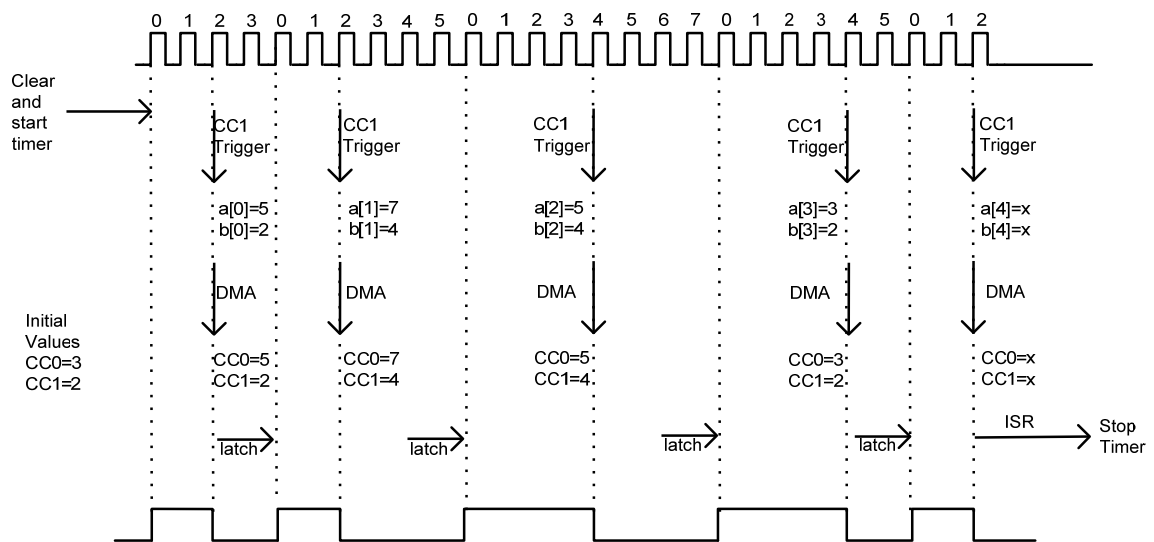
As seen from Figure 13, the CCO and CC1 register must be programmed with initial values to control the timing of the first pulse. The subsequent pulses are controlled with the timing information DMA'd from the RAM buffers.

This illustration uses one DMA channel each for the CCO and CC1 timing information. It can be observed that the CC0 value is constant. This is expected for pulse width encoding where the pulse duty cycle period is constant while the pulse active period varies to distinguish between a logical "0" and "1". As such, only one DMA channel is really necessary for pulse distance coding formats since CC0 doesn't need to be re-programmed. Note, however, that IR coding formats that include a preamble must use a DMA channel for the CC0 timing information as well due to different active period timing of the preamble and the individual pulse.

### 4.3.3 Manchester Encoding

Figure 14 below illustrates the sequence of events for the timer and DMA channels for pulse distance encoding

- CNT shows the timer counter values
- The mid section shows the DMAs trigger when CNT=CC1 and the DMA transfer from buffer a and b to the CCO and CC1 timer registers respectively
- The latch arrow shows the point in time when the new CC0 and CC1 values are latched into the timers
- IR OUT is the generated signal



**Figure 14 Manchester Encoding: DMA and Timer Details**

As seen from Figure 14, the CCO and CC1 register must be programmed with initial values to control the timing of the first pulse. The subsequent pulses are controlled with the timing information DMA'd from the RAM buffers.

This illustration uses one DMA channel each for the CCO and CC1 timing information. It can be observed that the neither CC0 nor CC1 values are constant as with pulse distance or pulse width encoding. The values of CC0 and CC1 varies dependent on the sequence of logical "0's and logical "1"s to be transmitted.

#### 4.3.4 Start Condition

It's important that the output of the selection IR generation pin is initialized correctly at application startup. This is accomplished by running the selected timer at IR generation module initialization with selected CC0 and CC1 values, and halting the timer when the pin is known to be in its desired state based on the timer counter value.

## 5 IrGenApp

The application code accompanying this application note contains example implementation of the NEC, RC5 and SIRC IR formats running on the CC2533F96 device. Note that the IR generation drivers for the different formats can run on all CC253x devices.

Unzip the application code on top of your RemoTI 1.2.1 Installation. The default <install directory> is C:\Texas Instruments\RemoTI-CC253xDK-1.2.1.

The application is using the RemoTI Target Board for as the IR generation platform. It will generate IR signals dependent on the RF4CE command received over-the-air.

### 5.1 IAR Workspace

The IrGenApp application can be found in <install directory>\Projects\RemoTI\IrGenApp. Open the IrGenApp.eww workspace in the CC2533RB directory. You will see the workspace includes the following project configurations:

- CC2533F96 SIRC
- CC2533F96 NEC
- CC2533F96 RC5

### 5.2 IR Generation Driver

Each of the IR drivers are contained in the following files

- hal\_irgen\_SIRC.h/c
- hal\_irgen\_NEC.h/c
- hal\_irgen\_RC5.h/c

Each IR generation driver consists of four main modules

1. Initialization

This function is used to initialize the timers and DMAs according to the IR format bit timing information, select output pin and also initialize the output pin to inactive state. This function is called by the application at system initialization time.

2. Command generation

This function prepares the RAM buffers based on the actual command and actually starts the IR generation. This function is called by the application layer when IR generation is requested.

3. Repeat command generation

This function is used to generate the repeat command. This function is called from the application layer, which means the repeat timing must be controller at the application layer.

#### 4. Interrupt Service Routine (ISR)

This is the entry point of the for the IR generation module when the signal generation is complete.

The driver also contains the calculation of the bit timing at the top of the respective .c file.

A common file called hal\_irgen.h contains definitions for DMA channel selection, generic definitions for timers and DMAs used to configure the appropriate resources.

### 5.3 IR Generation Application

The application code examples for using the IR generation drivers are contained in the following files

- irg\_target\_SIRC.c
- irg\_target\_NEC.c
- irg\_target\_RC5.c

The application calls the IR generation initialization module, generates the appropriate IR command based on the RF4CE message received over-the-air, and controls the generation of the repeat sequence.

### 5.4 Buttons and LEDs

The S2 button on the Target Board is used as input to trigger discovery/pairing.

Two LEDs are used as visual indication of RemoTI initialization, discovery/pairing and IR generation.

- Green LED (LED1) is used to indicate message exchange.
  - Off – no valid pairing in the node paring table
  - On – at least one pairing entry exist in the node paring table
  - Blinking - indicates the node is in discovery mode and will accept a discovery/pairing request from a remote controller node. The target node implements the auto-discovery pairing mechanism and will as such accept pairing request for 30 sec after S2 is activated.
- Red LED (LED2) is used to indicate RemoTI initialization and IR signal generation.
  - On - when IrGenApp is initializing and during IR signal generation.
  - Off – when in ready state

### 5.5 Execution Sequence

Follow these steps to run the sample application:

1. Connect the mini USB cable to the Target Board to apply power.
2. Connect the CC debugger to the target Board.
3. Build and download the application
4. Start the execution of the IrGenApp and observe the green LED turned on.
5. Wait until the green LED is turned off to indicate that RemoTI stack has initialized.
6. Press S1 to enable discovery/pairing mode and observe the green LED blinking.
7. Press the pairing button on the remote controller when the green LED is blinking.
8. The green LED will turn on solid when the pairing link is established.
9. Press the 'play' key on the remote controller to start IR generation and observe the red LED blink when IR signal generation is in progress. Note that other keys pressed on the remote controller have no effect.

## 6 Target Board

Earlier versions of the RemoTI Target board included an external active low IR driver circuit for the IR\_OUT (P1.1) pin. See chapter 6.1.7.1 of [4] for more information for how to change the polarity to active high.



## 7 References

- [1] <http://www.sbprojects.com/knowledge/ir/ir.htm>
- [2] CC253x User's Guide, SWRU191 ([www.ti.com/lit/swru191](http://www.ti.com/lit/swru191))
- [3] <http://focus.ti.com/docs/prod/folders/print/cc2530.html>
- [4] CC2533 RF4CE Basic Remote Development Kit Hardware User's Guide, SWRU266 ([www.ti.com/lit/swru266](http://www.ti.com/lit/swru266))

## 8 General Information

### 8.1 Document History

Revision	Date	Description/Changes
SWRA323	June 30, 2011	Initial release.

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Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
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