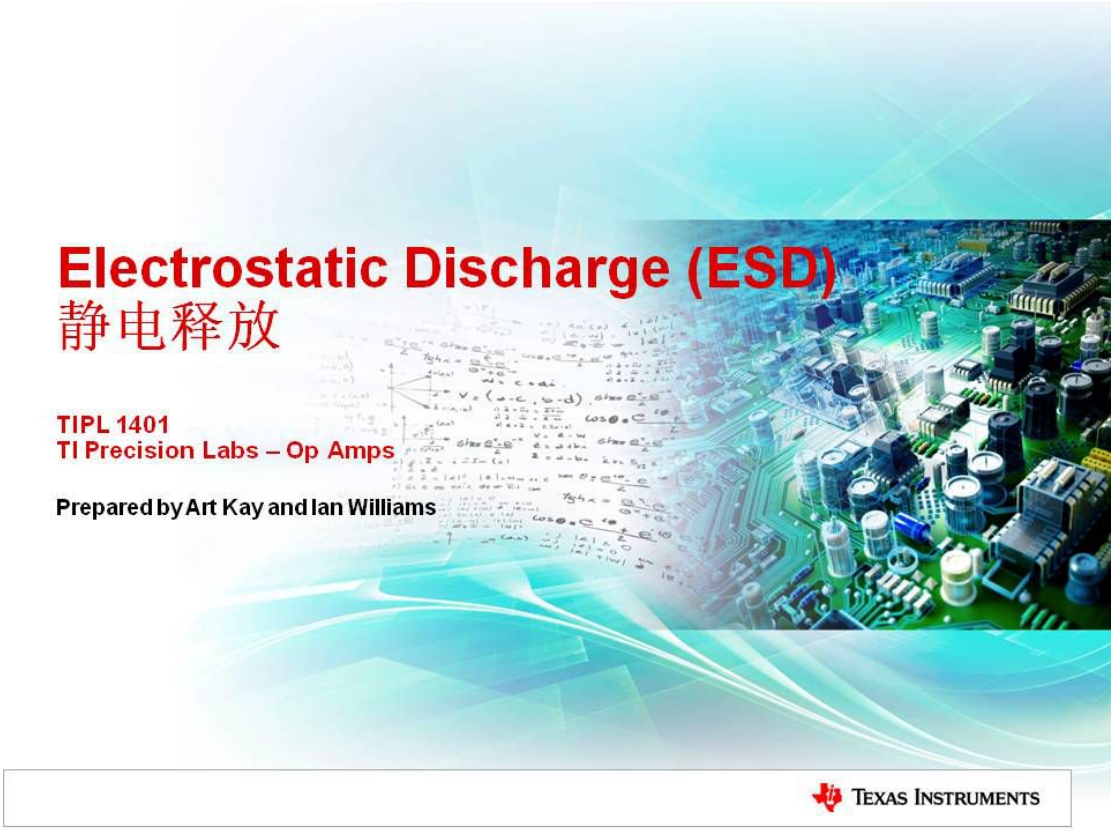
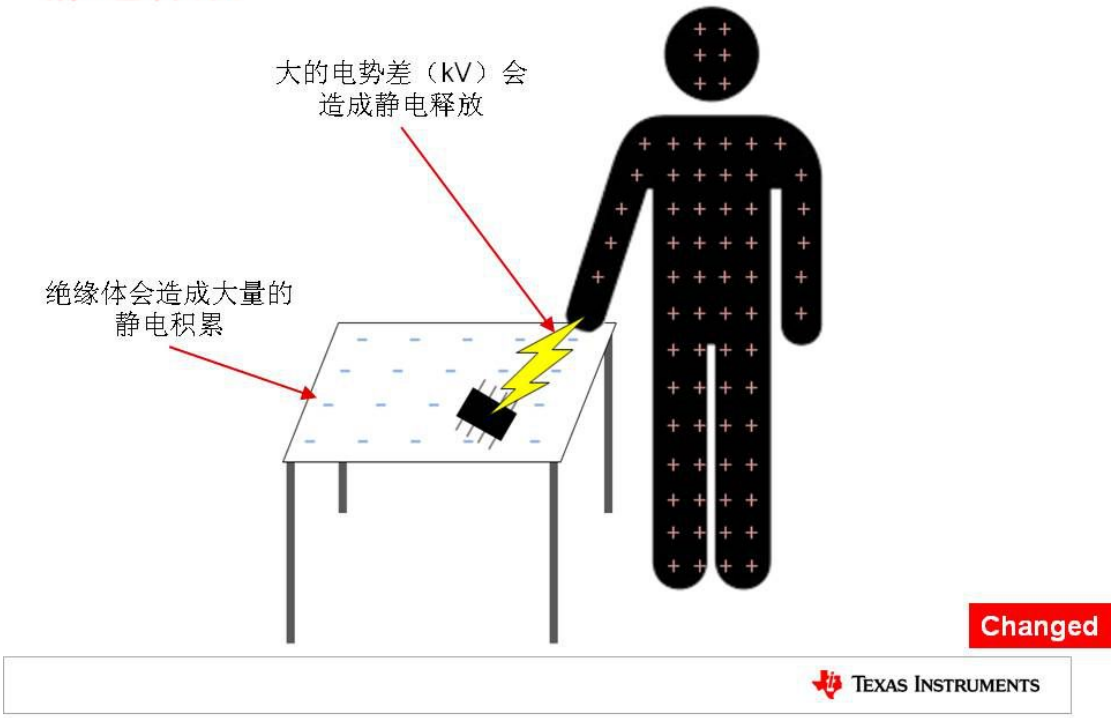


- Hello, and welcome to the video for the TI Precision Lab discussing electrostatic discharge, or ESD. In this video we'll explain how ESD can damage semiconductor components. We will also give detail on internal ESD protection circuits that are included in semiconductor devices. Finally, we will explain how ESD performance is characterized so that the robustness of the device is understood.

- 大家好，欢迎来到 TI Precision Labs（德州仪器高精度实验室），讨论关于 electrostatic discharge（ESD）静电释放的话题。本节视频将介绍 ESD 是如何损坏半导体元器件的，并且详细介绍半导体器件中的 ESD 保护电路的设计。最后，我们将介绍 ESD 性能指标是如何测定的，以帮助更好地理解器件的 ESD 性能。

Electrostatic Discharge (ESD)
静电释放



- Many common items can develop a static electrical charge. Insulators are especially prone to developing large static charges. Some materials tend to become positively charged and others become negatively charged. Whenever two items with a charge imbalance are brought in close proximity, you can have a sudden flow of electricity between the two objects, called an electrostatic discharge, ESD. ESD can show up as a visible spark and often has voltage levels in the thousands of volts. From a semiconductor perspective, ESD is the most common way that devices are damaged.

- 很多常见的物体会积累静电。特别是绝缘体很容易积累大量的静电。一些物体倾向于带正电，另外一些物体倾向于带负电。当两个电荷不同的物体靠到一起的时候，两个物体之间会产生一个瞬时电流，称为 ESD（静电释放）。ESD 电压经常能达到几千伏，产生可见的电火花。对于半导体器件来说，ESD 是最常见的损坏原因。

ESD Generation vs. Relative Humidity (RH)
ESD的发生和相对湿度的关系

Means of Generation	10-25% RH	65-90% RH
Walking across carpet	35,000V	1,500V
Walking across vinyl tile	12,000V	250V
Worker at bench	6,000V	100V
Poly bag picked up from bench	20,000V	1,200V
Chair with urethane foam	18,000V	1,500V

Source: ESD Association

ESD Generation vs. Human Awareness
人体对ESD现象的感知

Discharge	Awareness
>3500V	Feel
>5000V	Hear
>8000V	See

一些芯片在<10V的时候就会损坏，
这个时候你根本感觉不到ESD

Source: http://emp.byui.edu/fisherr/esd/esd_control_handbook.pdf

- The table at the top of this slide lists some materials that generate significant static charges. Also notice that the static charge is dependent on the relative humidity. Lower relative humidity generates more static charge.
  The table at the bottom of the slide shows ESD discharge voltages vs. human awareness. Notice that when you can see an ESD “spark” the voltage is very large, at 8000V or more.

- 上面的这个表格罗列了一些生活中常见动作所产生的静电电压。注意到，静电电压和相对湿度有关。相对湿度低的时候，产生的静电电压更高。
  下面的表格展示了人体对静电放电的感受程度。注意到，当你看到电火花的时候，静电电压已经很高，在 8kV 及以上。

Typical IC Device Sensitivity Thresholds
IC器件典型的损坏电压阈值

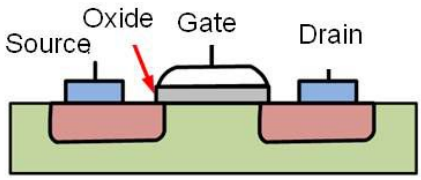
Device Type	Threshold Susceptivity (V)
MOSFET	10-100
VMOS	30-1800
NMOS	60-100
GaAsFET	60-2000
EPROM	100+
CMOS	200-3000
JFET	140-7000
SAW	150-500
Op-AMP	190-2500
Schottky Diodes	300-2500
Film Resistors	300-3000
Bipolar Resistors	300-7000
ECL	500+
SCR	500-1000
Schottky TTL	500-2500

Source: http://emp.byui.edu/fisherr/esd/esd_control_handbook.pdf

- Different device types are susceptible to different levels of ESD voltage. Some devices, such as MOSFETs, are susceptible at very low voltages. We will see later that ESD protection circuits are used inside most semiconductor devices to enhance ESD robustness. The ESD robustness of a MOSFET can be improved from only ten volts to thousands of volts with additional ESD protection circuits.

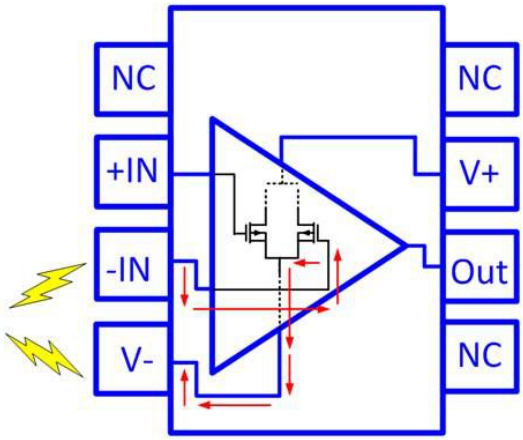
- 不同类型的器件对 ESD 的耐压值也不一样。一些器件，比如 MOS 管，在很低的电压时就会损坏。后面我们将会看到，大部分的芯片中采用的 ESD 保护电路能够提升器件的 ESD 性能。在添加了 ESD 保护电路以后，MOS 器件的 ESD 耐压值可以从 10V 提升到几千伏。

ESD Can Damage Semiconductors
ESD会损坏半导体器件



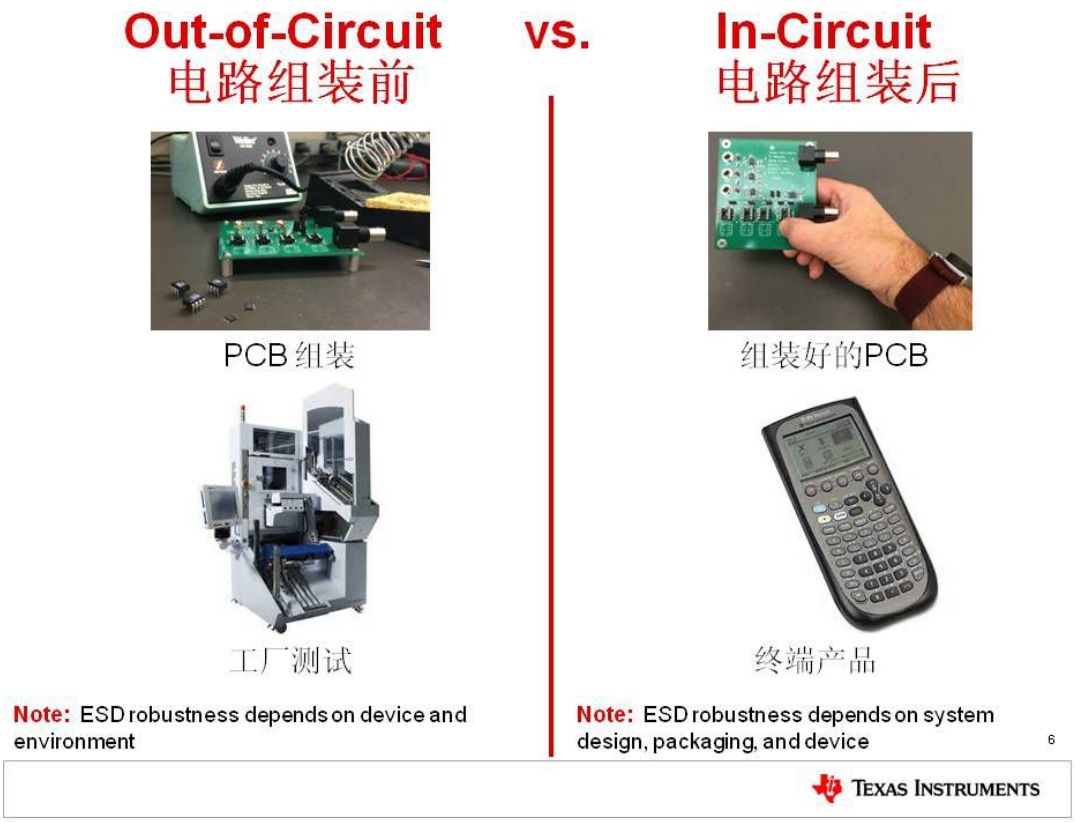
栅氧化层非常薄(nm)

ESD脉冲会击穿栅氧化层和其他结构



- Let's look more closely at the typical way in which semiconductor devices are damaged by ESD. Consider a large ESD potential, or voltage, which is applied between the inverting input and negative supply pin of an op amp. This places a large voltage from the gate to the source of one of the input MOSFETs, which can cause damage to the device. Keep in mind that the thickness of the MOSFET gate oxide may only be a few nanometers, making it very susceptible to this kind of damage.

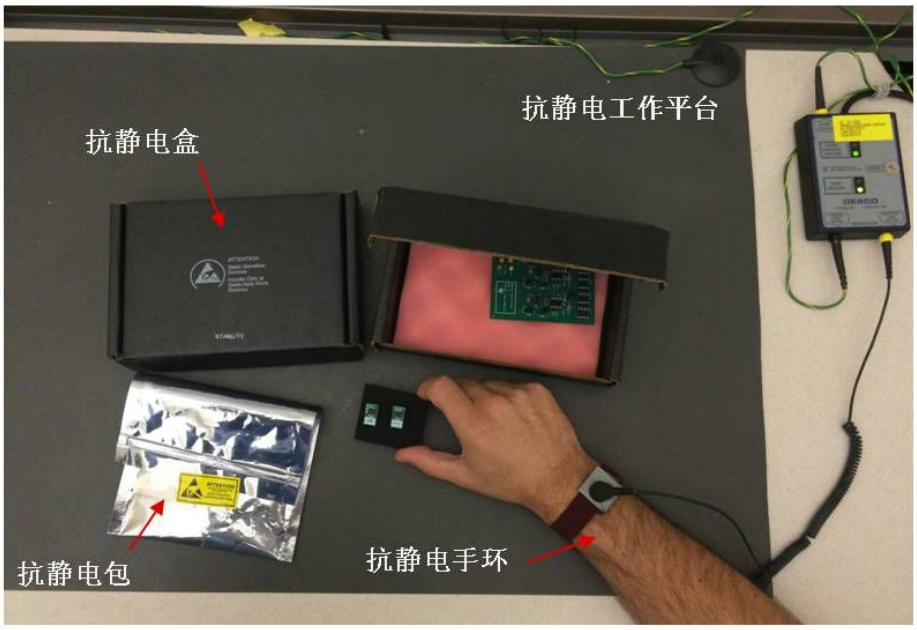
- 我们来详细的观察一下，ESD 是怎样损坏半导体器件的。假如，当一个幅值很高的静电或者电压加到运放的反相端和负电源端；这就会在输入 MOS 管的栅极和源极之间产生一个很高的电压，这个电压会击穿栅氧化层，损坏器件。值得注意的是，MOS 管栅极氧化层的厚度通常只有几个 nm，在这种电压下非常容易损坏。



- There are two main categories of ESD events for semiconductor devices. An "out of circuit" ESD event can occur to a loose device; that is, a device before it is soldered to a printed circuit board. Out of circuit events can happen during manufacturing, factory test, or the assembly process. In general, factory test and manufacturing processes are designed to minimize exposure to ESD.
  An "in-circuit" ESD event refers to damage caused on a fully assembled PCB, or end product. In this case the product packaging, product design, and the device's own robustness determine the ESD susceptibility of the product.
  The ESD protection circuits that are included in the device are intended to protect against **out-of-circuit** events.

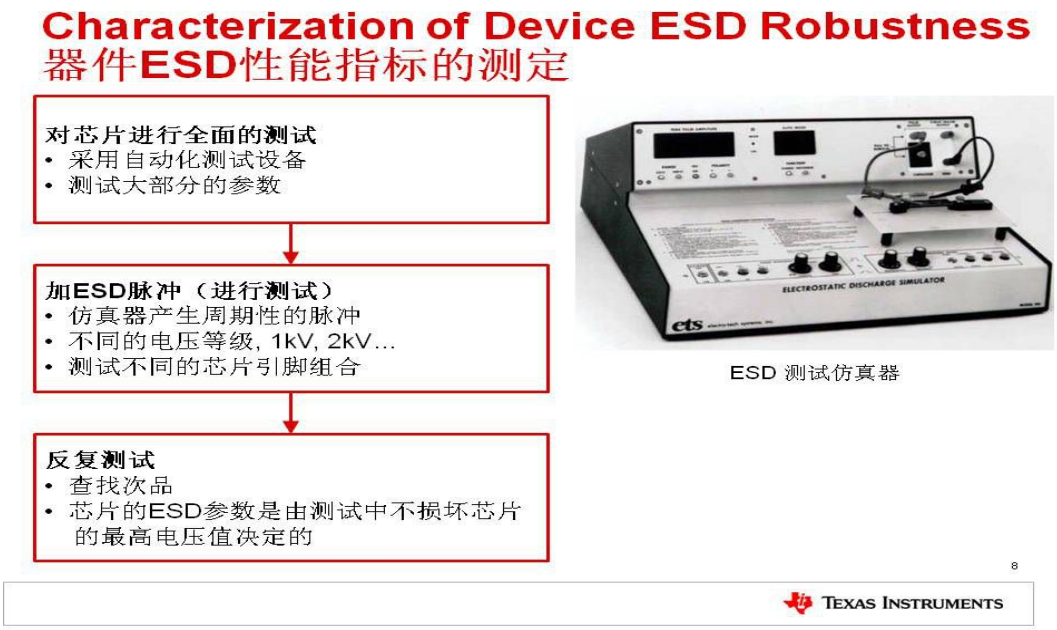
- 针对 ESD 事件，有两种主要的分类方法。在电路组装前，即芯片未焊接到 PCB 上之前，ESD 会造成器件损坏。这些可能发生在生产，工厂测试和组装的过程中。一般来说，工厂测试和生产工艺在设计的时候，就考虑到最小化 ESD 的发生。
  电路组装后的 ESD 指的是在一个组装好的 PCB 或者终端产品上，发生的 ESD 事件。这种情况下，产品的包装，设计以及器件本身的抗 ESD 性能，决定了产品的 ESD 特性。
  器件内部的 ESD 保护电路是为了防止器件在**电路组装前**的 ESD 损坏。

ESD Handling and Protection
ESD 处理和保护

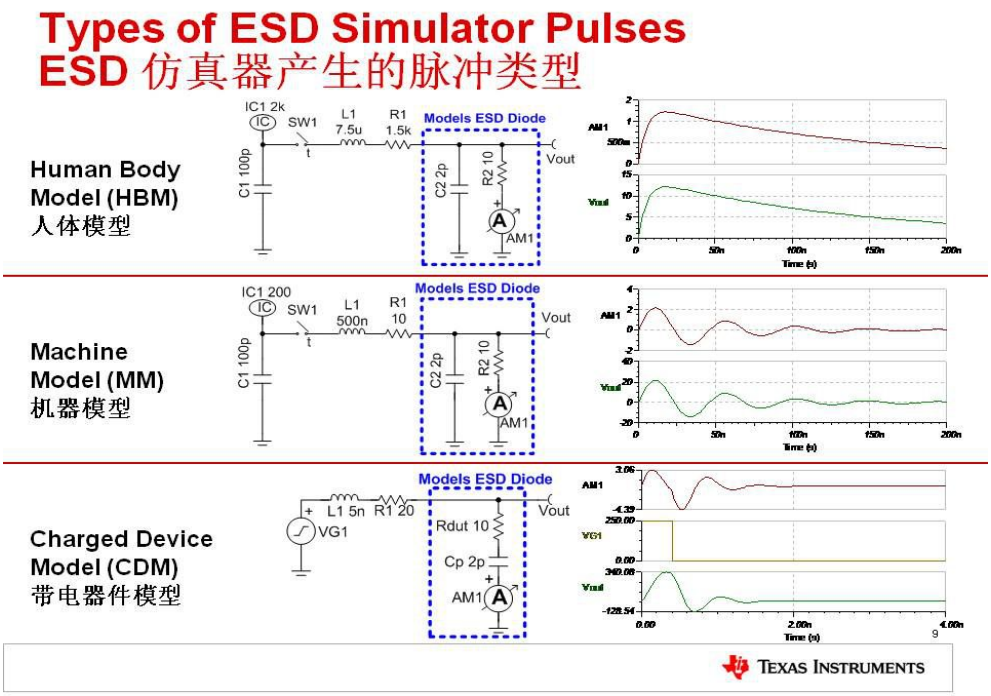


- There are some general precautions that can be followed to minimize ESD damage to devices and assembled products. In general, these precautions use resistive materials to dissipate charge. For example, the anti-static wrist strap shown in the picture allows a controlled discharge of static electricity to ground. Typically the impedance of antistatic materials is in the mega ohms. Note that the anti-static bag, box, and work surface also contain resistive materials that are intended to slowly neutralize charge.

- 我们可以采取一些基本的预防措施来最小化 ESD 对器件和产品的损坏。一般来说，这些预防措施采用电阻性材料来释放静电。比如，图中所示的抗静电手环能够让人体上的静电，可控地释放到大地上。这些抗静电材料的阻值一般在兆欧级别。值得注意的是，图中所示的抗静电包装，抗静电盒以及抗静电工作平台，同样都包含了电阻性材料，能够缓慢地释放静电。



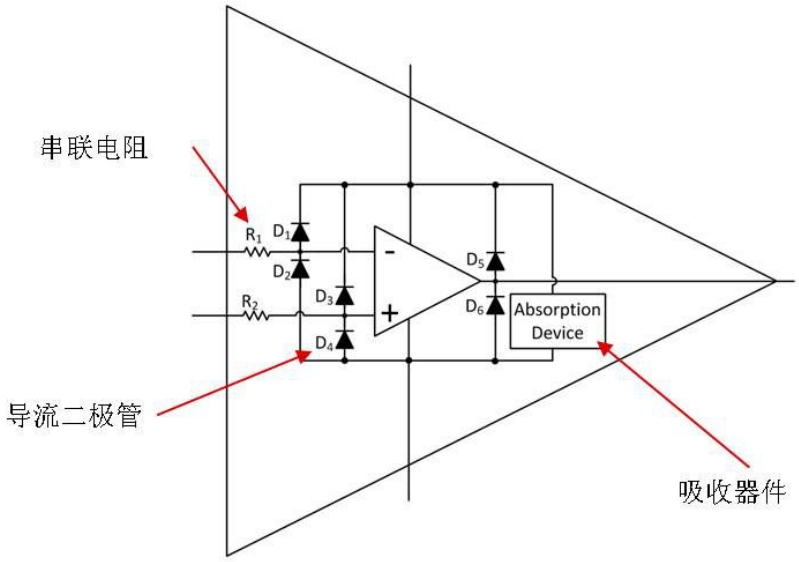
- During the initial development of a semiconductor product the ESD robustness is characterized. First, a statistically significant sample of devices is fully tested using automatic test equipment. Generally, most of the data sheet parameters are measured during this automated test.
  Second, a specialized ESD test system is used to apply a simulated ESD pulse to the device. The specific characteristics of the ESD pulse are controlled by the test hardware. For example, the amplitude and ESD model can be selected. Various ESD models will be discussed later, but in short the ESD model sets the capacitance, inductance and charge of the ESD pulse to simulate a real world ESD event. During the test the ESD pulse is applied to many different combinations of device pins for a significant sample of devices. Also, different levels of ESD pulses are applied to the device; for example, 1kV, 2kV, 3kV, and so on.
  Finally, the comprehensive test is repeated on the devices. The ESD rating of the device is determined by the highest ESD level that all devices in the sample pass. This ESD rating is listed in the absolute maximum rating table of the data sheet.
- 在半导体器件最初的生产过程中，芯片的 ESD 防护性能（参数）就已经确定了。首先，大量的芯片样片经过自动化测试。一般来说，芯片数据手册上的大部分参数都是在这个自动化测试中，测量出来的。
  然后，一个专门的 ESD 测试系统对器件进行 ESD 脉冲仿真测试。这个 ESD 脉冲的参数是由测试硬件控制的。比如，我们可以选择脉冲的幅度和 ESD 模型。我们将在后文中讨论多种不同的 ESD 模型。简要来说，ESD 模型通过设置电容，电感和 ESD 电流等参数来模拟现实中的 ESD 现象。在测试过程中，ESD 脉冲加到芯片的多个引脚和引脚的不同组合上。同样的，我们采用不同级别的 ESD 脉冲对芯片进行测试，比如 1kV，2kV，3kV 等。
  最后，根据这个复杂的 ESD 测试流程，对芯片进行反复测试。芯片的 ESD 等级是由这一批样片均能通过测试的最高值决定的。这个数值就是芯片数据手册上的 ESD 绝对最高值。



- 3 different models are used to generate controlled ESD pulses. The “Human Body Model,” or HBM, is first and the most common model developed for ESD emulation. This model attempts to emulate the ESD discharge that could occur when a human touches an microelectronic device. Typical HBM voltage levels range from 1kV to 5kV.
  The “Machine Model,” or MM, is also called the zero ohm model because it simulates a very low impedance discharge of static charge to ground. The MM is meant to simulate a static discharge in a metal handler or automatic assembly equipment. The Machine Model has in most cases been replaced by the Charged Device Model.
  The “Charged Device Model,” or CDM, is designed to accurately simulate the test and assembly environment, for example, the static charge developed when a device slides down shipping tubes. CDM voltages are typically in the hundreds to thousands of volts. CDM currents are higher than HBM currents because the current limiting resistance is much smaller.

- 我们采用 3 种不同的模型来产生 ESD 脉冲。人体模型是 ESD 测试中最常用的的模型。这个模型是用来模拟当人体碰触到芯片时产生的 ESD。典型的人体模型电压值范围从 1kV 到 5kV。
  机器模型也被称作零欧姆模型，因为它是用来仿真一个阻抗非常低的 ESD 到地的释放情形。机器模型是用来仿真金属臂或者自动化组装设备的 ESD。大部分情况下，机器模型都被带电器件模型所替代了。
  带电器件模型用来精确仿真测试环境和组装环境中的 ESD。比如，当器件从传送管道上滑下时，会产生静电积累。带电模型的典型电压值从几百伏到几千伏。带电器件模型的电流比人体模型的电流高很多，因为带电器件模型的限流电阻很小。

ESD Protection Inside an IC
芯片内部的ESD保护

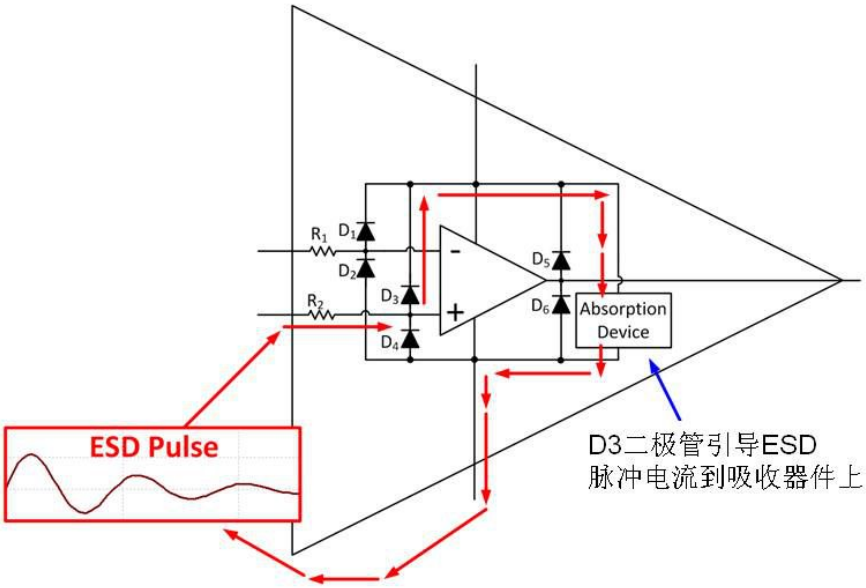


- Here we illustrate the ESD protection circuits commonly used on semiconductor devices. In this case an op-amp is shown, but similar ESD protection is used on other types of devices.
  Remember that this type of ESD protection is intended to protect the device from an “out of circuit” ESD event. In other words, these structures are intended to protect the device during the test, assembly, and manufacturing process. They are also effective for ESD protection in unpowered systems, but they may actually cause issues such as latch-up in powered systems. The video series on electrical overstress will cover this topic in much more detail.
  Three common structures used in ESD protection are the series resistance, steering diodes, and absorption device. The steering diodes turn on and direct the ESD pulse away from the sensitive circuit elements to the absorption device. The absorption device absorbs the energy of the ESD pulse and limits the voltage level to prevent damage. The series resistance limits the input or output current. Note that a larger series resistance offers more protection but often degrades other key parameters such as noise or maximum output current. This practical limitation on resistance may affect the ESD robustness of some devices.

- 这部分我们介绍一下芯片内部常用的 ESD 保护设计。这里，我们采用运放作为示例，其他器件中采用的 ESD 保护也是类似的。
  注意一下，这里的 ESD 保护是用来保护器件还未组装到电路中的 ESD 情形。也就是说，这些结构是用来防护器件在测试、组装和加工过程的 ESD 现象。在未上电的系统中，这些 ESD 保护同样有效。但是在上电系统中，它们也可

能造成闩锁效应。这一点，我们将在有关芯片过压的视频中做详细介绍。
芯片内部中一般有 3 种 ESD 保护结构，分别是：串联电阻，导流二极管和吸收器件。导流二极管引导 ESD 脉冲电流到吸收器件上，避免损坏其他电路。吸收器件能够吸收 ESD 脉冲能量、限制电压值来保护电路。串联电阻限制了输入和输出的电流。 值得注意的是，大的串联电阻能够提供更好的保护，但是也会使芯片的噪声或者最大输出电流等指标变差。因为有这些限制，串联电阻会影响到某些器件的 ESD 性能。

ESD Protection with Pulse Applied
添加脉冲时的ESD保护

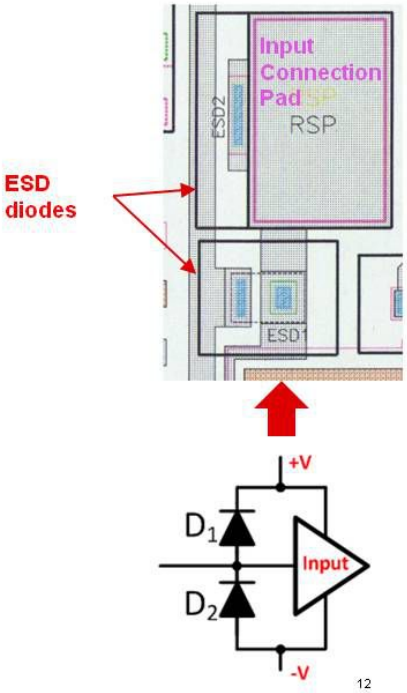


- These specifications are meant to give a general idea of the ESD diode's performance. Actual diodes will very depending on the device design and the process used. One key thing to notice is that the diode drop is about 0.7V with significant current. This diode is designed to take amps of pulse currents for only a few nanoseconds, as is typical with ESD pulses. However, they are rated for only 10mA of continuous current. These diodes also have a reverse leakage current that may be less then a nano-amp at room temperature, but could be hundreds of nano-amps at high temperatures. In fact, leakage current from ESD diodes makes up the majority of the "bias current" of CMOS devices. Finally, it should be noted that the ESD diodes have parasitic capacitance in the low pico-farads.

- 这些参数让我们对 ESD 二极管的性能有一个基本的了解。实际情况下，二极管性能由设计和工艺来决定。很重要的一点是，二极管导通压降为 0.7V 时，导通电流很大。对应于 ESD 脉冲的情形，这种二极管能够保护芯片免受几 ns 的、安培级别的脉冲电流的损害。但如果是持续的电流，只有约 10mA。这些二极管还会引入反方向的漏电流。在室温下，漏电流只有几 nA 或更小；但是高温时，漏电流可以达到几百 nA。实际上，CMOS 器件的输入偏置电流大部分都是由 ESD 二极管的漏电流造成的。最后，大家还需要记住，ESD 二极管还会引入几 pF 的寄生电容。

ESD Diode Specifications
ESD二极管的参数

Specification	Typical Value
Diode Drop (250mA)	0.7 V
Diode Drop (2A)	1 V
Pulse Current	A (for ns)
Continuous Current	10 mA
Leakage Current	0.5 nA (25°C, typical) 500 nA (125°C, typical)
Parasitic Capacitance	1 pF to 2 pF



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TEXAS INSTRUMENTS

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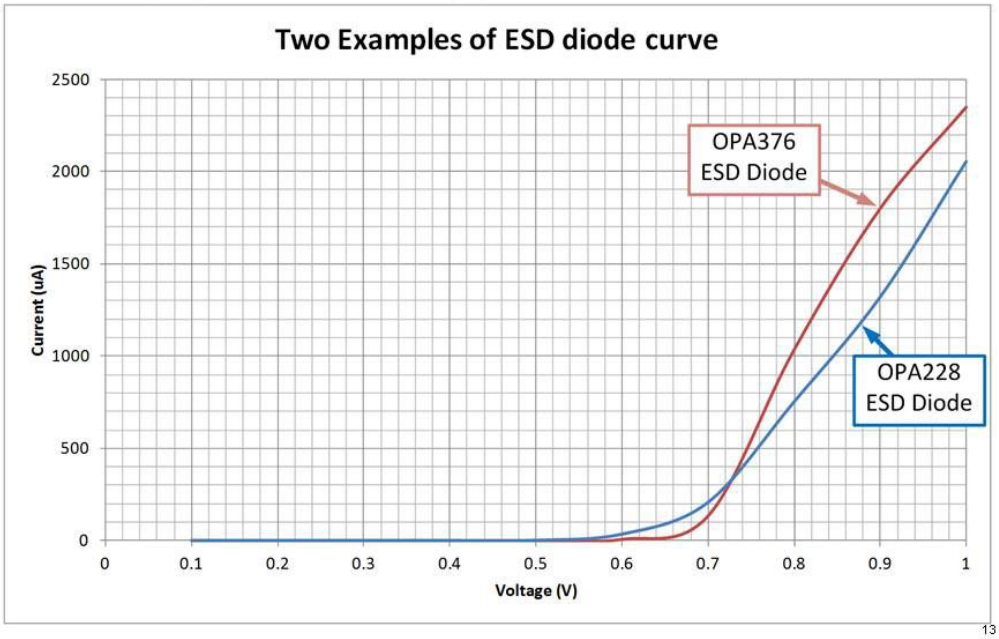
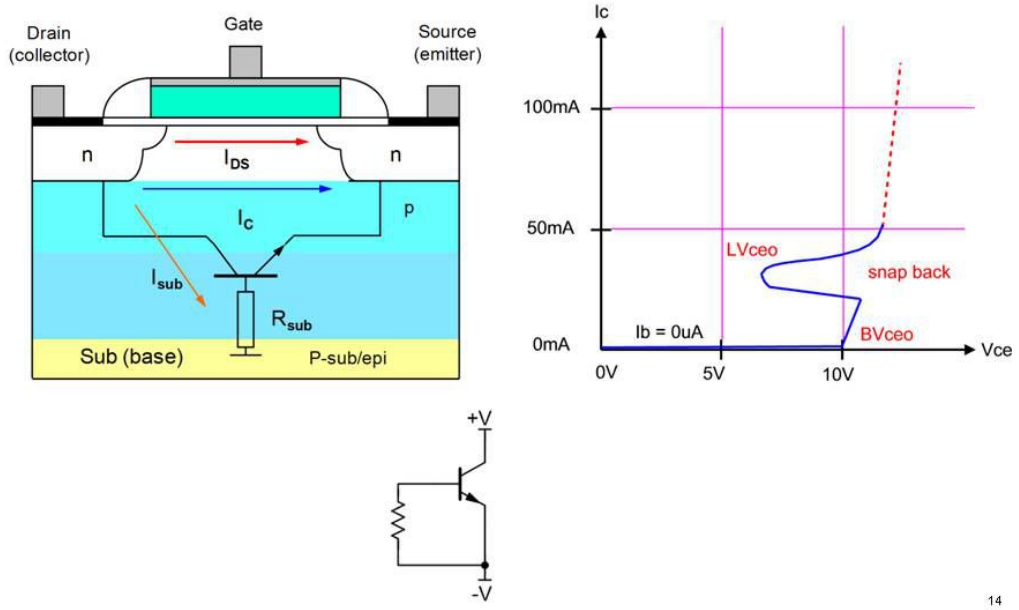
ESD Diode Curve Examples
ESD二极管的I-V 曲线示例



- Here we take a look at the I-V characteristic for the ESD diodes in two different op amp ICs. Notice that at low currents, the forward drop is about 0.7 V and at high current the drop increases to about 1V. Understanding the ESD diode characteristics will become useful when investigating electrical overstress issues in later videos.

- 这里，我们来看一下两种运放芯片中 ESD 二极管的 I-V 曲线。可以看到，低电流时二极管的正向压降约为 0.7V；大电流时导通压降增加到 1V。理解 ESD 二极管特性可以帮助更好地理解后续视频中的电气过压问题。

Absorption Device
吸收器件



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Texas Instruments

We previously discussed the absorption device only in a very general sense. The absorption device is a parasitic bipolar device that is formed vertically with regards to the substrate. Normally, this device is reverse biased so that no base current flows. As the voltage across the device increases, the Collector-to-Emitter reverse breakdown is approached. Increasing the voltage beyond the breakdown level causes a rapid increase in current. Collector current will increase until a point where a “snap back” takes place. Beyond the snap region, current again begins to rapidly increase. If there isn’t another source of resistance in the transistor’s path to limit the current, it can increase to the point where the thermal generation results in excessively high temperatures and transistor melt down. Usually the emitter ends up spiking through the base and shorting to the collector forming a permanent short circuit.

The absorption device is designed to clamp the supply voltage during an **out-of-circuit** ESD event to prevent damage. Once the event ends, typically after a few nano-seconds, the absorption device turns off since there is no power supply connected to the device. On the other hand, if the absorption device turns on for an **in-circuit** event, it will remain on and in a low impedance state until power is removed from the circuit. Thus, it is imperative that the absorption device is not allowed to turn on during in-circuit electrical overstress events. This topic is the focus of the next video series.

前面的章节中，我们粗略地讨论了下吸收器件。这里的吸收器件是一个由衬底引入的寄生三极管。 正常情况下，这个三极管是反偏的，所以不会有衬底电流。 当

加到三极管上的电压升高，接近集电极-发射极的击穿区时，加大处于击穿区的三极管上的电压，电流会急剧增大。集电极的电流会增加直到进入一个点，称为回跳点 (snap back)的区域。在超过这个区域之后，电流会持续快速增加。如果在三极管的电流通路上，没有一个电阻来限制电流；电流过大会造成芯片过热，直到三极管烧坏。这时候，通常情况下，发射极电流会停止升高，并和集电极之间形成一个永久的短路。

吸收器件是用来钳制供电电压、避免芯片在未安装到电路之前损坏而设计的。当ESD 结束后，因为没有电压加到器件上，一般几个 ns 以后，吸收器件就会关闭。另一方面，如果芯片被安装到电路中以后发生 ESD 现象，吸收器件会持续开通，并保持一个低阻的状态，直到电源电压关掉。因此在芯片过压时，不能让吸收装置开启。这个话题，我们将在后面的视频中进一步探讨。

Absolute Maximum Ratings
绝对最大额定值

			VALUE	UNIT
Supply voltage			±20 (+40, single supply)	V
Signal input terminals	Voltage	Common-mode	(V-) - 0.5 to (V+) + 0.5	V
		Differential	(V+) - (V-) + 0.2	V
	Current		±10	mA
Output short circuit			Continuous	mA
Operating temperature			-55 to +150	°C
Storage temperature			-55 to +150	°C
Junction temperature			+150	°C
Electrostatic discharge (ESD) ratings	Human Body Model (HBM)		4	kV
	Charged device model (CDM)		1	kV

- The absolute maximum ratings given in a device data sheet describe the worst case conditions that can be applied to a device before damage occurs. Maximum supply voltage, input voltage, input current, and temperature are given. Notice that the maximum input current is given as ±10mA. This is the limit for most devices and is based on the maximum continuous current that the ESD diodes can sustain. Also notice that the ESD ratings for the device are given in the maximum ratings table. In this example, the rating is 4kV for human body model and 1kV for charged device model. Different devices will achieve different ratings based on their performance during characterization.

- 芯片数据手册中的最大额定值，是指在最坏的情况下不让芯片损坏的数值。表格中给出了最大供电电压，输入电压，输入电流，温度等指标。注意到，最大输入电流是±10mA。对于大多数器件来说，这都是一个极限值；这个值是根据 ESD 二极管所能承受的最大持续电流值得来的。 同样，表格中也给出了芯片的 ESD 指标。本例中，ESD 人体模型的额定值是 4kV，带电器件模型是 1kV。不同的器件，根据测试结果，ESD 性能指标会略有不同。

Thanks for your time!
Please try the quiz.

- That concludes this video – thank you for watching! Please try the quiz to check your understanding of the video's content.

- 以上就是本次视频的内容。谢谢观看！请准备好下面的一个小测试，看看你是否已掌握本次学习的内容。

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