

PGA204  
PGA205

# Programmable Gain INSTRUMENTATION AMPLIFIER

## FEATURES

- **DIGITALLY PROGRAMMABLE GAIN:**  
PGA204:  $G=1, 10, 100, 1000V/V$   
PGA205:  $G=1, 2, 4, 8V/V$
- **LOW OFFSET VOLTAGE:**  $50\mu V$  max
- **LOW OFFSET VOLTAGE DRIFT:**  $0.25\mu V/^{\circ}C$
- **LOW INPUT BIAS CURRENT:**  $2nA$  max
- **LOW QUIESCENT CURRENT:**  $5.2mA$  typ
- **NO LOGIC SUPPLY REQUIRED**
- **16-PIN PLASTIC DIP, SOL-16 PACKAGES**

## APPLICATIONS

- **DATA ACQUISITION SYSTEM**
- **GENERAL PURPOSE ANALOG BOARDS**
- **MEDICAL INSTRUMENTATION**

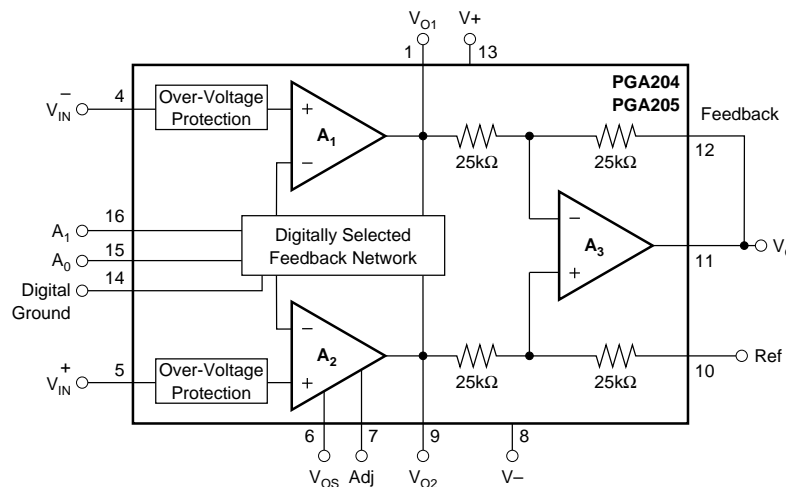
## DESCRIPTION

The PGA204 and PGA205 are low cost, general purpose programmable-gain instrumentation amplifiers offering excellent accuracy. Gains are digitally selected: PGA204—1, 10, 100, 1000, and PGA205—1, 2, 4, 8V/V. The precision and versatility, and of the PGA204 and PGA205 make them ideal for a wide range of applications.

Gain is selected by two TTL or CMOS-compatible address lines,  $A_0$  and  $A_1$ . Internal input protection diodes can withstand up to  $\pm 40V$  on the analog inputs without damage.

The PGA204 and PGA205 are laser trimmed for low offset voltage ( $50\mu V$ ), drift ( $0.25\mu V/^{\circ}C$ ) and high common-mode rejection ( $115dB$  at  $G=1000$ ). They operate with power supplies as low as  $\pm 4.5V$ , allowing use in battery operated systems. Quiescent current is  $5.2mA$  typical.

The PGA204 and PGA205 are available in plastic DIP, and SOL-16 surface-mount packages. They are specified for the  $-40^{\circ}C$  to  $+85^{\circ}C$  temperature range.



PGA204和PGA205是低成本、通用可编程增益仪表放大器，提供极佳的精度。增益是数字选择的：  
PGA204—1, 10, 100, 1000和  
PGA205—1, 2, 4, 8V/V。PGA204和PGA205的精度和多功能性以及低成本使其成为各种应用的理想选择。增益由两条TTL或CMOS兼容地址线A0和A1选择。内部输入保护可以在模拟输入上承受高达 $\pm 40V$ 的电压，而不会损坏。PGA204和PGA205是针对非常低的失调电压 ( $50\mu V$ )，漂移 ( $0.25\mu V/^{\circ}C$ ) 和高共模抑制 ( $115dB, G=1000$ ) 进行激光修整。它们使用低至 $\pm 4.5V$ 的电源工作，允许在电池供电系统中使用。静态电流为 $5mA$ 。PGA204和PGA205采用16引脚塑料DIP和SOL-16表面贴装封装，规定工作温度范围为 $-40^{\circ}C$ 至 $+85^{\circ}C$

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706  
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

## ELECTRICAL

## PGA204 G=1, 10, 100, 1000V/V

At  $T_A = +25^{\circ}\text{C}$ ,  $V_S = \pm 15\text{V}$ , and  $R_L = 2\text{k}\Omega$  unless otherwise noted.

PARAMETER	CONDITIONS	PGA204BP, BU			PGA204AP, AU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>INPUT</b>								
Offset Voltage, RTI vs Temperature	$T_A = +25^{\circ}\text{C}$ $T_A = T_{\text{MIN}}$ to $T_{\text{MAX}}$ $V_S = \pm 4.5\text{V}$ to $\pm 18\text{V}$		$\pm 10 + 20/\text{G}$ $\pm 0.1 + 0.5/\text{G}$ $0.5 + 2/\text{G}$ $\pm 0.2 + 0.5/\text{G}$	$\pm 50 + 100/\text{G}$ $\pm 0.25 + 5/\text{G}$ $3 + 10/\text{G}$		$\pm 25 + 30/\text{G}$ $\pm 0.25 + 5/\text{G}$	$\pm 125 + 500/\text{G}$ $\pm 1 + 10/\text{G}$	$\mu\text{V}$ $\mu\text{V}/^{\circ}\text{C}$ $\mu\text{V}/\text{V}$ $\mu\text{V}/\text{mo}$
Impedance, Differential Common-Mode Input Common-Mode Range Safe Input Voltage Common-Mode Rejection	$V_O = 0\text{V}$ (see text)  $V_{\text{CM}} = \pm 10\text{V}$ , $\Delta R_S = 1\text{k}\Omega$ $G=1$ $G=10$ $G=100$ $G=1000$	$\pm 10.5$     80 96 110 115	$\pm 12.7$     99 114 123 123	$\pm 40$     	*     75 90 106 106	*     90 106 110 110	*     	$\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$ $\text{V}$ $\text{V}$  dB dB dB dB
<b>BIAS CURRENT</b>			$\pm 0.5$	$\pm 2$		*	$\pm 5$	nA
vs Temperature			$\pm 8$			*		pA/ $^{\circ}\text{C}$
<b>Offset Current</b>			$\pm 0.5$	$\pm 2$		*	*	nA
vs Temperature			$\pm 8$			*		pA/ $^{\circ}\text{C}$
<b>NOISE</b> , Voltage, RTI <sup>(1)</sup> : $f=10\text{Hz}$ $f=100\text{Hz}$ $f=1\text{kHz}$ $f_B = 0.1\text{Hz}$ to $10\text{Hz}$  Noise Current $f=10\text{Hz}$ $f=1\text{kHz}$ $f_B = 0.1\text{Hz}$ to $10\text{Hz}$	$G \geq 100$ , $R_S = 0\Omega$ $G \geq 100$ , $R_S = 0\Omega$ $G \geq 100$ , $R_S = 0\Omega$ $G \geq 100$ , $R_S = 0\Omega$		16 13 13 0.4			*		nV/ $\sqrt{\text{Hz}}$ nV/ $\sqrt{\text{Hz}}$ nV/ $\sqrt{\text{Hz}}$ $\mu\text{Vp-p}$
			0.4 0.2 18			*		pA/ $\sqrt{\text{Hz}}$ pA/ $\sqrt{\text{Hz}}$ pAp-p
<b>GAIN</b> , Error	$G=1$ $G=10$ $G=100$ $G=1000$		$\pm 0.005$ $\pm 0.01$ $\pm 0.01$ $\pm 0.02$	$\pm 0.024$ $\pm 0.024$ $\pm 0.024$ $\pm 0.05$		*	$\pm 0.05$ $\pm 0.05$ $\pm 0.05$ $\pm 0.1$	% % % %
Gain vs Temperature	$G=1$ to $1000$		$\pm 2.5$	$\pm 10$		*	*	ppm/ $^{\circ}\text{C}$
Nonlinearity	$G=1$ $G=10$ $G=100$ $G=1000$		$\pm 0.0004$ $\pm 0.0004$ $\pm 0.0004$ $\pm 0.0008$	$\pm 0.001$ $\pm 0.002$ $\pm 0.002$ $\pm 0.01$		*	$\pm 0.002$ $\pm 0.004$ $\pm 0.004$ $\pm 0.02$	% of FSR % of FSR % of FSR % of FSR
<b>OUTPUT</b>								
Voltage, Positive <sup>(2)</sup> Negative <sup>(2)</sup>	$I_O = 5\text{mA}$ , $T_{\text{MIN}}$ to $T_{\text{MAX}}$ $I_O = -5\text{mA}$ , $T_{\text{MIN}}$ to $T_{\text{MAX}}$	(V+)−1.5 (V−)+1.5	(V+)−1.3 (V−)+1.3		* *	* *		V V
Load Capacitance Stability			1000			*		pF
<b>Short Circuit Current</b>			+23/−17			*		mA
<b>FREQUENCY RESPONSE</b>								
Bandwidth, −3dB	$G=1$ $G=10$ $G=100$ $G=1000$		1 80 10 1			*		MHz kHz kHz kHz
Slew Rate	$V_O = \pm 10\text{V}$ , $G=10$	0.3	0.7		*	*		V/ $\mu\text{s}$
Settling Time <sup>(3)</sup> , 0.1%	$G=1$ $G=10$ $G=100$ $G=1000$		22 23 100 1000			*		$\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$
0.01%	$G=1$ $G=10$ $G=100$ $G=1000$		23 28 140 1300			*		$\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$
Overload Recovery	50% Overdrive		70			*		$\mu\text{s}$
<b>DIGITAL LOGIC</b>								
Digital Ground Voltage, $V_{\text{DG}}$		V−		(V+)−4	*		*	V
Digital Low Voltage		V−		$V_{\text{DG}} + 0.8\text{V}$	*		*	V
<b>Digital Input Current</b>			1			*		$\mu\text{A}$
Digital High Voltage		$V_{\text{DG}} + 2$		V+	*		*	V
<b>POWER SUPPLY</b> , Voltage		$\pm 4.5$	$\pm 15$	$\pm 18$	*	*	*	V
<b>Current</b>	$V_{\text{IN}} = 0\text{V}$		+5.2/−4.2	$\pm 6.5$		*	$\pm 7.5$	mA
<b>TEMPERATURE RANGE</b>								
Specification		−40		+85	*		*	$^{\circ}\text{C}$
Operating		−40		+125	*		*	$^{\circ}\text{C}$
$\theta_{\text{JA}}$			80			*		$^{\circ}\text{C}/\text{W}$

\* Specification same as PGA204BP.

NOTES: (1) Input-referred noise voltage varies with gain. See typical curves. (2) Output voltage swing is tested for  $\pm 10\text{V}$  min on  $\pm 11.4\text{V}$  power supplies. (3) Includes time to switch to a new gain.



**PGA204/205**



## PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER <sup>(1)</sup>
PGA204AP	16-Pin Plastic DIP	180
PGA204BP	16-Pin Plastic DIP	180
PGA204AU	SOL-16 Surface Mount	211
PGA204BU	SOL-16 Surface Mount	211
PGA205AP	16-Pin Plastic DIP	180
PGA205BP	16-Pin Plastic DIP	180
PGA205AU	SOL-16 Surface Mount	211
PGA205BU	SOL-16 Surface Mount	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

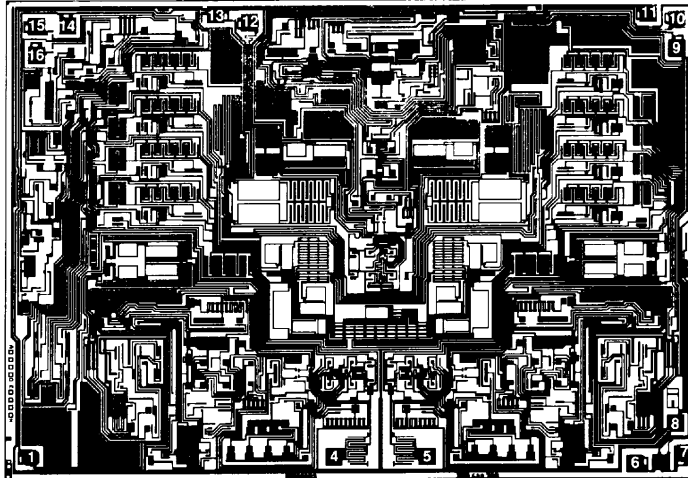
## ABSOLUTE MAXIMUM RATINGS

Supply Voltage .....	±18V
Analog Input Voltage Range .....	±40V
Logic Input Voltage Range .....	±V <sub>S</sub>
Output Short-Circuit (to ground) .....	Continuous
Operating Temperature .....	-40°C to +125°C
Storage Temperature .....	-40°C to +125°C
Junction Temperature .....	+150°C
Lead Temperature (soldering -10s) .....	+300°C

## ORDERING INFORMATION

MODEL	GAINS	PACKAGE	TEMPERATURE RANGE
PGA204AP	1, 10, 100, 1000V/V	16-Pin Plastic DIP	-40 to +85°C
PGA204BP	1, 10, 100, 1000V/V	16-Pin Plastic DIP	-40 to +85°C
PGA204AU	1, 10, 100, 1000V/V	SOL-16 Surface-Mount	-40 to +85°C
PGA204BU	1, 10, 100, 1000V/V	SOL-16 Surface-Mount	-40 to +85°C
PGA205AP	1, 2, 4, 8V/V	16-Pin Plastic DIP	-40 to +85°C
PGA205BP	1, 2, 4, 8V/V	16-Pin Plastic DIP	-40 to +85°C
PGA205AU	1, 2, 4, 8V/V	SOL-16 Surface-Mount	-40 to +85°C
PGA205BU	1, 2, 4, 8V/V	SOL-16 Surface-Mount	-40 to +85°C

## DICE INFORMATION



PGA204/205 DIE TOPOGRAPHY

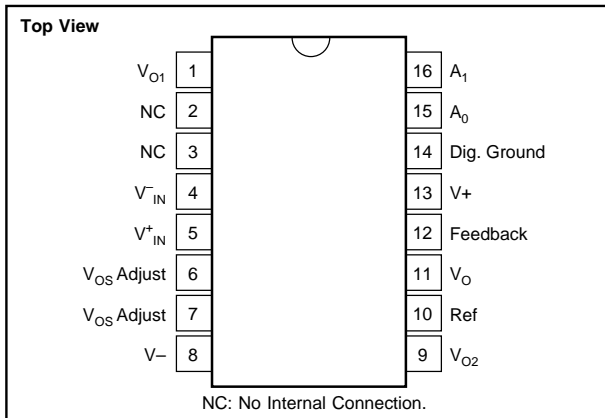
PAD	FUNCTION	PAD	FUNCTION
1	$V_{O1}$	9	$V_{O2}$
2	—	10	Ref
3	—	11	$V_O$
4	$V_{IN}^-$	12	Feedback
5	$V_{IN}^+$	13	$V_+$
6	$V_{OS}$ Adj	14	Dig. Ground
7	$V_{OS}$ Adj	15	$A_0$
8	$V_-$	16	$A_1$

Substrate Bias: Internally connected to  $V_-$  power supply.

## MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	186 x 130 ±5	4.72 x 3.30 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		Gold

## PIN CONFIGURATION



## ELECTROSTATIC DISCHARGE SENSITIVITY

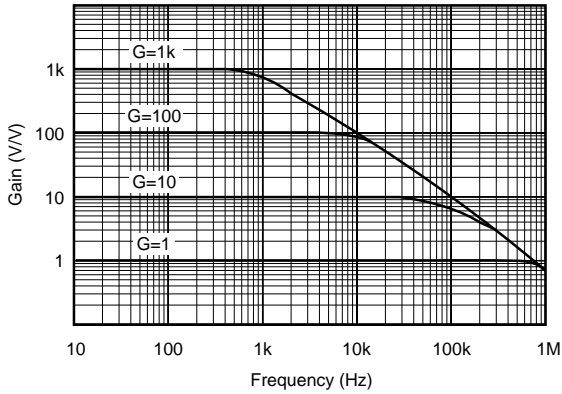
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

# TYPICAL PERFORMANCE CURVES

At  $T_A = +25^\circ\text{C}$ , and  $V_S = \pm 15\text{V}$ , unless otherwise noted.

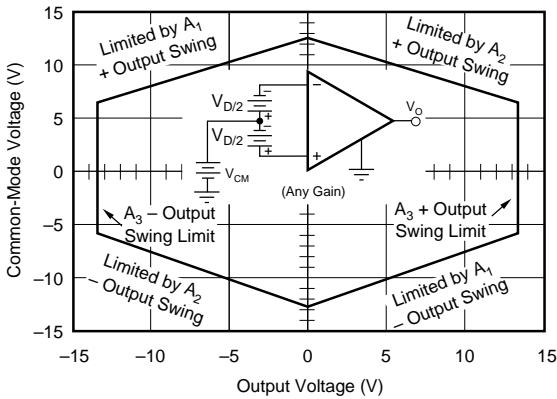
GAIN vs FREQUENCY



COMMON-MODE REJECTION vs FREQUENCY



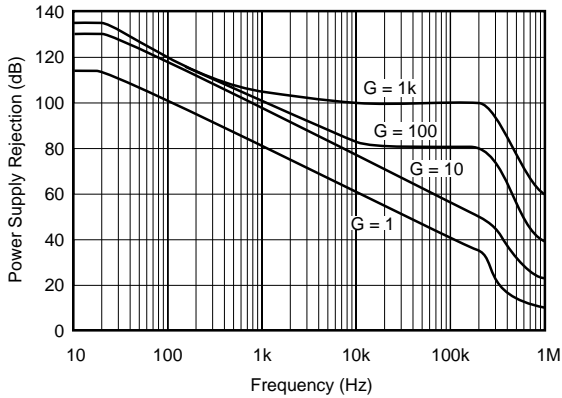
INPUT COMMON-MODE VOLTAGE RANGE vs OUTPUT VOLTAGE



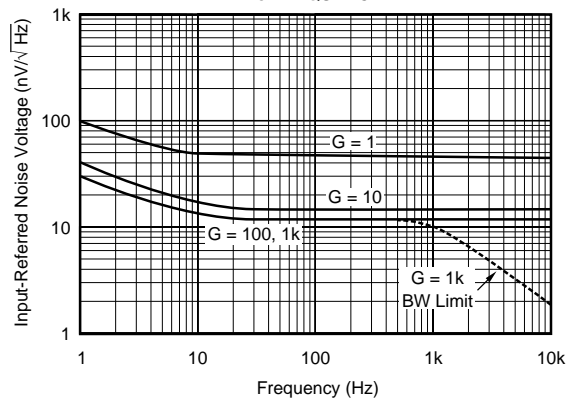
POSITIVE POWER SUPPLY REJECTION vs FREQUENCY



NEGATIVE POWER SUPPLY REJECTION vs FREQUENCY

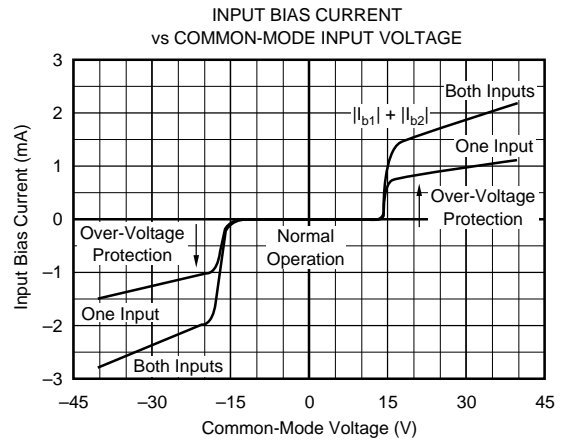
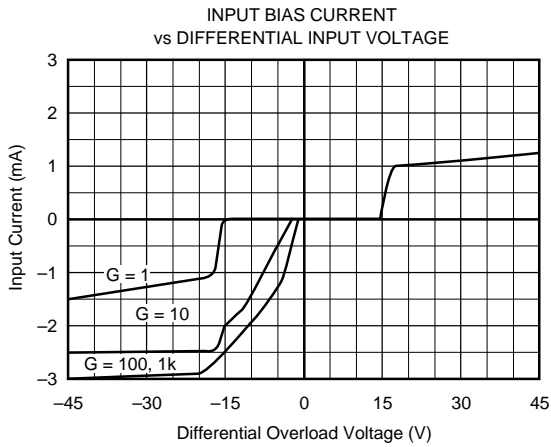
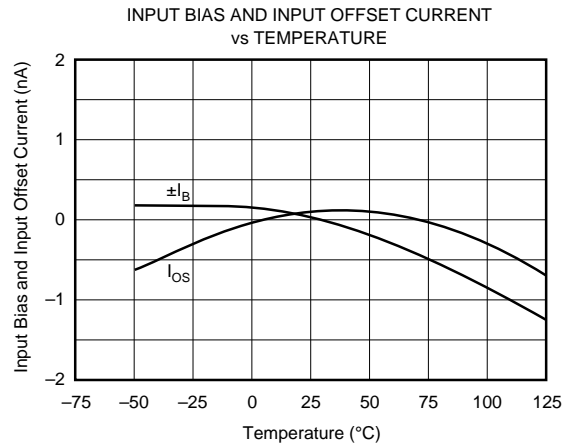


INPUT-REFERRED NOISE VOLTAGE vs FREQUENCY



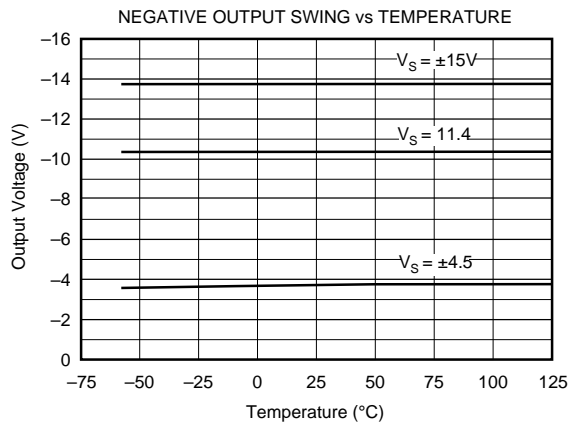
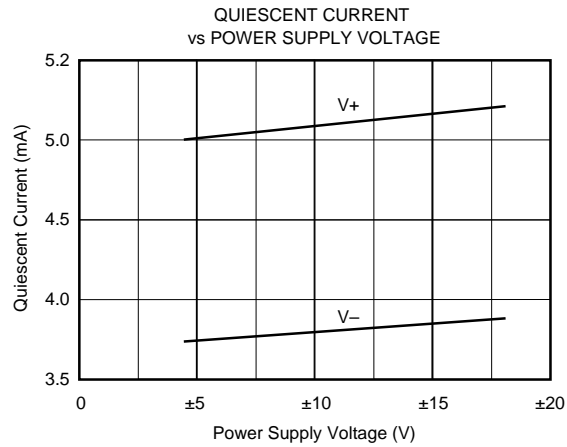
# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$ , and  $V_S = \pm 15\text{V}$ , unless otherwise noted.



# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$ , and  $V_S = \pm 15\text{V}$ , unless otherwise noted.

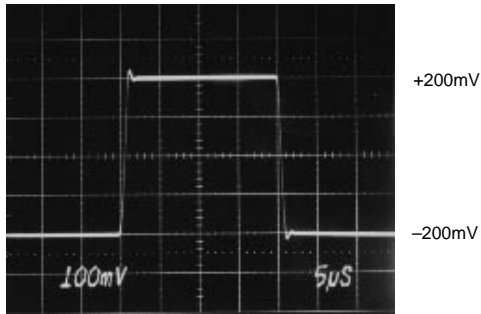




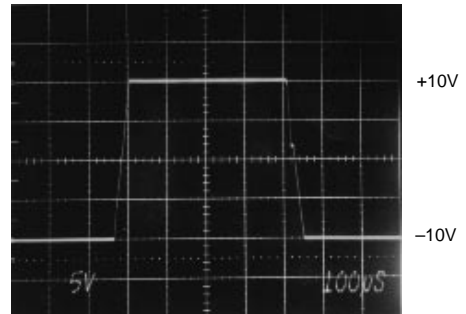
# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$ , and  $V_S = \pm 15\text{V}$ , unless otherwise noted.

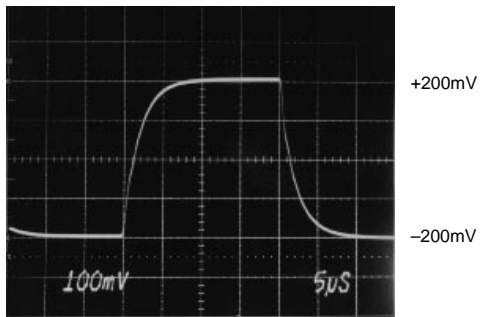
SMALL-SIGNAL RESPONSE,  $G = 1$



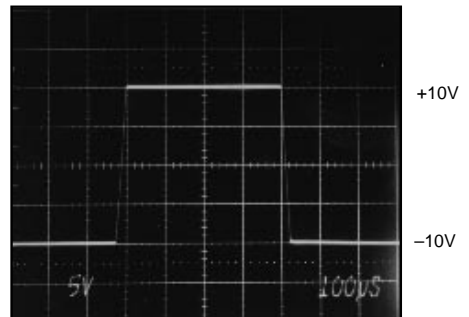
LARGE-SIGNAL RESPONSE,  $G = 1$



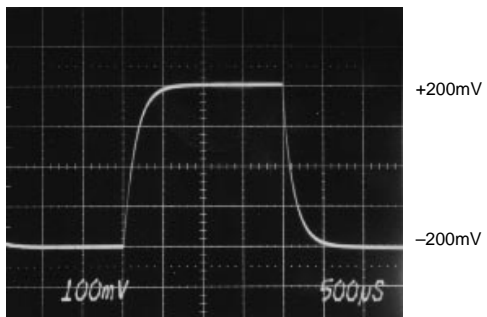
SMALL-SIGNAL RESPONSE,  $G = 10$



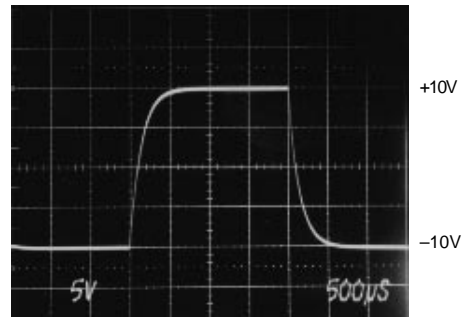
LARGE-SIGNAL RESPONSE,  $G = 10$



SMALL-SIGNAL RESPONSE,  $G = 1000$

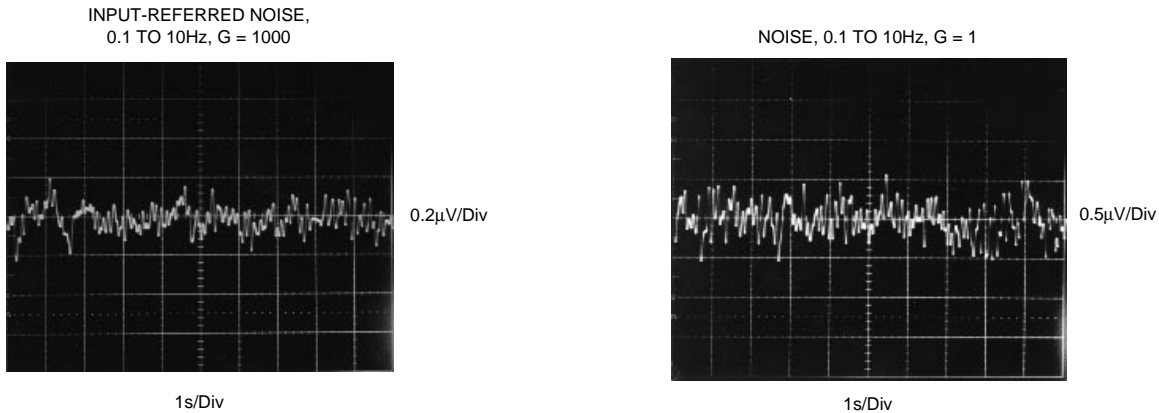


LARGE-SIGNAL RESPONSE,  $G = 1000$



# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$ , and  $V_S = \pm 15\text{V}$ , unless otherwise noted.



## APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the PGA204/205. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of  $5\Omega$  in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR ( $G=1$ ).

The PGA204/205 has an output feedback connection (pin 12). Pin 12 must be connected to the output terminal (pin 11) for proper operation. The output Feedback connection can

be used to sense the output voltage directly at the load for best accuracy.

### DIGITAL INPUTS

The digital inputs  $A_0$  and  $A_1$  select the gain according to the logic table in Figure 1. Logic "1" is defined as a voltage greater than 2V above digital ground potential (pin 14). Digital ground can be connected to any potential from the  $V^-$  power supply to 4V less than  $V^+$ . Digital ground is normally connected to ground. The digital inputs interface directly CMOS and TTL logic components.

Approximately  $1\mu\text{A}$  flows out of the digital input pins when a logic "0" is applied. Logic input current is nearly zero with a logic "1" input. A constant current of approximately

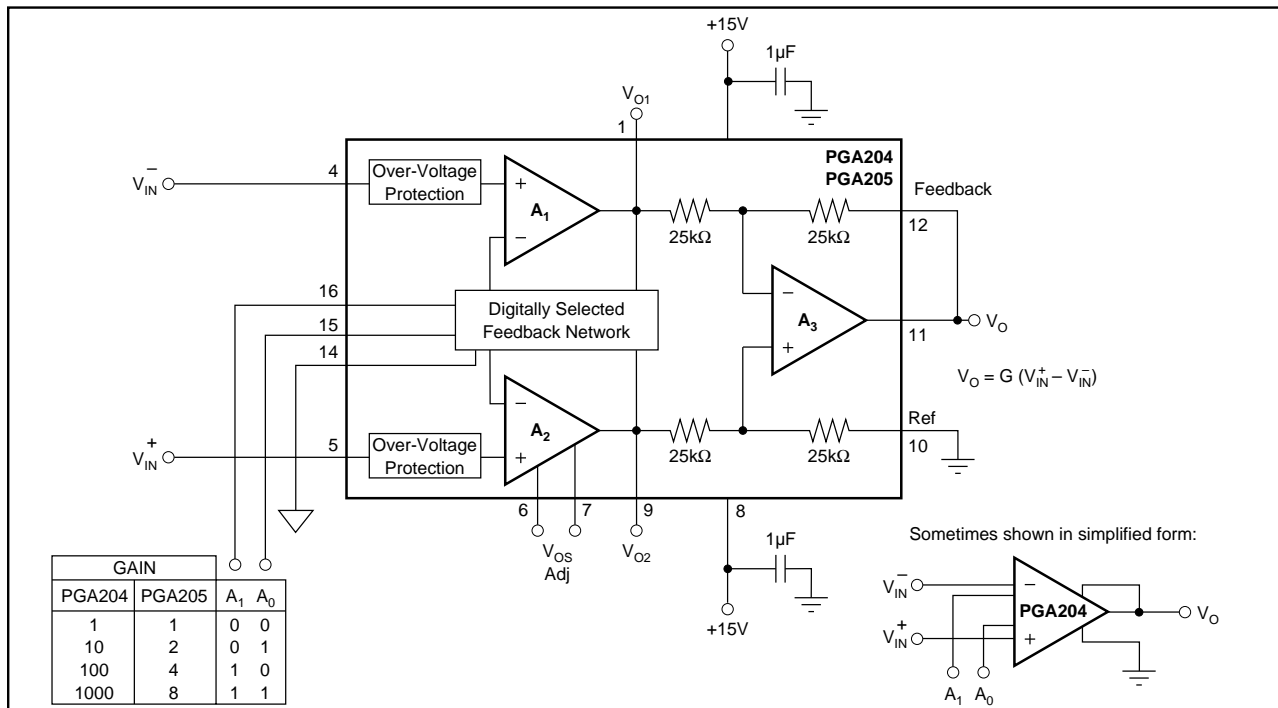


FIGURE 1. Basic Connections.

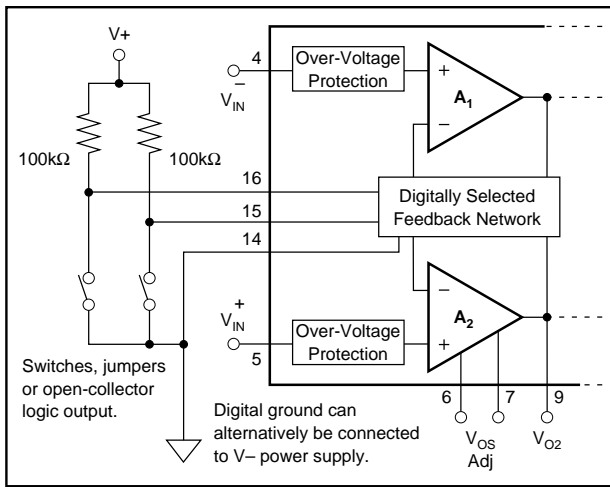


FIGURE 2. Switch or Jumper-Selected Digital Inputs.

1.3mA flows in the digital ground pin. It is good practice to return digital ground through a separate connection path so that analog ground is not affected by the digital ground current.

The digital inputs,  $A_0$  and  $A_1$ , are not latched; a change in logic inputs immediately selects a new gain. Switching time of the logic is approximately 1 $\mu$ s. The time to respond to gain change is effectively the time it takes the amplifier to settle to a new output voltage in the newly selected gain (see settling time specifications).

Many applications use an external logic latch to access gain control data from a high speed data bus (see Figure 7). Using an external latch isolates the high speed digital bus from sensitive analog circuitry. Locate the latch circuitry as far as practical from analog circuitry.

Some applications select gain of the PGA204/205 with switches or jumpers. Figure 2 shows pull-up resistors connected to assure a noise-free logic “1” when the switch, jumper or open-collector logic is open or off. Fixed-gain applications can connect the logic inputs directly to  $V+$  or  $V-$  (or other valid logic level); no resistor is required.

### OFFSET VOLTAGE

Voltage offset of the PGA204/205 consists of two components—input stage offset and output stage offset. Both components are specified in the specification table in equation form:

$$V_{OS} = V_{OSI} + V_{OSO} / G \quad (1)$$

where:

$V_{OS}$  total is the combined offset, referred to the input.

$V_{OSI}$  is the offset voltage of the input stage,  $A_1$  and  $A_2$ .

$V_{OSO}$  is the offset voltage of the output difference amplifier,  $A_3$ .

$V_{OSI}$  and  $V_{OSO}$  do not change with gain. The composite offset voltage  $V_{OS}$  changes with gain because of the gain term in equation 1. Input stage offset dominates in high gain ( $G \geq 100$ ); both sources of offset may contribute at low gain ( $G = 1$  to 10).

### OFFSET TRIMMING

Both the input and output stages are laser trimmed for very low offset voltage and drift. Many applications require no external offset adjustment.

Figure 3 shows an optional input offset voltage trim circuit. This circuit should be used to adjust only the input stage offset voltage of the PGA204/205. Do this by programming

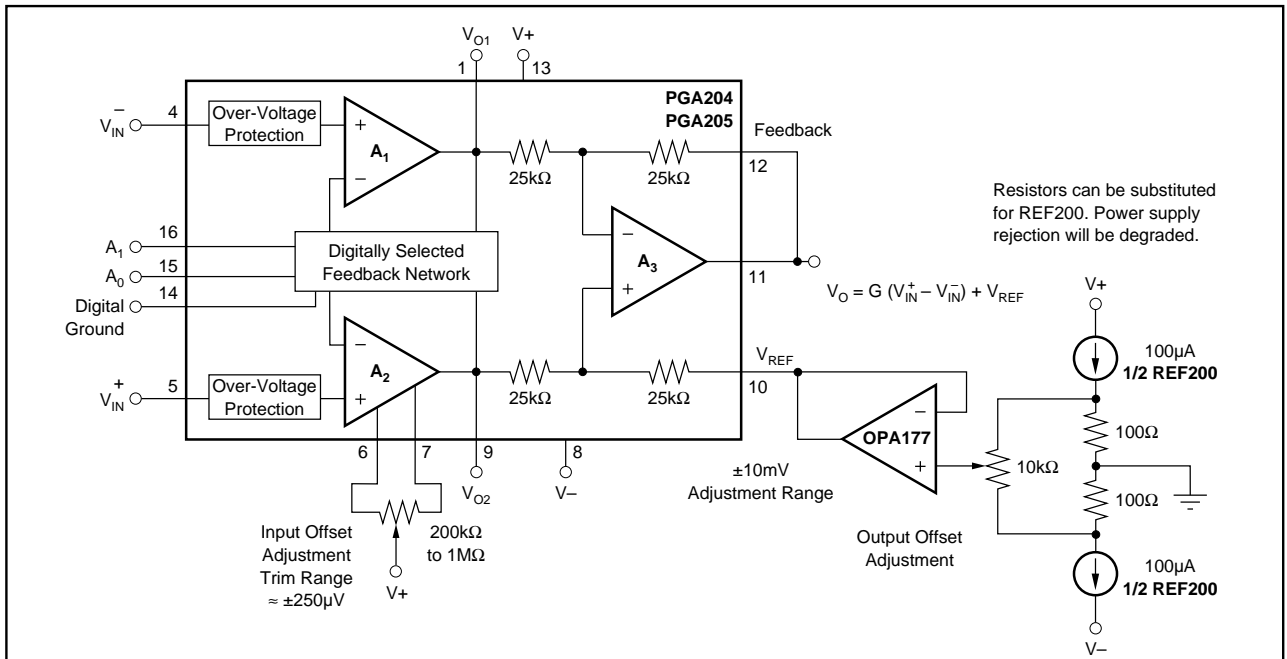


FIGURE 3. Optional Offset Voltage Trim Circuit.

it to its highest gain and trimming the output voltage to zero with the inputs grounded. Drift performance usually improves slightly when the input offset is nulled with this procedure.

Do not use the input offset adjustment to trim system offset or offset produced by a sensor. Nulling offset that is not produced by the input amplifiers will increase temperature drift by approximately  $3.3\mu\text{V}/^\circ\text{C}$  per 1mV of offset adjustment.

Many applications that need input stage offset adjustment do not need output stage offset adjustment. Figure 3 also shows a circuit for adjusting output offset voltage. First, adjust the input offset voltage as discussed above. Then program the device for  $G=1$  and adjust the output to zero. Because of the interaction of these two adjustments at  $G=8$ , the PGA205 may require iterative adjustment.

The output offset adjustment can be used to trim sensor or system offsets without affecting drift. The voltage applied to the Ref terminal is summed with the output signal. Low impedance must be maintained at this node to assure good common-mode rejection. This is achieved by buffering the trim voltage with an op amp as shown.

## NOISE PERFORMANCE

The PGA204/205 provides very low noise in most applications. Low frequency noise is approximately  $0.4\mu\text{Vp-p}$  measured from 0.1 to 10Hz. This is approximately one-tenth the noise of “low noise” chopper-stabilized amplifiers.

## INPUT BIAS CURRENT RETURN PATH

The input impedance of the PGA204/205 is extremely high—approximately  $10^{10}\Omega$ . However, a path must be provided for the input bias current of both inputs. This input bias current is typically less than  $\pm 1\text{nA}$  (it can be either polarity due to cancellation circuitry). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the PGA204/205 is to operate properly. Figure 4 shows provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the common-mode range of the PGA204/205 and the input amplifiers will saturate. If the differential source resistance is low, bias current return path can be connected to one input (see thermocouple example in Figure 4). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due bias current and better common-mode rejection.

Many sources or sensors inherently provide a path for input bias current (e.g. the bridge sensor shown in Figure 4). These applications do not require additional resistor(s) for proper operation.

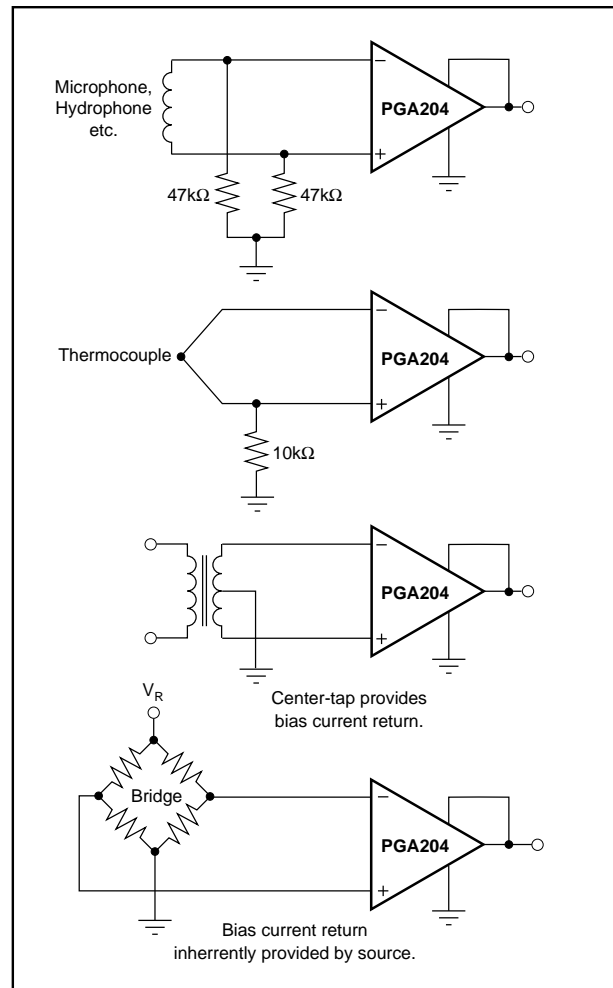


FIGURE 4. Providing an Input Common-Mode Current Path.

## INPUT COMMON-MODE RANGE

The linear common-mode range of the input op amps of the PGA204/205 is approximately  $\pm 12.7\text{V}$  (or 2.3V from the power supplies). As the output voltage increases, however, the linear input range will be limited by the output voltage swing of the input amplifiers,  $A_1$  and  $A_2$ . The common-mode range is related to the output voltage of the complete amplifier—see performance curve “Input Common-Mode Range vs Output Voltage”.

A combination of common-mode and differential input voltage can cause the output of  $A_1$  or  $A_2$  to saturate. Figure 5 shows the output voltage swing of  $A_1$  and  $A_2$  expressed in terms of a common-mode and differential input voltages. Output swing capability of these internal amplifiers is the same as the output amplifier,  $A_3$ . For applications where input common-mode range must be maximized, limit the output voltage swing by selecting a lower gain of the PGA204/205 (see performance curve “Input Common-Mode Voltage Range vs Output Voltage”). If necessary, add gain after the PGA204/205 to increase the voltage swing.

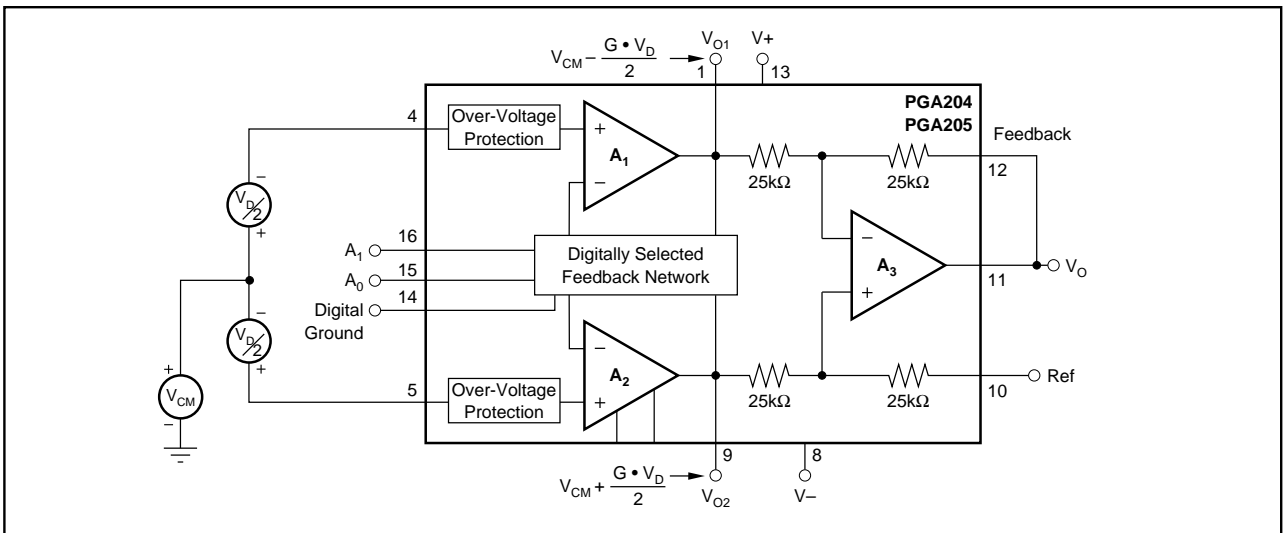


FIGURE 5. Voltage Swing of A<sub>1</sub> and A<sub>2</sub>.

Input-overload often produces an output voltage that appears normal. For example, consider an input voltage of +20V on one input and +40V on the other input will obviously exceed the linear common-mode range of both input amplifiers. Since both input amplifiers are saturated to the nearly the same output voltage limit, the difference voltage measured by the output amplifier will be near zero. The output of the PGA204/205 will be near 0V even though both inputs are overloaded.

### INPUT PROTECTION

The inputs of the PGA204/205 are individually protected for voltages up to ±40V. For example, a condition of -40V on one input and +40V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value (approximately 1.5mA). The typical performance curve “Input Bias Current vs Common-Mode Input Voltage” shows this input current limit behavior. The inputs are protected even if no power supply voltage is present.

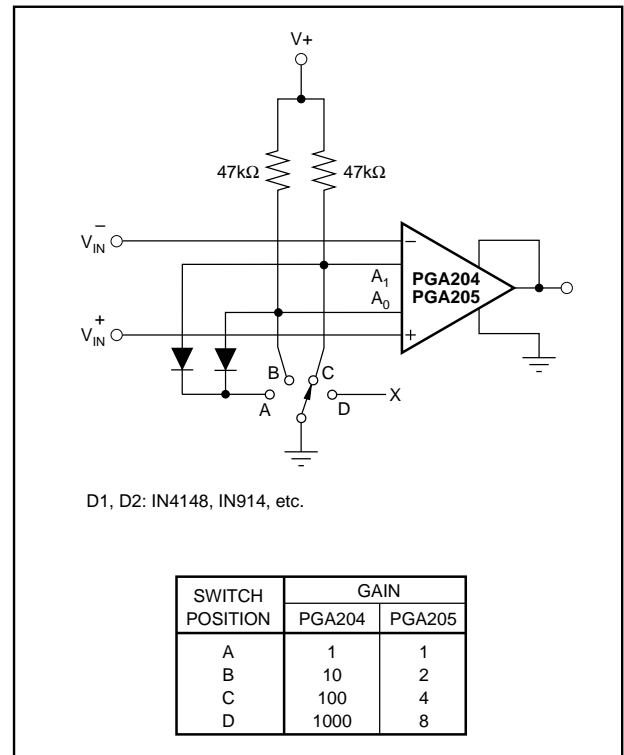


FIGURE 6. Switch-Selected PGIA.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.



FIGURE 7. Multiplexed-Input Programmable Gain IA.



FIGURE 8. Shield Drive Circuit.

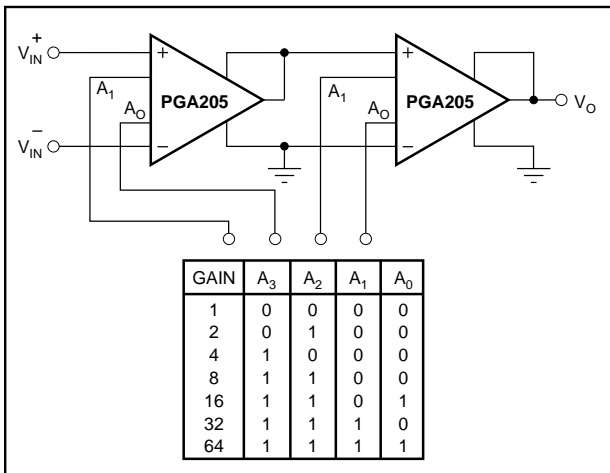


FIGURE 9. Binary Gain Steps, G=1 to G=64.

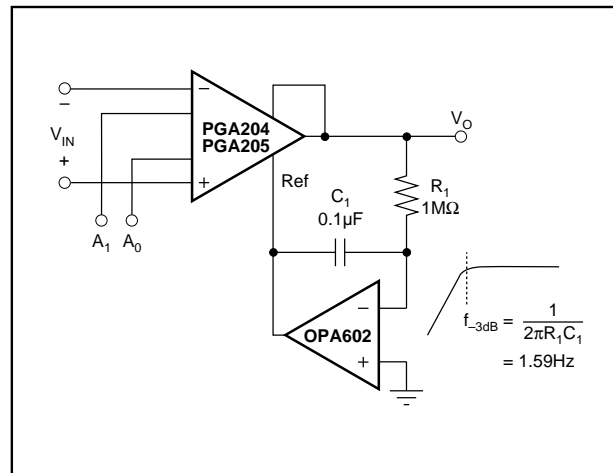


FIGURE 10. AC-Coupled PGIA.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PGA204AP	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		PGA204AP	<a href="#">Samples</a>
PGA204APG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		PGA204AP	<a href="#">Samples</a>
PGA204AU	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	PGA204AU	<a href="#">Samples</a>
PGA204AU/1K	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	PGA204AU	<a href="#">Samples</a>
PGA204AU/1KE4	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	PGA204AU	<a href="#">Samples</a>
PGA204AUE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	PGA204AU	<a href="#">Samples</a>
PGA204AUG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	PGA204AU	<a href="#">Samples</a>
PGA204BP	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		PGA204BP	<a href="#">Samples</a>
PGA204BPG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		PGA204BP	<a href="#">Samples</a>
PGA204BU	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR		PGA204BU	<a href="#">Samples</a>
PGA204BU/1K	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR		PGA204BU	<a href="#">Samples</a>
PGA204BUE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR		PGA204BU	<a href="#">Samples</a>
PGA205AP	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	PGA205AP	<a href="#">Samples</a>
PGA205APG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	PGA205AP	<a href="#">Samples</a>
PGA205AU	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	PGA205AU	<a href="#">Samples</a>
PGA205AU/1K	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	PGA205AU	<a href="#">Samples</a>
PGA205AU/1KG4	ACTIVE	SOIC	DW	16		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PGA205AUG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	PGA205AU	<a href="#">Samples</a>
PGA205BP	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	PGA205BP	<a href="#">Samples</a>
PGA205BPG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	PGA205BP	<a href="#">Samples</a>
PGA205BU	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	PGA205BU	<a href="#">Samples</a>
PGA205BUG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	PGA205BU	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA204AU/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
PGA204BU/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
PGA205AU/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA204AU/1K	SOIC	DW	16	1000	367.0	367.0	38.0
PGA204BU/1K	SOIC	DW	16	1000	367.0	367.0	38.0
PGA205AU/1K	SOIC	DW	16	1000	367.0	367.0	38.0

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)