Section 4

Interfacing High-Speed Amplifiers and A/D converters

Agenda

- High Speed ADC Drive Amplifier Options
- Combining Amplifier and ADC Performance
- Amplifier and ADC Interface Options
- Amplifier to ADC Design Example: THS4509 + ADS5413-11

Key Assumptions

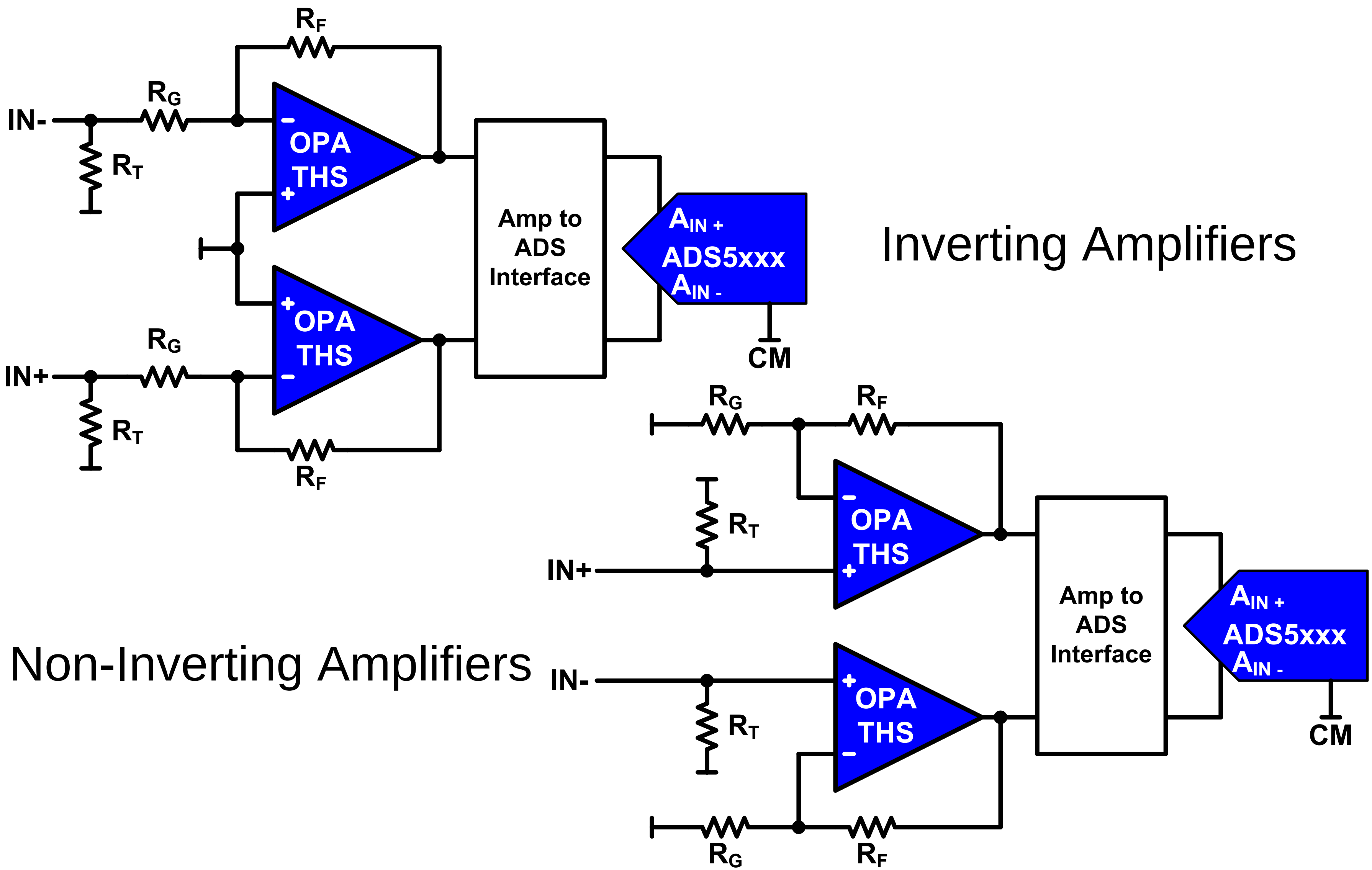
1. Only Looking at Frequency Domain Issues - focus specs are SNR and SFDR
2. Differential Input Signal to ADC Required
3. Target Specifications for both the converter and the system are known

ADC Drive Circuit Options

- Amplifiers
  - Single Ended Output Amplifiers
  - Fully Differential Amplifiers

- Topology
  - DC Coupled
  - AC Coupled
  - Differential In
  - Single Ended In

2 Single Ended Amplifiers

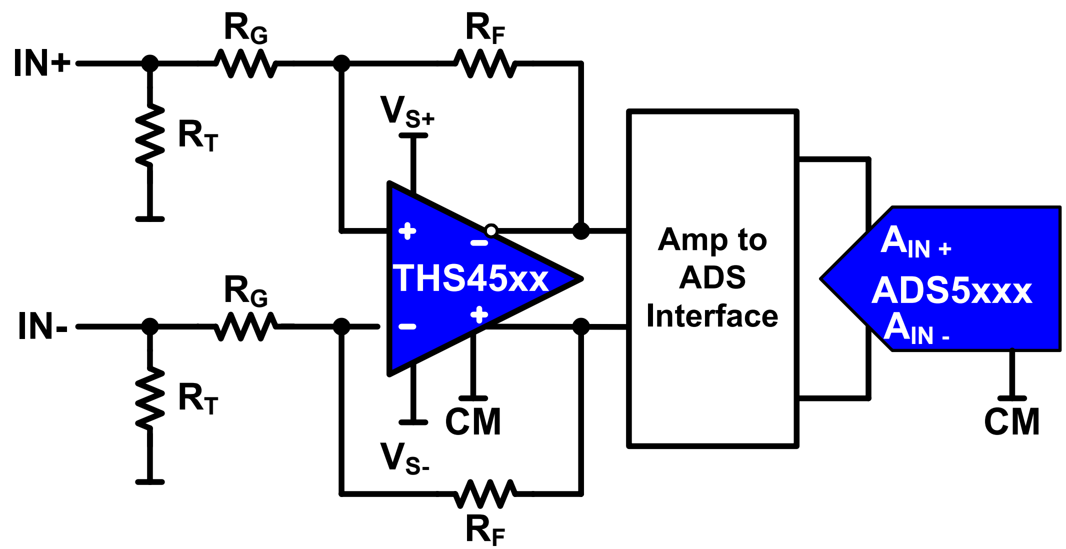


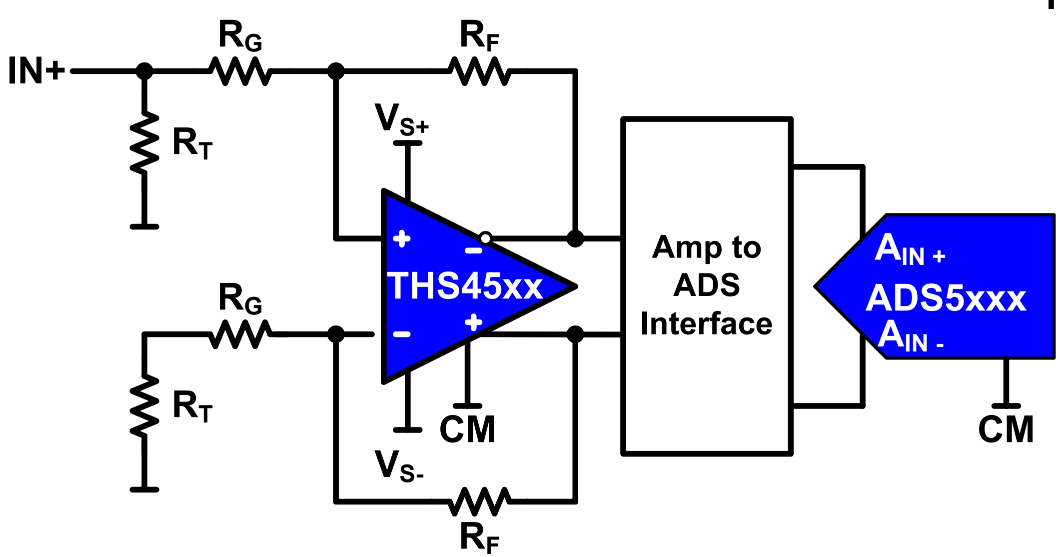
Inverting Amplifiers

Non-Inverting Amplifiers

Fully Differential Amplifiers

Differential Source



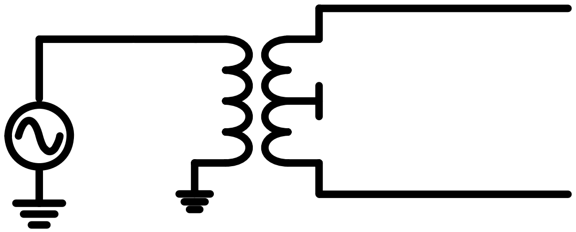


Single-Ended Source

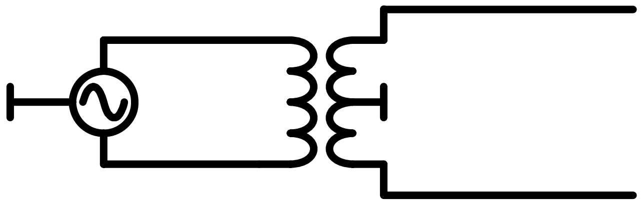
AC Coupling

Source to Amplifier or Amplifier to ADC

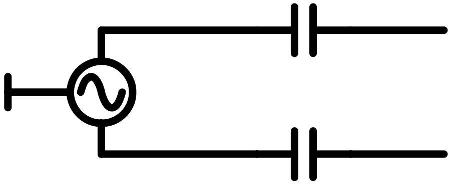
Single-Ended



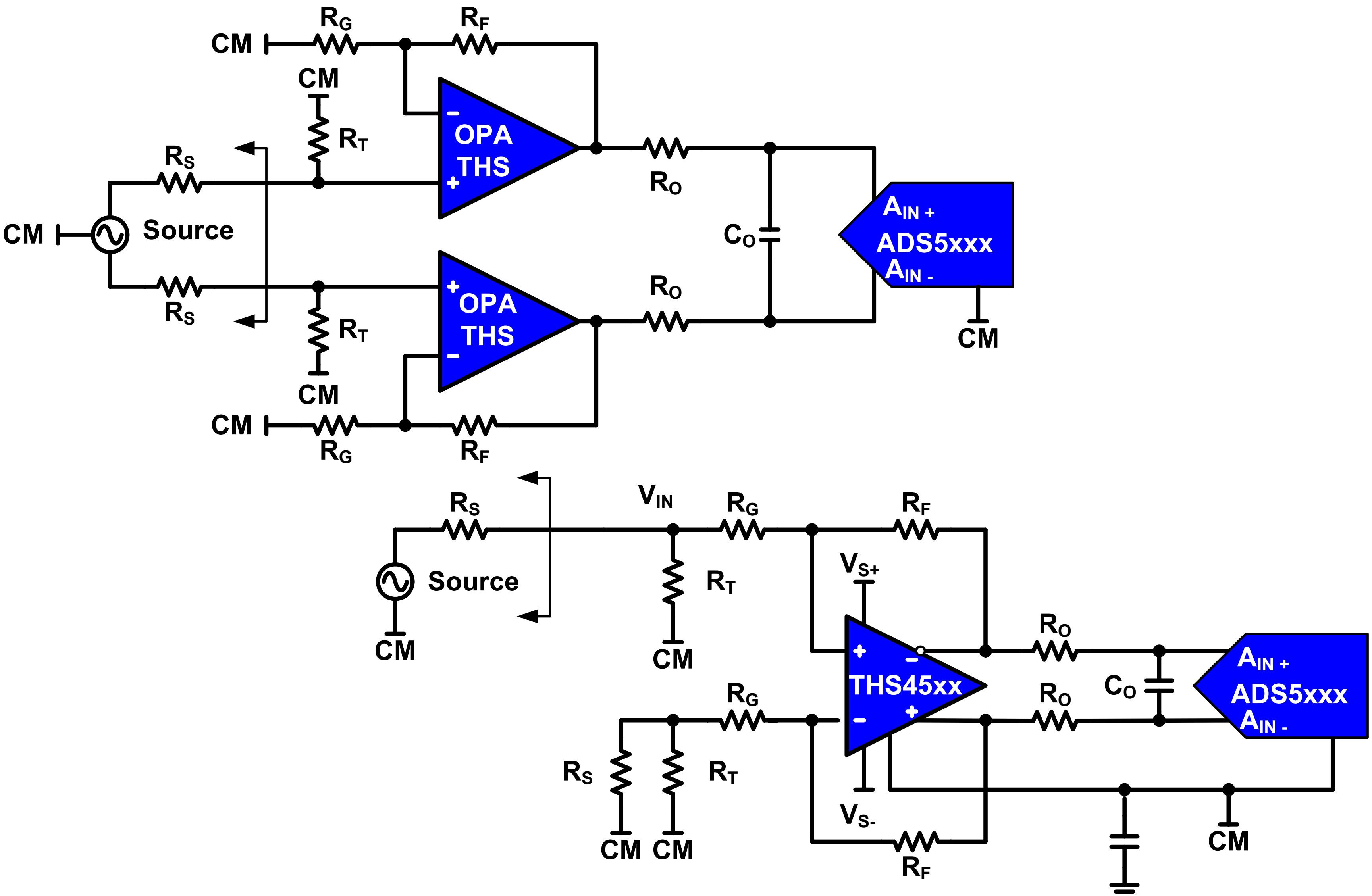
Differential



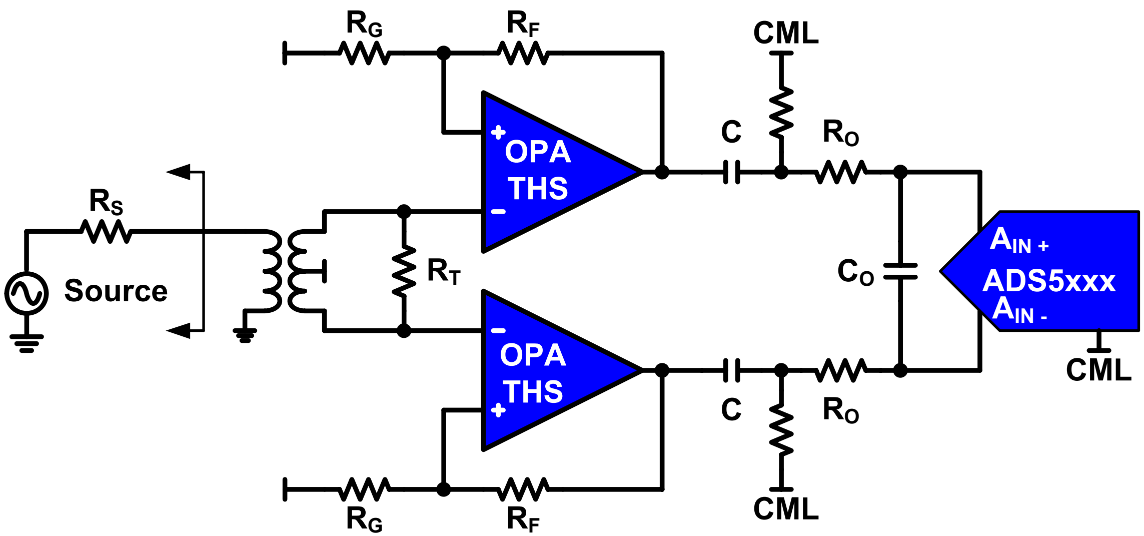
Differential

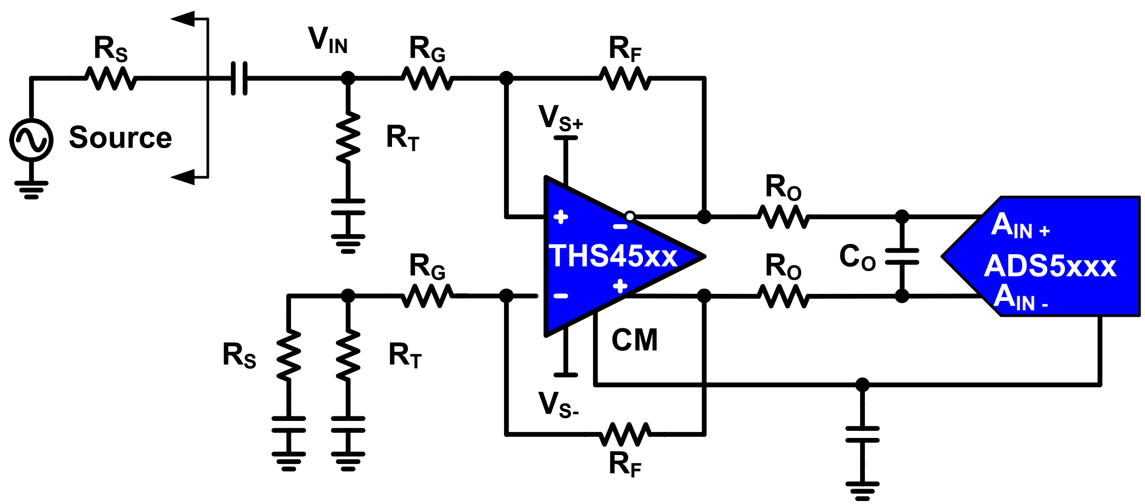


DC Coupling Examples



AC Coupling Examples





Combining Amplifier and ADC Performance

Combining Amplifier and ADC Performance

ADC

- **ADC Specs**
  - SNR (dB)
  - 2nd & 3rd Harmonic Distortion (dB)

Driver

- **Amplifier Specs**
  - Input Referred Noise (e_n : nV/√Hz)
  - 2nd & 3rd Harmonic Distortion (dB)

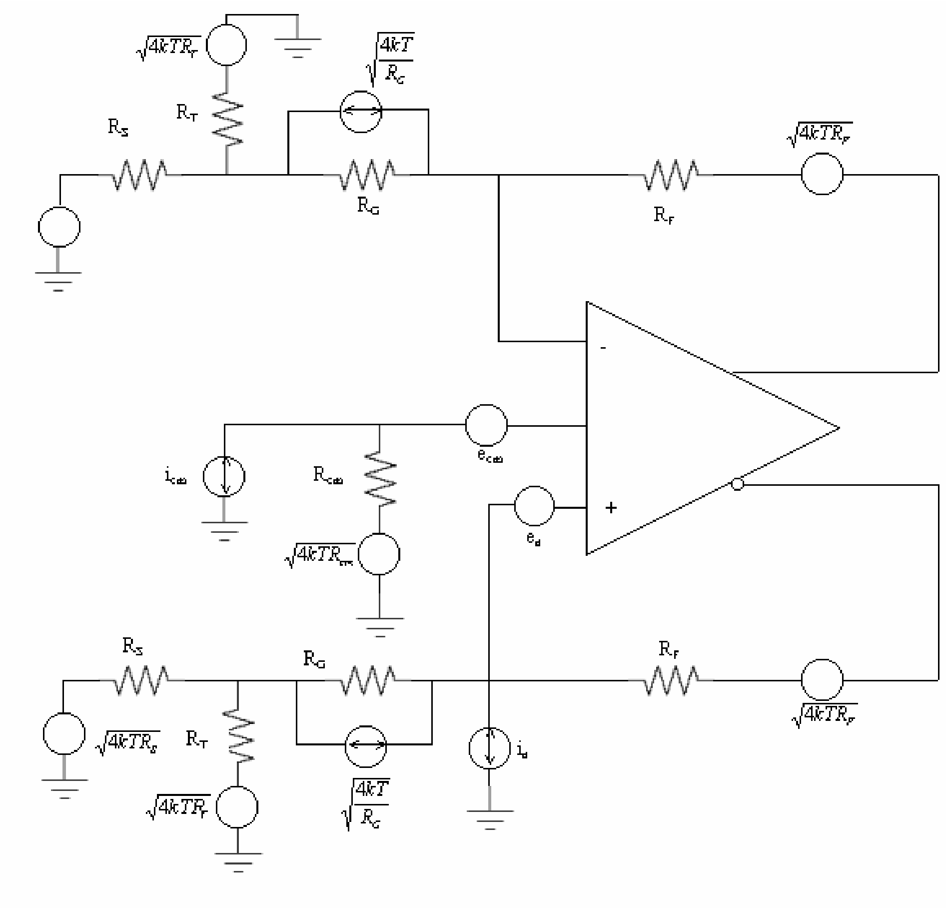
+

System

- **System Specs**
  - SNR_{System} (dB)
  - $SFDR_{System}$ (dB)

Differential Noise: Diff Amp

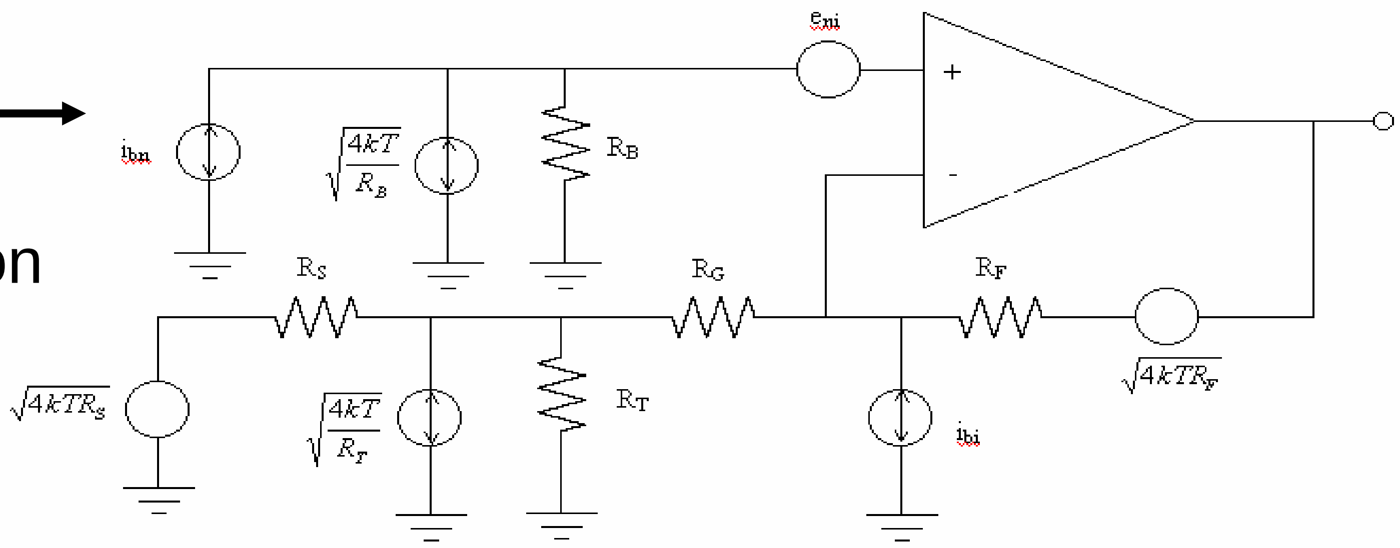
$$e_o^2 = (e_n NG)^2 + 2 \times (i_n R_F)^2 + 2 \times 4kTR_F NG$$



$$NG = 1 + \frac{R_F}{R_G + R_S \parallel R_T}$$

Diff. Noise: Diff. Configuration

½ of a differential configuration →



$$e_{odiff}^2 = 2\times[(e_{ni}^2 + (i_{bn}R_B)^2 + 4kTR_B)NG^2 + (i_{bi}R_F)^2 + 4kTR_F NG]$$

$$NG = 1 + \frac{R_F}{R_G + R_S \parallel R_T}$$

- Inverting and non-inverting amplifier in differential configuration have the same noise formula. What varies is the noise gain definition

Calculating RMS Noise (e_{RMS})

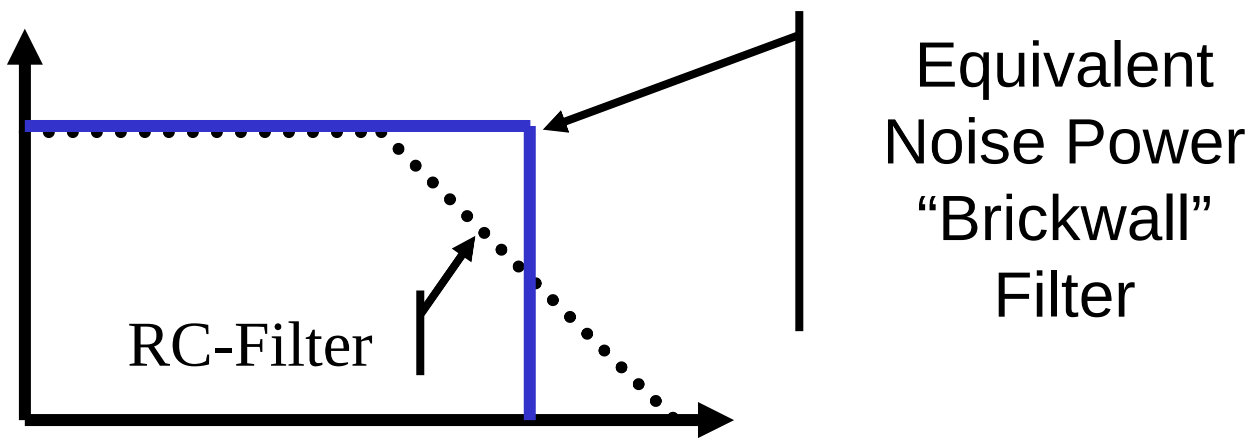
$$e_{RMS} = e_O \cdot \sqrt{f_{NPBW}}$$

- Minimize e_{RMS} by:
  - Minimizing e_O
  - Reduce f_{NPBW}

Calculating NPBW for RC Filter 1st Order Filter

$$f_{NPBW} = \frac{\pi}{2} \cdot f_C$$

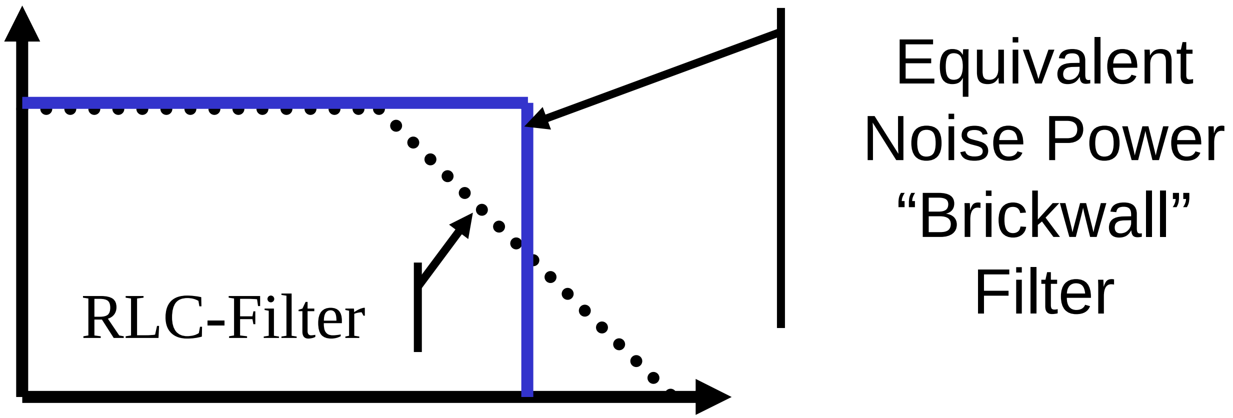
- f_{NPBW} is the noise bandwidth for the equivalent Noise Power “Brickwall” Filter for an RC filter of cut-off frequency of f_C



Calculating NPBW for RLC Filter 2nd Order Filter

$$f_{NPBW} = Q \cdot \frac{\pi}{2} \cdot f_C$$

- f_{NPBW} is the noise bandwidth for the equivalent Noise Power "Brickwall" Filter for an RLC filter of cut-off frequency of f_C



Calculating SNR For Amplifiers

$$SNR_{OPA} = 20 \cdot \log\left(\frac{V_{Signal\_RMS}}{e_{O\_RMS}}\right)$$

- SNR can be calculated with the above definition given the RMS signal amplitude and the RMS output noise.

But

- One difference in calculating the SNR for the converter and the amplifier.
  - The SNR is calculated at the input of the converter for the converter, thus using the full input range of the converter as defined in the datasheet.
  - For the Amplifier, the SNR needs to be calculated at the output of the Amplifier/Filter, thus using the full input range of the converter as value for the RMS signal.

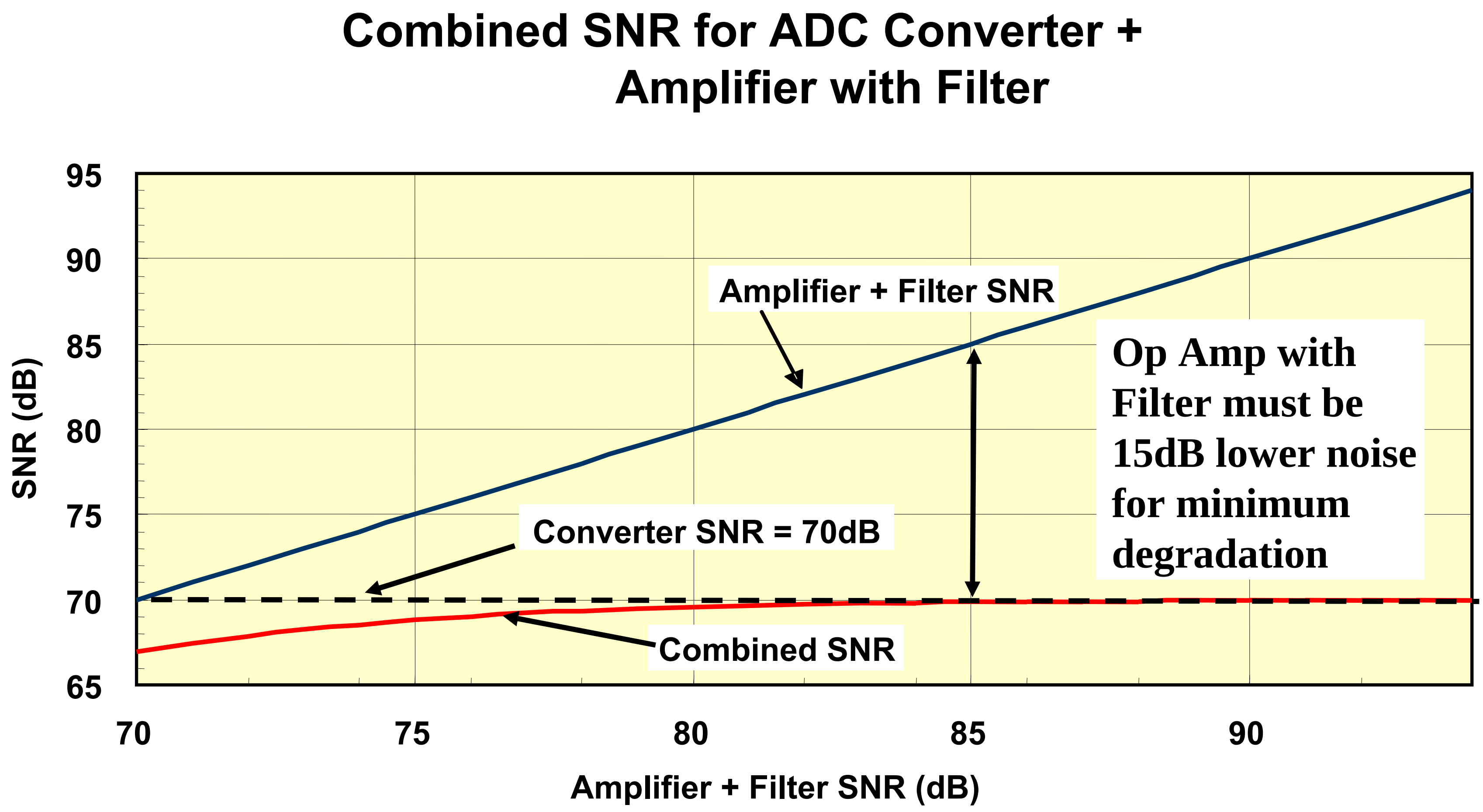
Adding Noise

$$SNR_{System} \approx -20 \cdot \log \sqrt{\left(10^{\frac{-SNR_{ADC}}{20}}\right)^2 + \left(10^{\frac{-SNR_{Op-Amp}}{20}}\right)^2}$$

- SNR_{System} is the RMS addition of SNR_{ADC} and SNR_{OPA}
- As an example, for a 70dB SNR_{ADC} for the converter, the combined SNR becomes →

SNR_{OPA}	**SNR_{System}**
65 dB	63.8 dB
70 dB	67 dB
75 dB	68.8 dB
80 dB	69.6 dB
85 dB	69.86 dB
90 dB	69.95 dB

Combined SNR for a 70dB Converter SNR



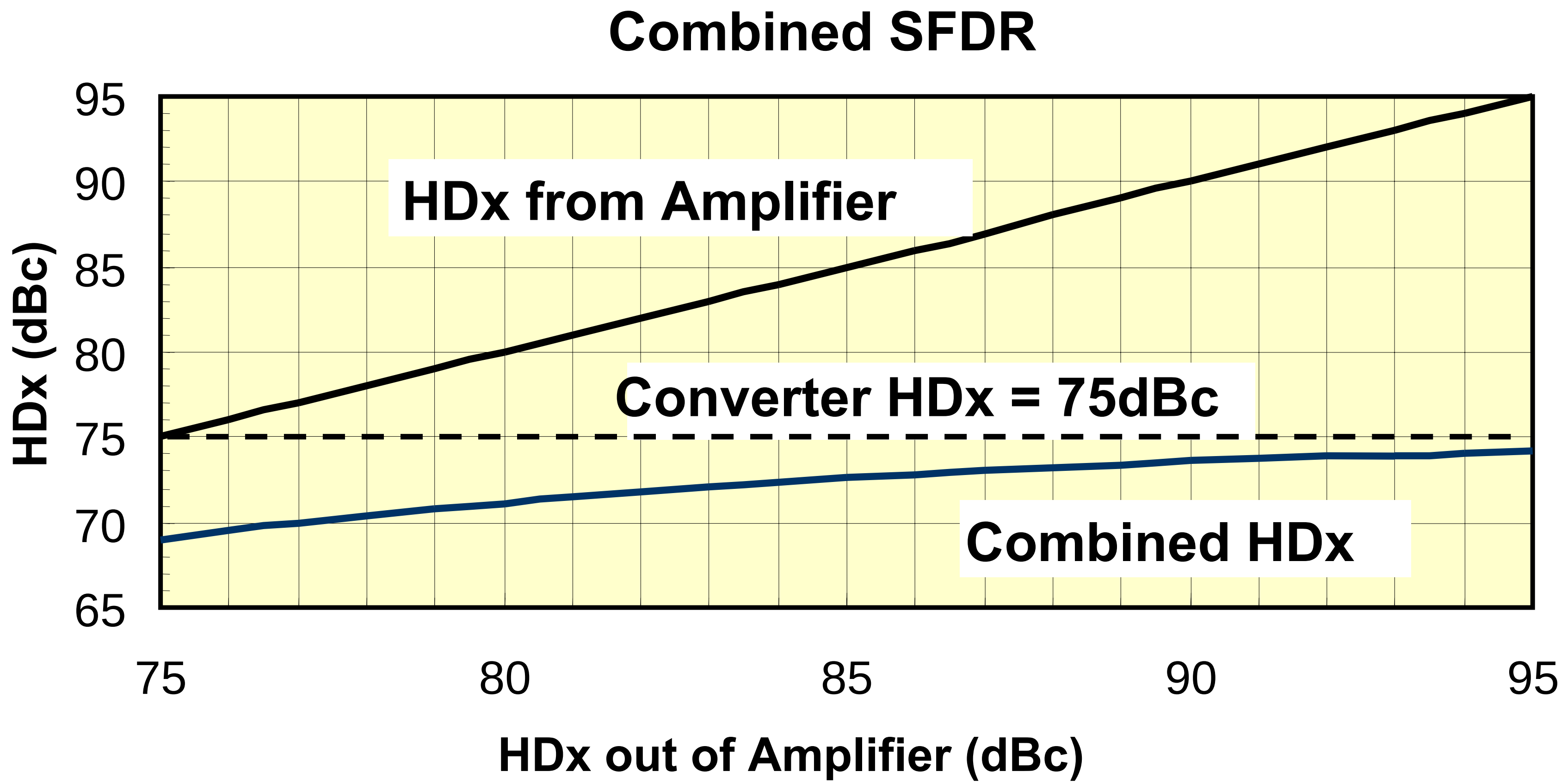
Adding Distortion

$$HDx_{System} \approx 20 \cdot \log\left(10^{\frac{HDx_{ADC}}{20}} + 10^{\frac{HDx_{Amp}}{20}}\right)$$

- A/D Converter and Amplifier Distortion add linearly
- As an example, for a 70dBc $HD2_{ADC}$ for the converter, the combined HD2 becomes →

$HD2_{OPA}$	$HD2_{System}$
65 dB	61.1 dB
70 dB	64 dB
75 dB	66.2 dB
80 dB	67.6 dB
85 dB	68.5 dB
90 dB	69.17 dB

Combined HDx for a target 75dBc HDx ADC Converter

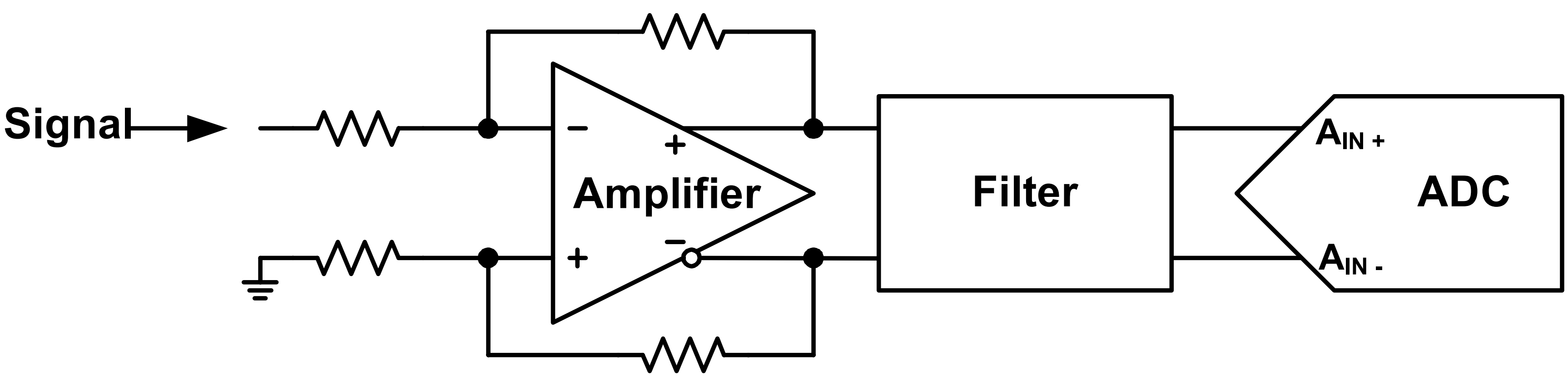


System SFDR

- The A-to-D conversion process of an ADC **may** lead to spurs that set the SFDR of the ADC that **are not either HD2 or HD3**
- In this case there is **no comparable amplifier term** to combine and the SFDR of the system is best taken as that of the ADC
- **If** SFDR of the ADC **is set by HD2 or HD3,** the SFDR can be estimated as the linear sum as shown

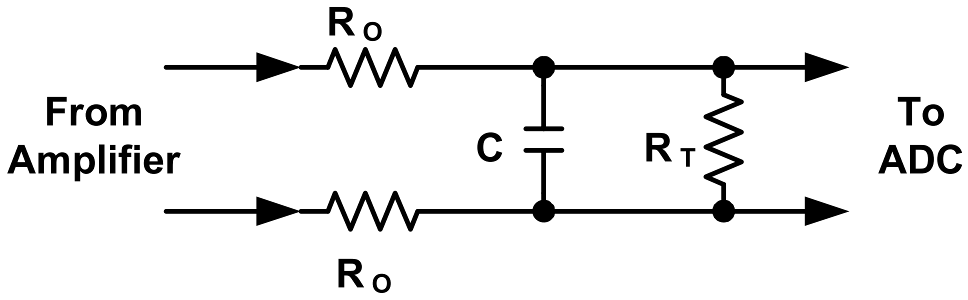
Amplifier and ADC Interface Options

- As high performance ADCs continue to improve their performance, the last stage interface, the filter from the final amplifier into the converter input becomes increasingly critical in the system design



1st Order Differential

RC Low-Pass Filter



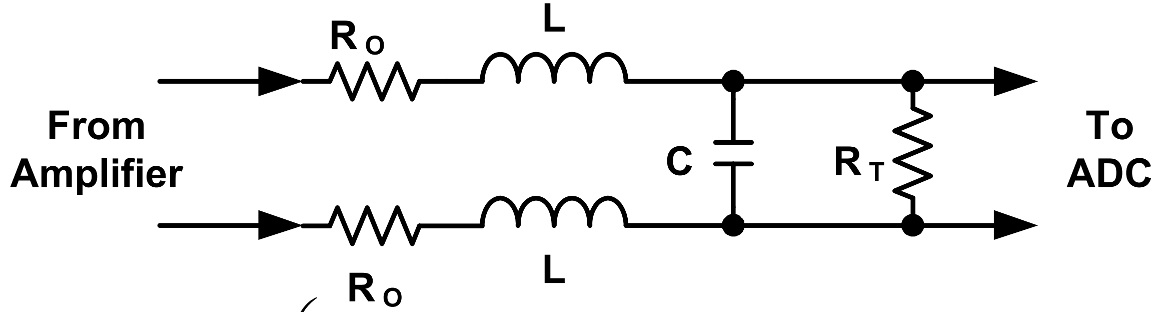
$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{R_T}{R_T + 2R_O} \right) \times \left(\frac{1}{1 + s\left(R_T \parallel 2R_O\right)C} \right)$$

If the effects of R_T are minimized, this can be simplified to:

$$\frac{V_{OUT}}{V_{IN}} \cong \frac{1}{1 + s2R_O C} \longrightarrow C = \frac{1}{2\pi f_O \times 2R_O}$$

2nd Order Differential

LRC Low-Pass Filter



$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{1}{LC}\right) \times \left(\frac{1}{s^2 + s\left(\frac{1}{R_T C} + \frac{2R_O}{L}\right) + \left(\frac{2R_O}{R_T + 2R_O}\frac{1}{LC}\right)} \right)$$

If we assume, as before, the effects of R_T are minimized, this formula can be simplified

But lets explore another less rigorous approach using basic definitions of Q and resonance

Simple 2nd Order Equations

- By definition, Q is set by the reactance and resistance in the circuit
- By definition, at resonance the inductive reactance and capacitive reactance are equal

If the effects of R_T are minimized, this leads to the equations at resonance (f_O), :

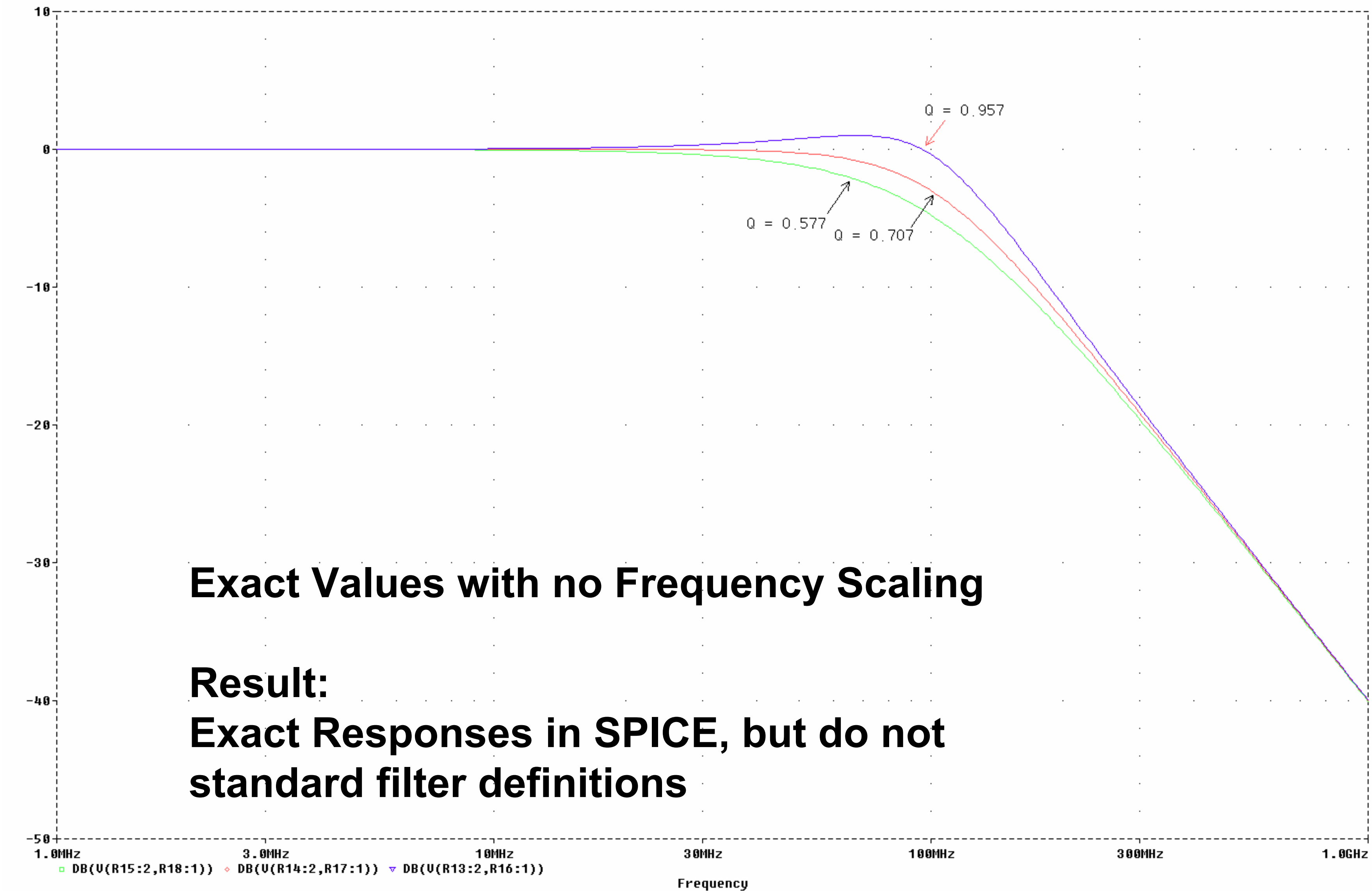
$$Q = \frac{X_L}{R_O} \qquad Q = \frac{X_C}{2R_O} \qquad 2X_L = X_C$$

Rearrange to Solve for L and C

$$L = \frac{Q \times R_O}{2\pi f_O} \qquad C = \frac{1}{Q \times 2\pi f_O \times 2R_O}$$

- Given the frequency of resonance and resistance, solve for inductance and capacitance

SPICE Simulation 0



Exact Values with no Frequency Scaling

Result:
Exact Responses in SPICE, but do not standard filter definitions

Frequency Scaling and Q

- Q is the quality factor and is fairly commonly understood. The most obvious impact is the peaking near the cut-off frequency
- Frequency scaling factor (FSF) may be new to you
- FSF is used to scale the cut-off frequency of the filter to meet the classic definitions;
  - for example Butterworth and Bessel define the cut-off frequency as the -3dB point and Chebyshev defines it as the frequency where the response first falls out of the ripple band
- This means value of f_O is scaled by FSF for use in the equations above in order to design a filter that meet standard definitions

Frequency Scaling and Q

- A good filter book will list the zeroes and the coefficients of the particular polynomial being used to define the filter

frequency scaling factor: $$FSF = \sqrt{\text{Re}^2 + |\text{Im}|^2}$$

quality factor: $$Q = \frac{\sqrt{\text{Re}^2 + |\text{Im}|^2}}{2\,\text{Re}}$$

Re is the real part of the complex zero pair, and Im is the imaginary part

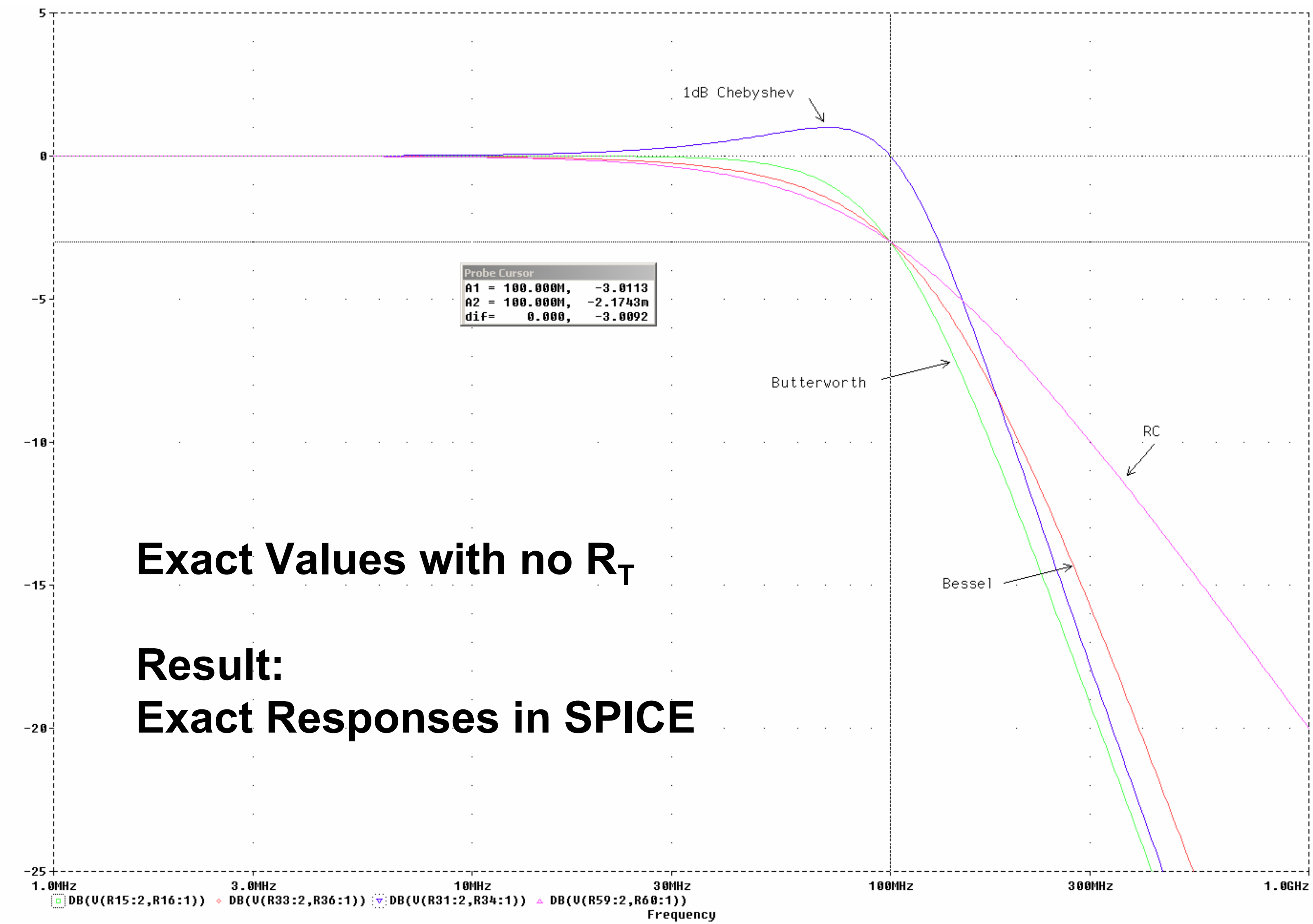
FSF and Q for 3 Classic Filters

Filter Type	FSF	Q
1dB Chebyshev	1.0500	0.9565
Butterworth	1.000	0.7071
Bessel	1.2736	0.5773

Given R_O = 50Ω and 100MHz cut-off frequency, L and C values as follows:

Filter Type	f_O x FSF (MHz)	Q	R (ohms)	L (nH)	C (pF)
1dB Chebyshev	105	0.9565	50	72.49	15.85
Butterworth	100	0.707	50	56.26	22.51
Bessel	127	0.5773	50	36.06	21.64

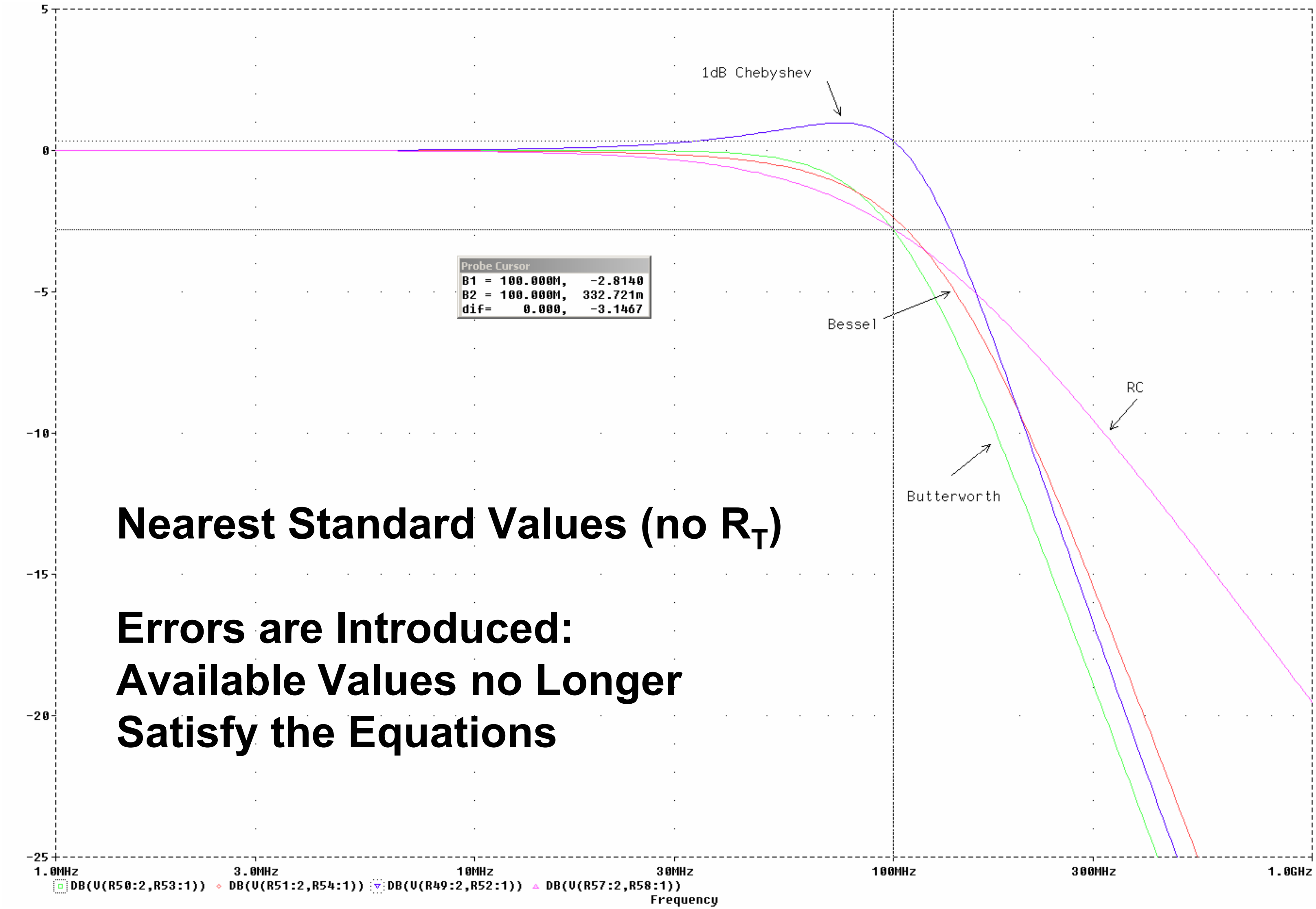
SPICE Simulation 1



Exact Values with no R_T

Result:
Exact Responses in SPICE

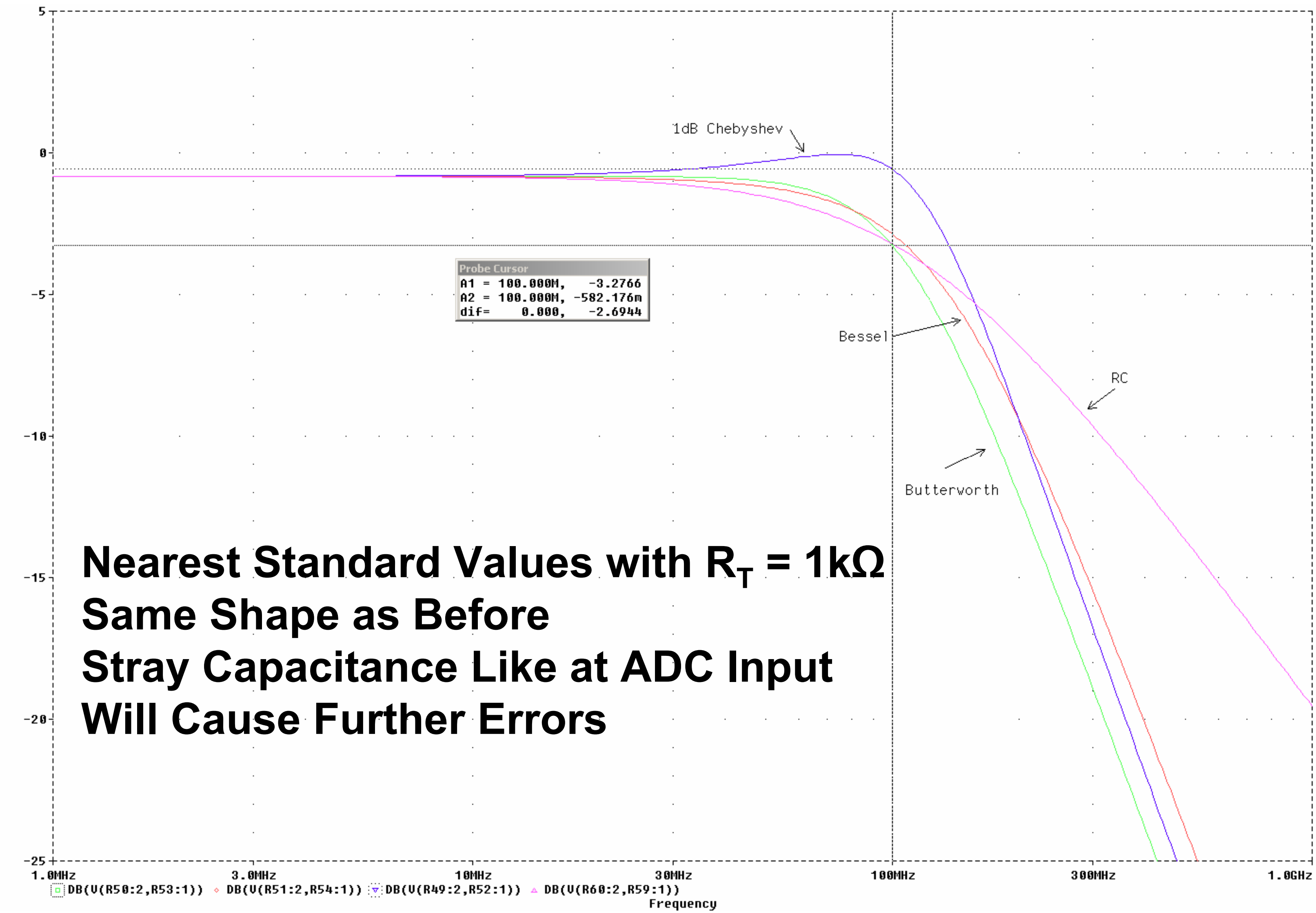
SPICE Simulation 2



Nearest Standard Values (no R_T)

Errors are Introduced: Available Values no Longer Satisfy the Equations

SPICE Simulation 3

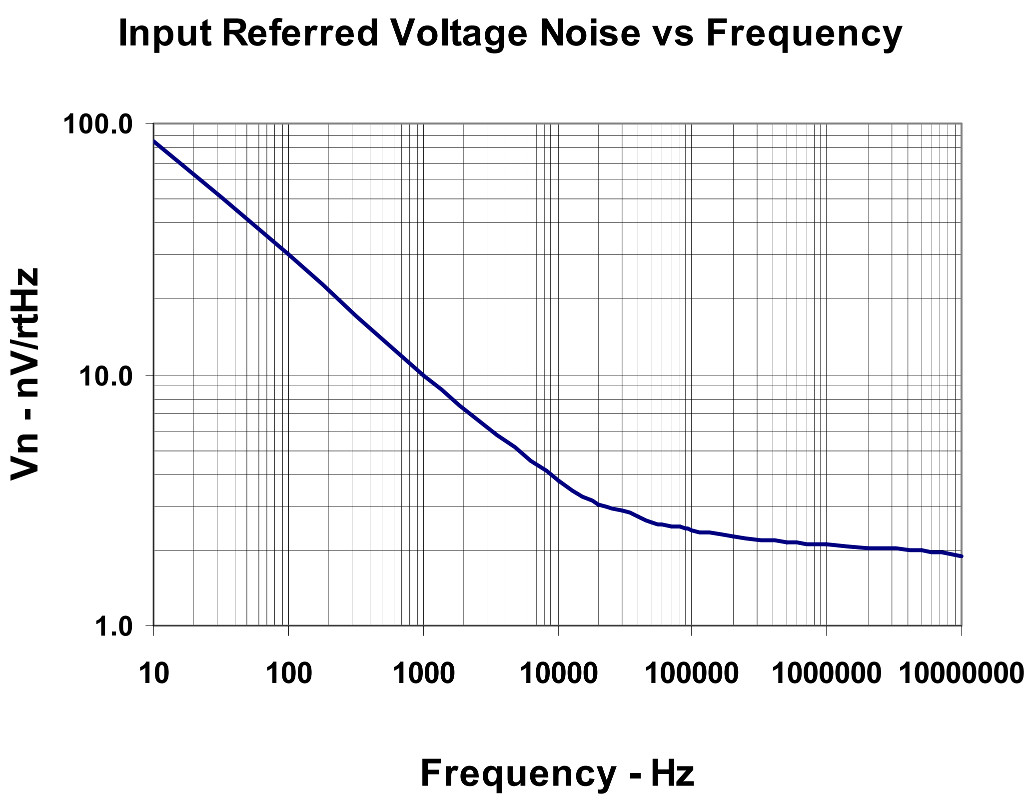


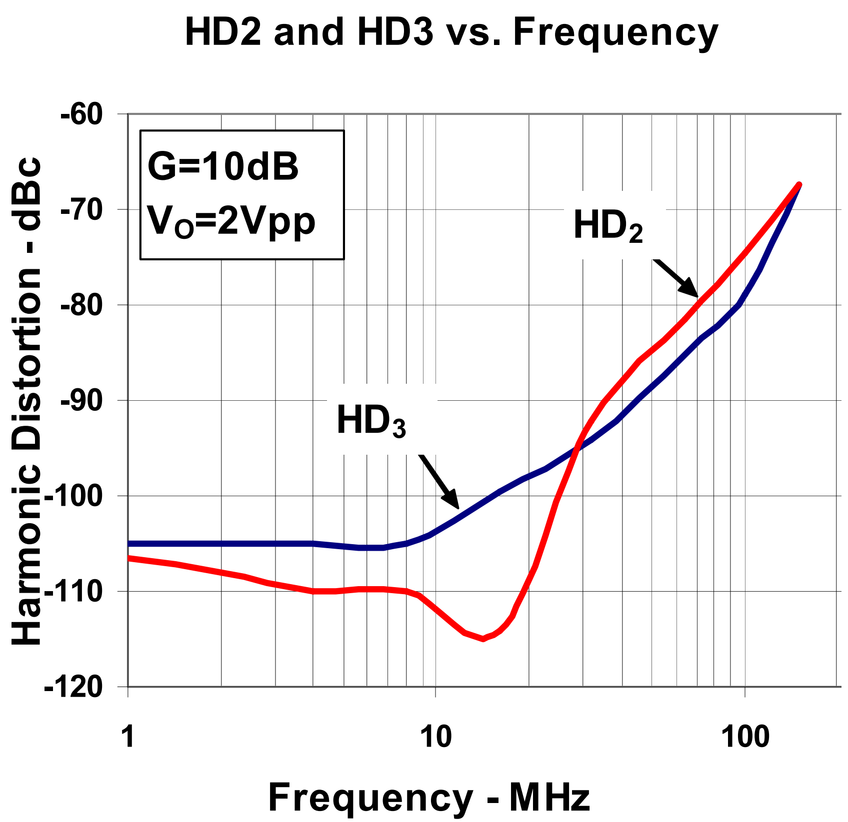
Nearest Standard Values with R_T = 1kΩ
Same Shape as Before
Stray Capacitance Like at ADC Input
Will Cause Further Errors

Amplifier to ADC Design Example: THS4509 + ADS5413-11

1. Data sheet specification for each part
2. Lab measurements of each part separately
3. Circuits
4. Comparison of actual combined performance versus predicted performance

THS4509 Noise and Distortion





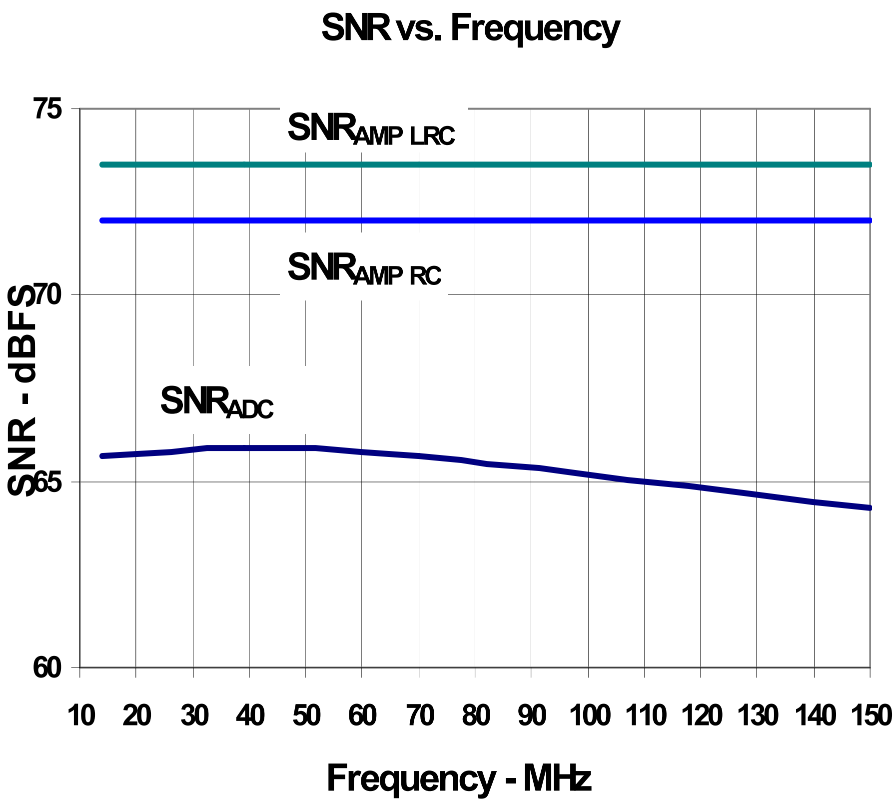
Information from Data Sheet

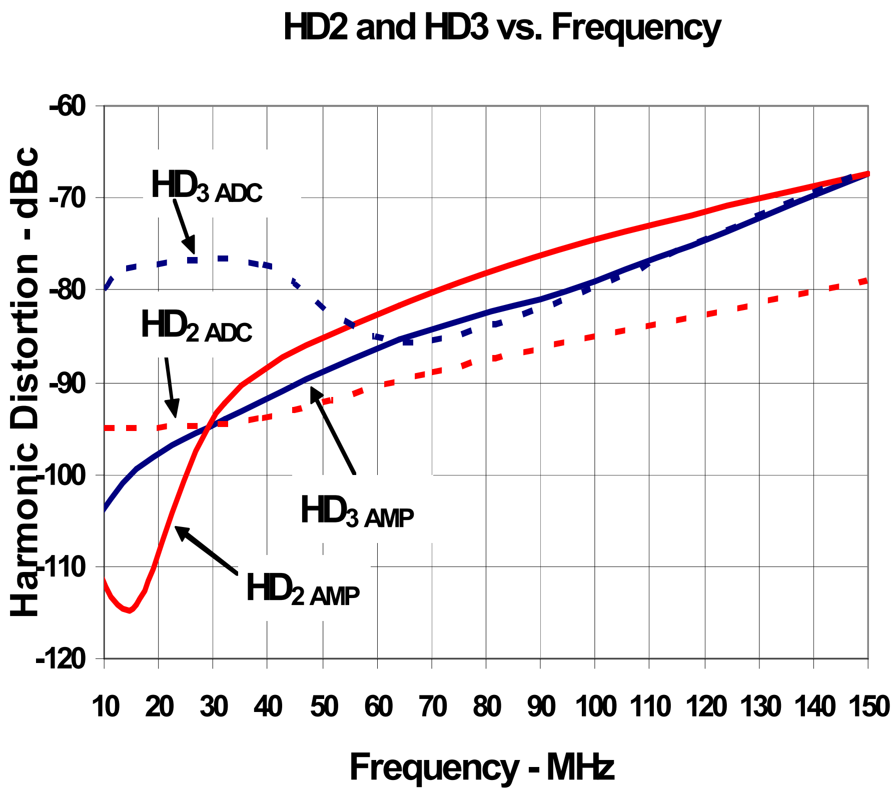
ADS5413-11 Noise and Distortion

SNR	Signal-to-noise ratio	f_{IN} = 14 MHz	61.5	65.7	dBFS
		f_{IN} = 39 MHz		65.9	
		f_{IN} = 70 MHz		65.7	
		f_{IN} = 150 MHz		64.3	
		f_{IN} = 190 MHz		63.9	
		f_{IN} = 220 MHz		63.3	
HD2	Second order harmonic	f_{IN} = 14 MHz		95	dBc
		f_{IN} = 39 MHz		94	
		f_{IN} = 70 MHz		89	
		f_{IN} = 150 MHz		79	
		f_{IN} = 190 MHz		84.5	
		f_{IN} = 220 MHz		72	
HD3	Third order harmonic	f_{IN} = 14 MHz		77.6	dBc
		f_{IN} = 39 MHz		75.4	
		f_{IN} = 70 MHz		85.5	
		f_{IN} = 150 MHz		70.5	
		f_{IN} = 190 MHz		68.3	
		f_{IN} = 220 MHz		77.6	

Information from Data Sheet

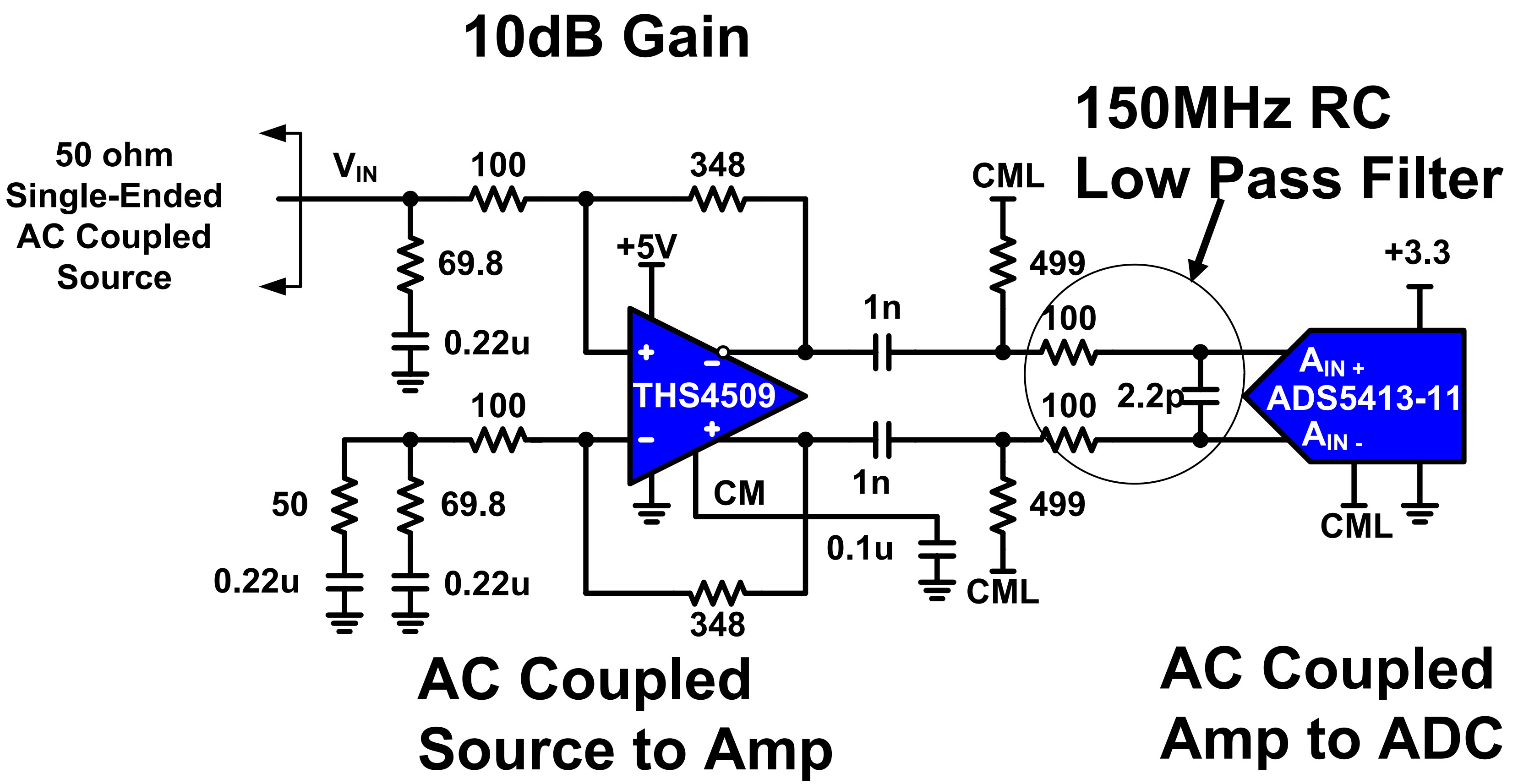
THS4509 and ADS5413-11



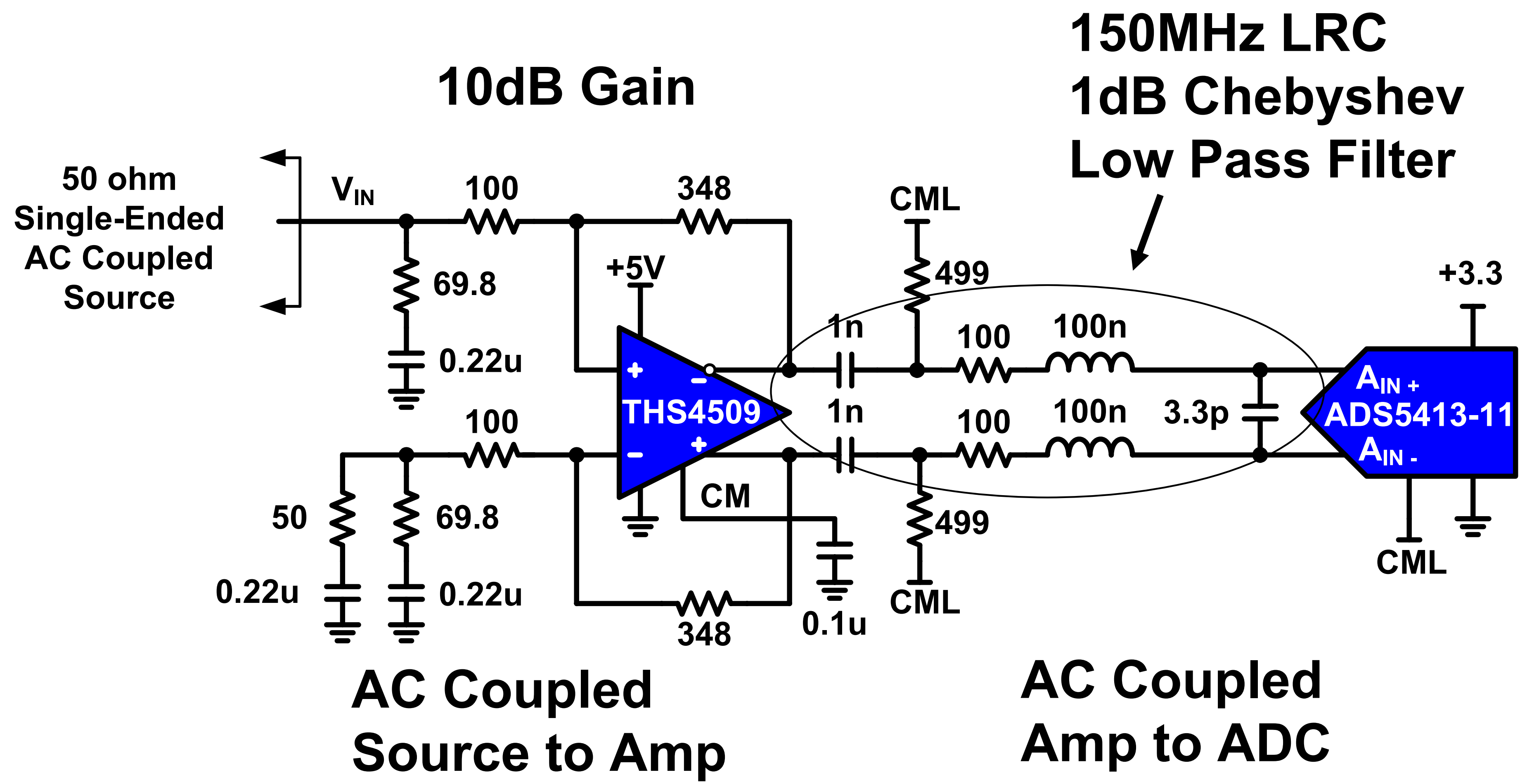


ADS5413-11 measured on EVM with transformer input
THS4509 distortion measured on EVM with 1k output load; SNR calculated

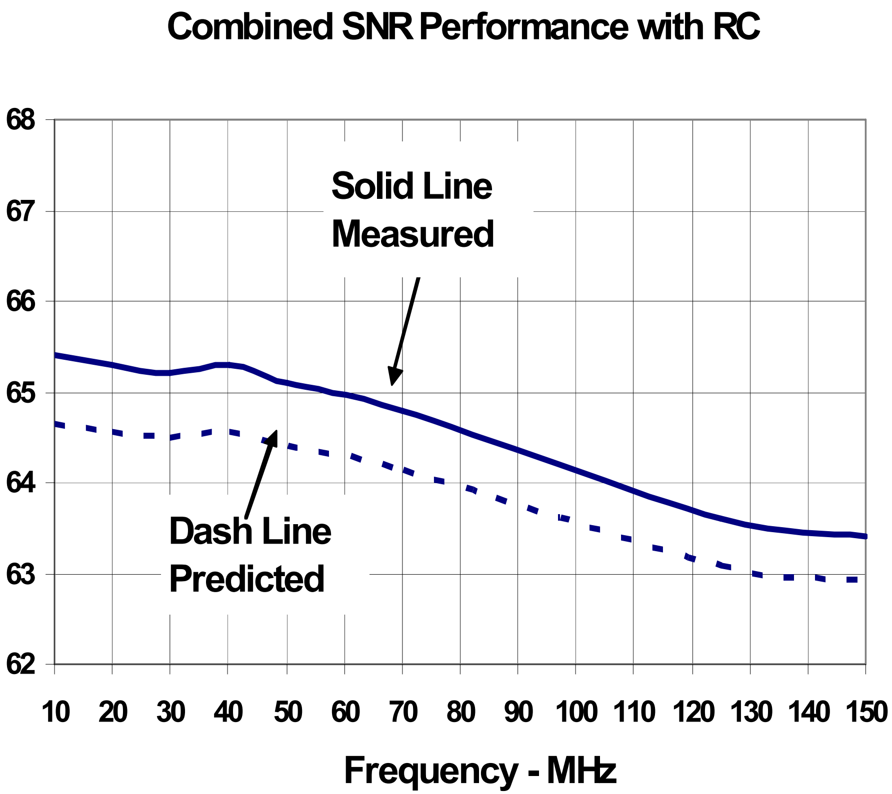
THS4509 + ADS5413-11: Circuit 1

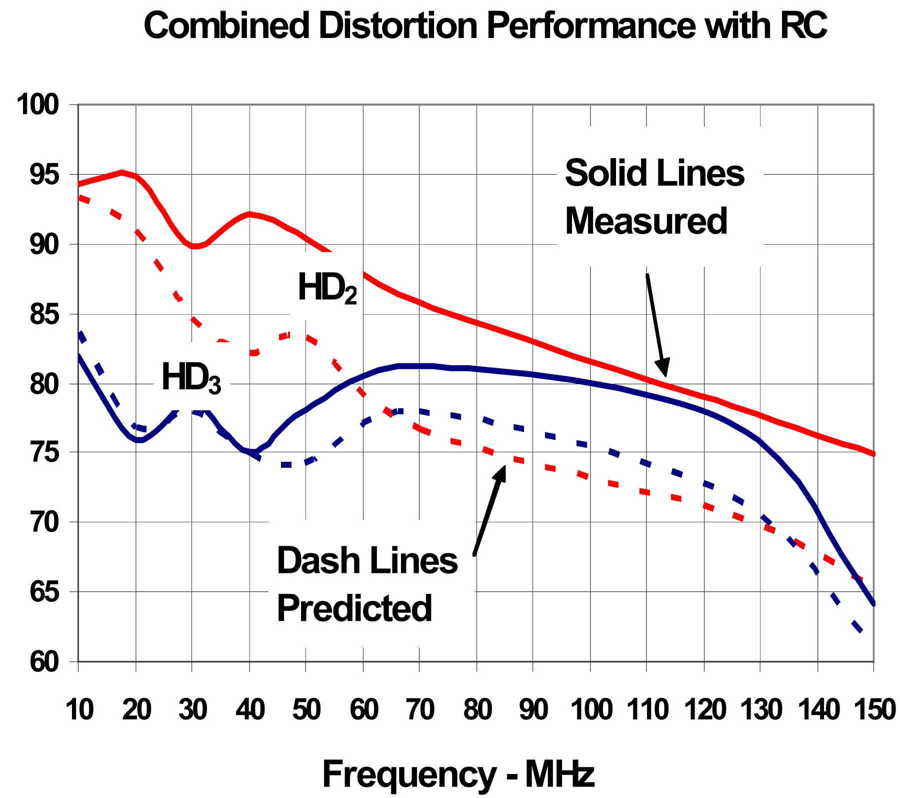


THS4509 + ADS5413-11: Circuit 2



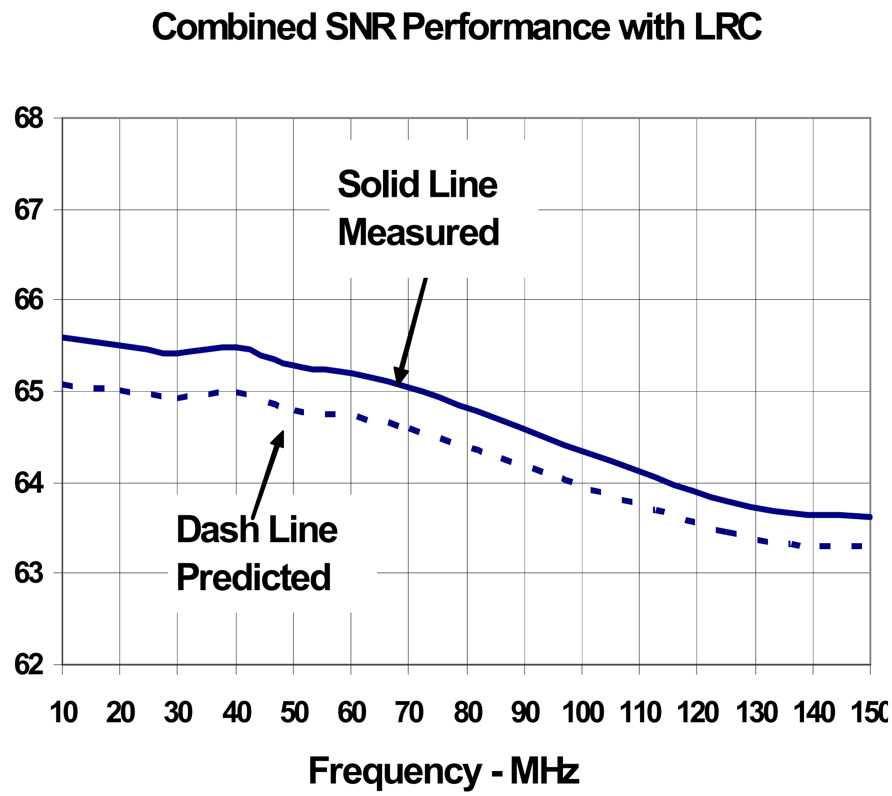
THS4509 and ADS5413-11

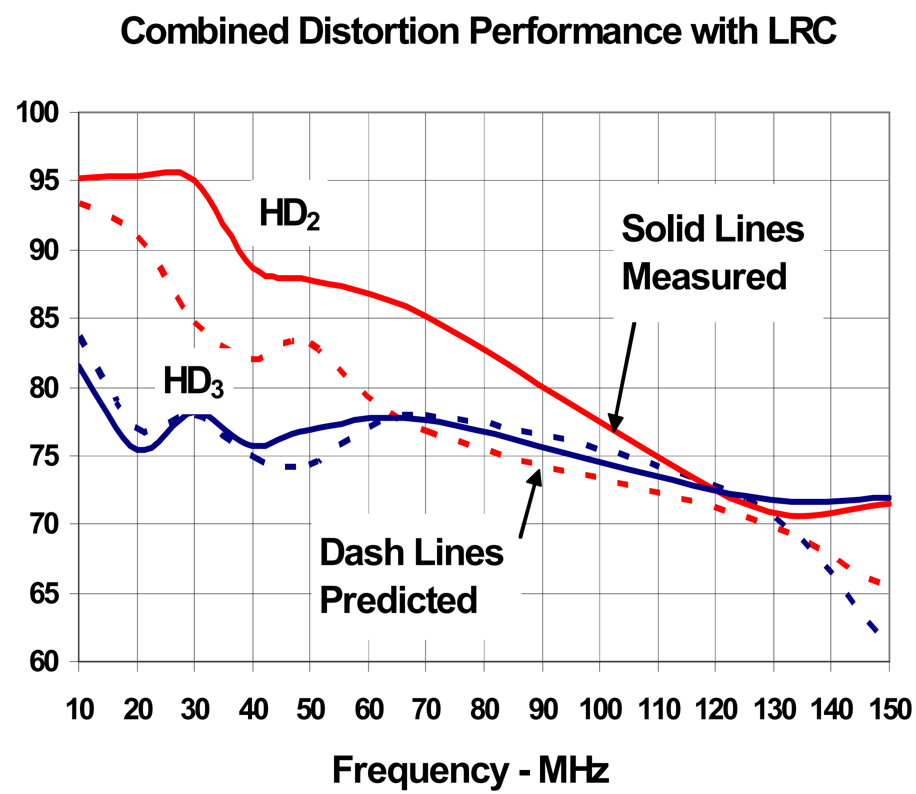




Combined Performance Circuit 1: RC

THS4509 and ADS5413-11





Combined Performance Circuit 2: LRC

Conclusion

- A variety of circuit topologies are available to convert single-ended input to differential
  - AC coupling allow the greatest freedom in choice of amplifiers and power supply voltage
  - Fully differential amplifier allows DC coupling
- System performance can be analyzed knowing the performance of the individual components
- Passive differential 1st order RC and 2nd order RLC low-pass filters can be designed with simple equations
  - 2nd order filters will provide better SNR performance because of faster role off, but may lead to lower SFDR
- The actual system needs to be built and tested to validate system performance.