Four Voltage References, an ADC and MSP430

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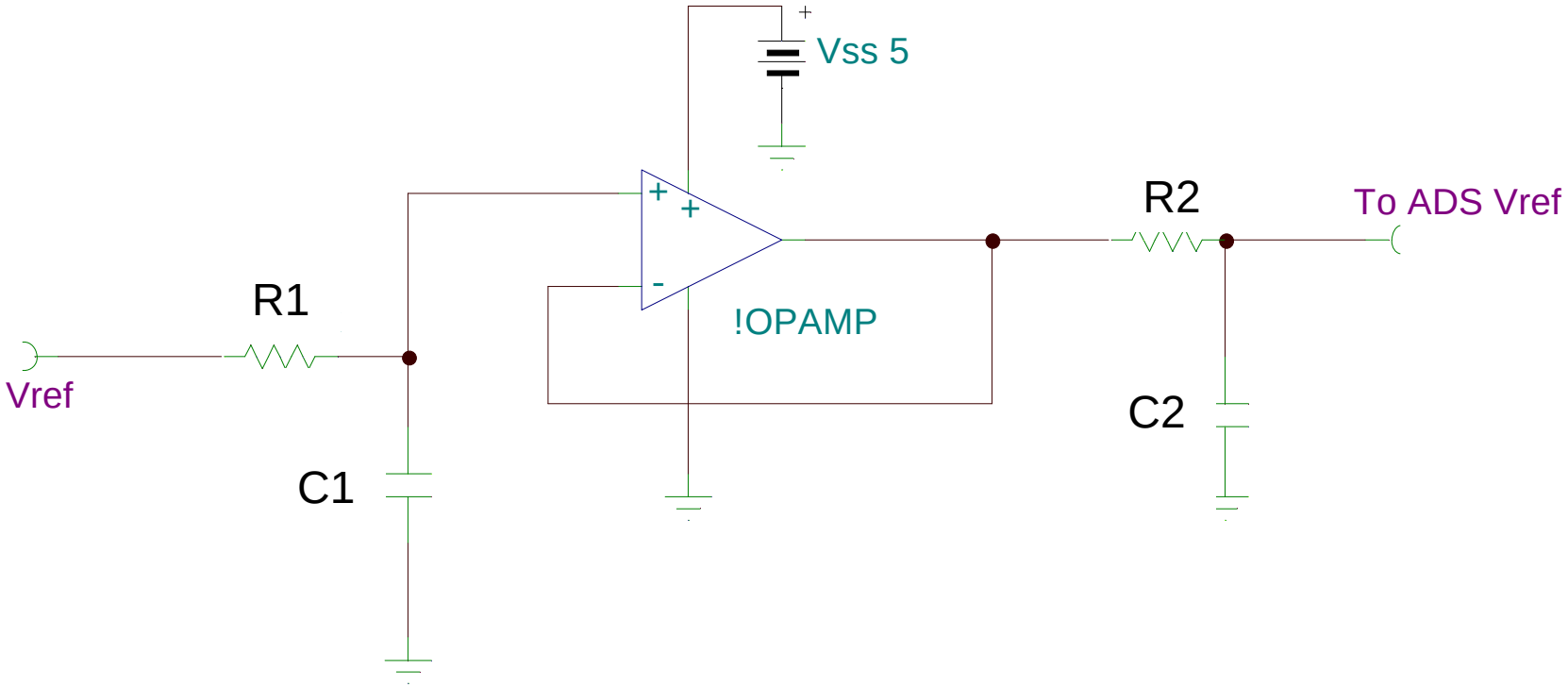
Motivation

- *Total Solution Concept*
- *Application section of datasheets*
- *New REF products from TI*
- *Greed*
  - *Product Recognition*
  - *Increased Revenue*

Experiment

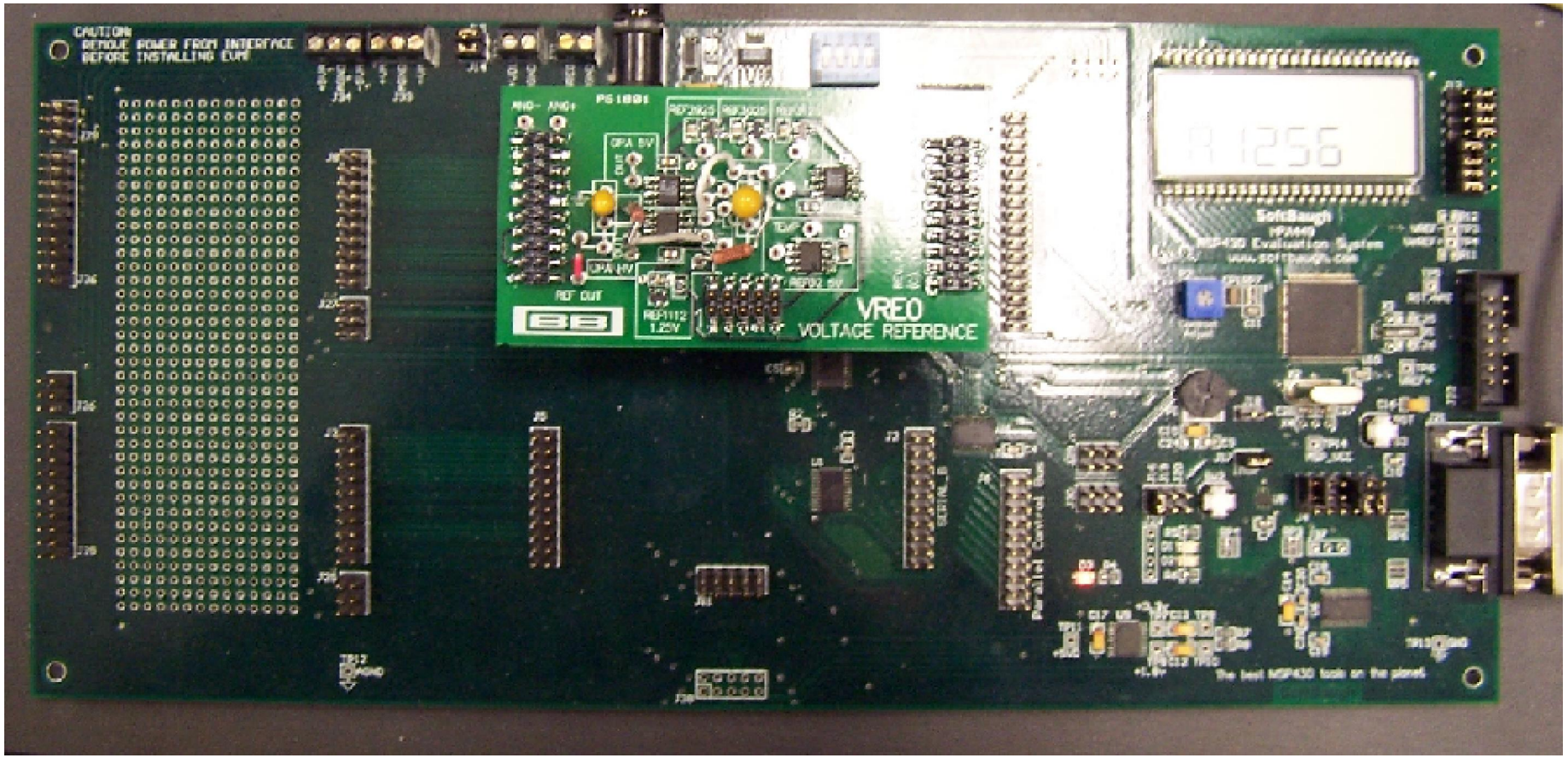
- *Verify setup/measurements*
- *Evaluate TI REFs with ADS1256*
- *Compare different TI REF results*
- *Suggest the optimal circuitry*

Basic Setup

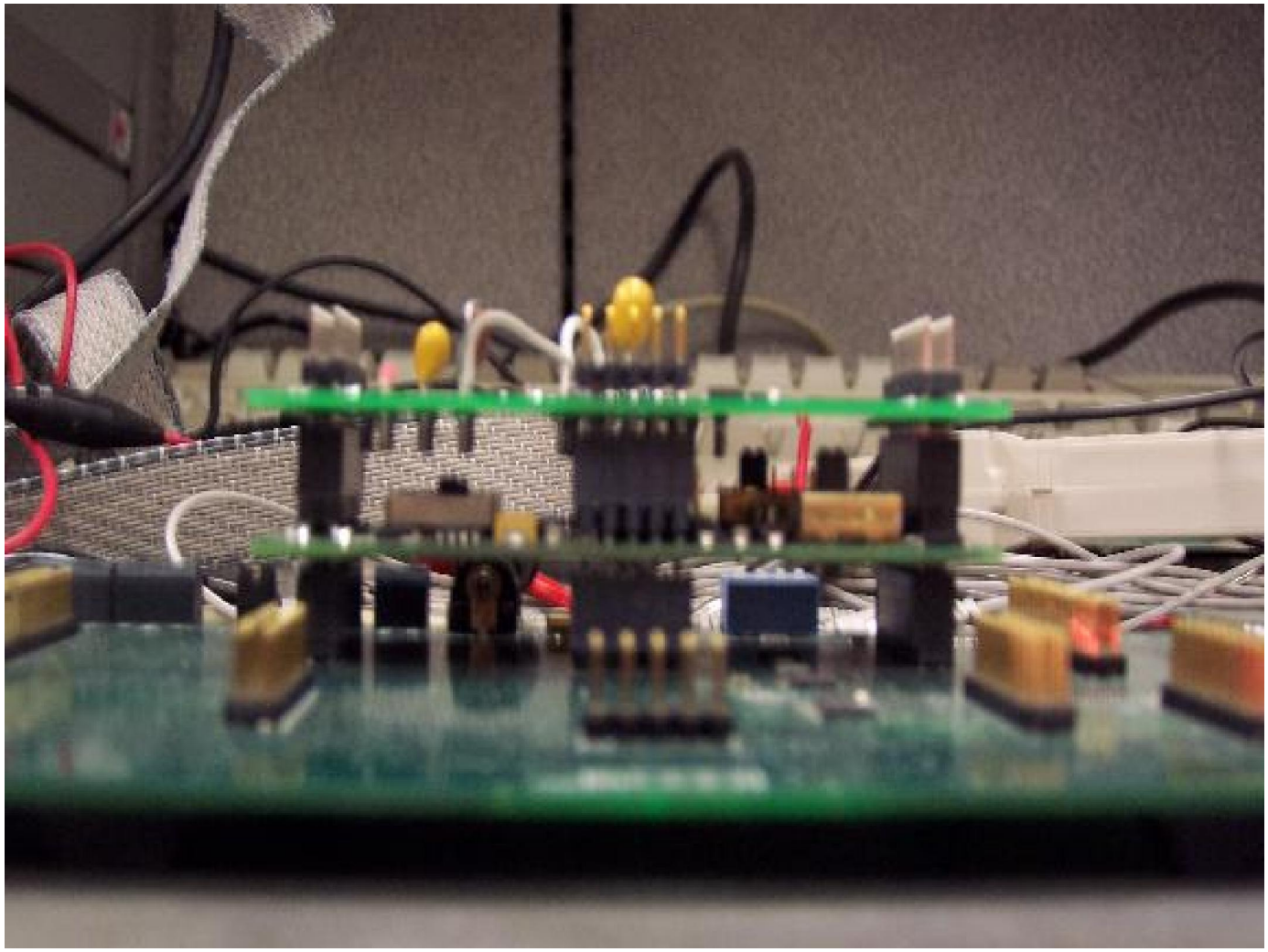


ADS1256, PGA=1, Vref=2.5V

Board



Board (side view)



Considerations

- *Low Noise*
- *Long term stability*
  - *Time*
  - *Temperature*

Experiment Design

R1	*C1*	*OPA*	*R2*	*C2*	*RMS noise free bits*
…..	*…..*	*335*	*100*	*10u*	
		227	*100*	*10u*	

Additional considerations:

Vin amplitude, f_s (data output rate)

Confirm the Setup

Table 2. Effective Number of Bits (ENOB, rms) with Buffer On

DATA RATE (SPS)	PGA						
	1	2	4	8	16	32	64
50	23.9	23.6	23.0	22.5	21.8	21.1	20.3
60	23.8	23.4	22.9	22.4	21.7	21.0	20.2

REF	*R1*	*C1*	*OPA*	*R2*	*C2*	*RMSnfb*
1004	*10k*	*47u*	*227*	*100*	*10u*	*23.8*

VIn=0V, shorted inputs,

Results

REF	R1	C1	OPA	R2	C2	RMSnfb
1004	------	------	OPA335	100	10u	20.7
1004	10k	220u	same	same	same	22.3
1004	10k	47u	same	same	same	**22.4**
3025	same	same	same	same	same	20.8
3125	same	same	same	same	same	20
1112*	same	same	same	same	same	**22.1**
1004	same	same	OPA227	same	same	**22.4**

* OPA in a gain of 2

Vin=2.5V, data output rate = 60Hz,

Conclusions

- *On ADS1256 one needs external buffer*
  - *Input impedance 18k*
- *Noise-wise OPA227 and OPA335 equal*
  - *However, we tried at T=25 °C*
- *REF1004 and REF1112 similar results*
- *REF3xxx family good for lower precision*
- *RC (settling time vs. noise) trade off*

MSP430

- *Has 12 bit ADC (ADC12)*
- *Has Vref (2.5V or 1.5V)*
  - *800uA max*
  - *100ppm/ °C max*
  - *4% initial accuracy*

- TI REFs:
  - 8uA -110 uA max current
  - 15 -100ppm/ ° C
  - 2.048/2.5/3.0V/3.3V 0.2%

Results

REF	R1	C1	Noise RMS bits
Internal (2.5V)	------	------	~3.1
1004 – 2.5V	100	47u	~3.0
3025	10k	47u	**~2.7**
3125	same	same	~2.7
1004	same	same	~2.7
3125	100	same	~3.0
3025	same	same	**~3.0**
1112	same	same	**5.5**

Conclusions – Part II

- *External REFs improve performance*
  - *Lower noise*
  - *Lower supply current*
- *REF1112 can not be used with MSP430*
  - *VeRef is 1.4V min!!!!!*

Summary

- *Built tools for evaluations*
- *Got preliminary results*
- *Will work on other ADCs and MSP430*
  - *SARs, Delta-Sigma*
- *Will improve datasheets*
- ***Support customers** with optimal solution*

Thank You

Amplifier to A/D Interface Study

Or…that short task
that will not go away

Bill Klein

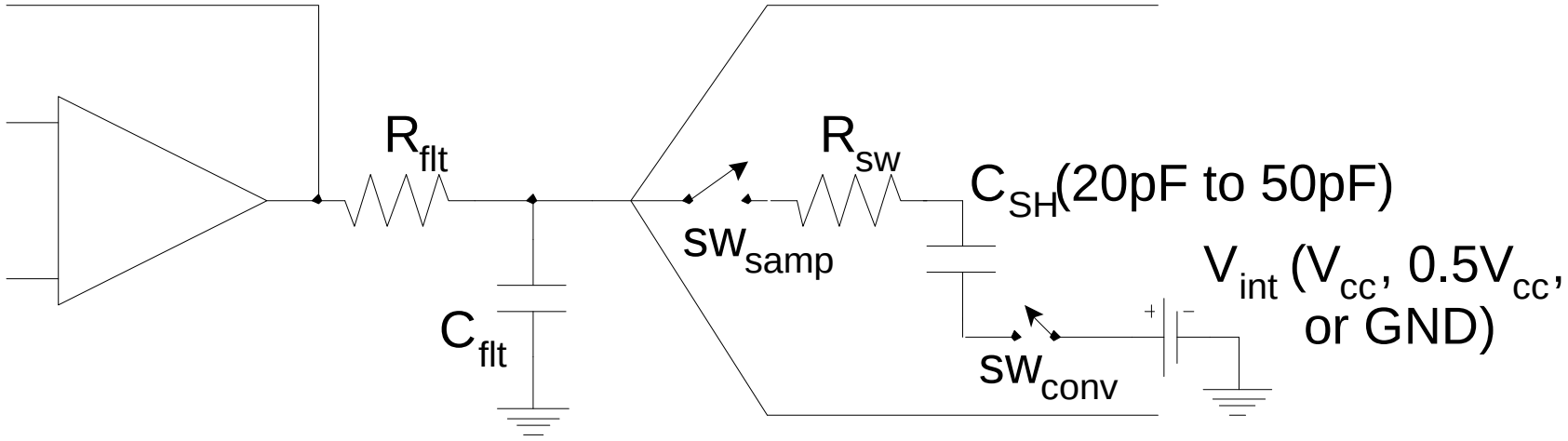
Senior Applications Engineer

Miro Oljaca

Strategic Marketing:
Motor Control

With major contributions from: Tom Hendrick, Tim Green, Rick Downs, Rod Burt, Bob Benjamin, Bernd Rundel, Bruce Trump, Dennis Goeke, Pat Highton

The Interface Circuit



Op Amp

CMV Range, V_{OS} vs CMV

RR Out-Swing to the rail

Slew Rate, Signal BW,

Load Transient, Settling Time,

Output Impedance,

Filter

Charge Bucket

Filtering,

C_{load} Isolation,

A/D

Acquisition Time

Input Circuit Parameters

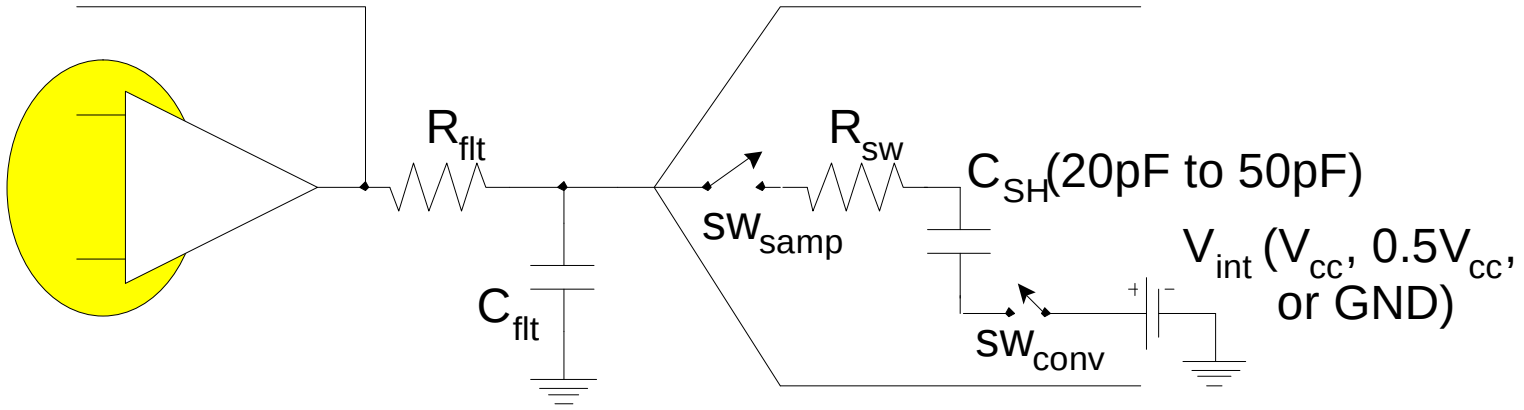
Initial Voltage on C_{SH}

LSB Size

- *Signal range:*
  - *+/-10V is a 20V range*
    - *12 bits: 20V/4,096 = 4.88mV per LSB*
    - *16 bits: 20V/65,536 = 305µV per LSB*
  - *+5V range*
    - *12 bits: 5V/4,096 = 1.22mV per LSB*
    - *16 bits: 5V/65,536 = 76.2µV per LSB*
    - *24 bits: 5V/16,777,216 = 298nV per LSB*
  - *+3.3V range*
    - *12 bits: 3.3V/4,096 = 806µV per LSB*
    - *16 bits: 3.3V/65,536 = 50.4µV per LSB*
    - *24 bits: 3.3V/16,777,216 = 196nV per LSB*

Op Amp Input Concerns

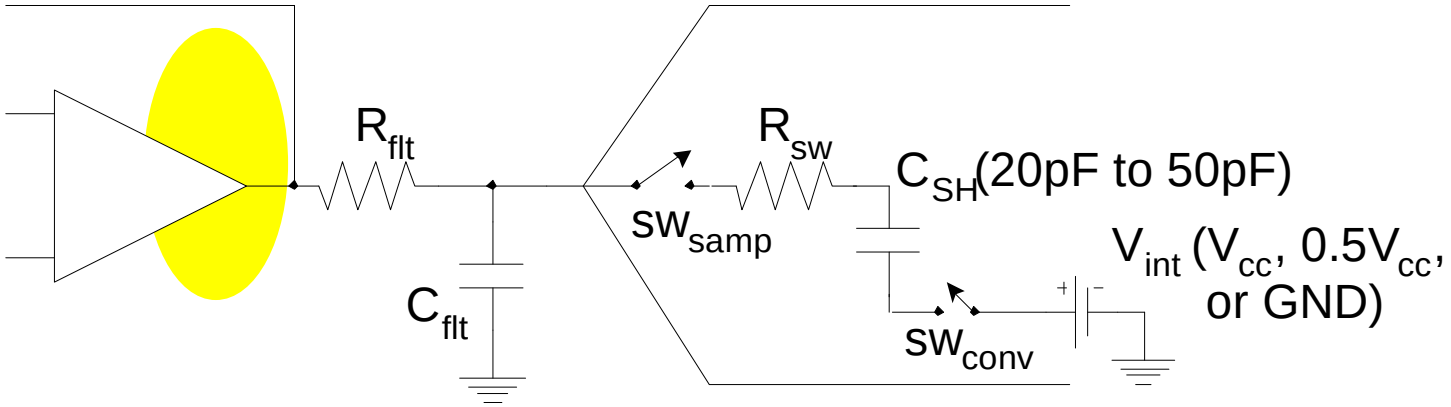
See Appendix



Rail-to-Rail Input

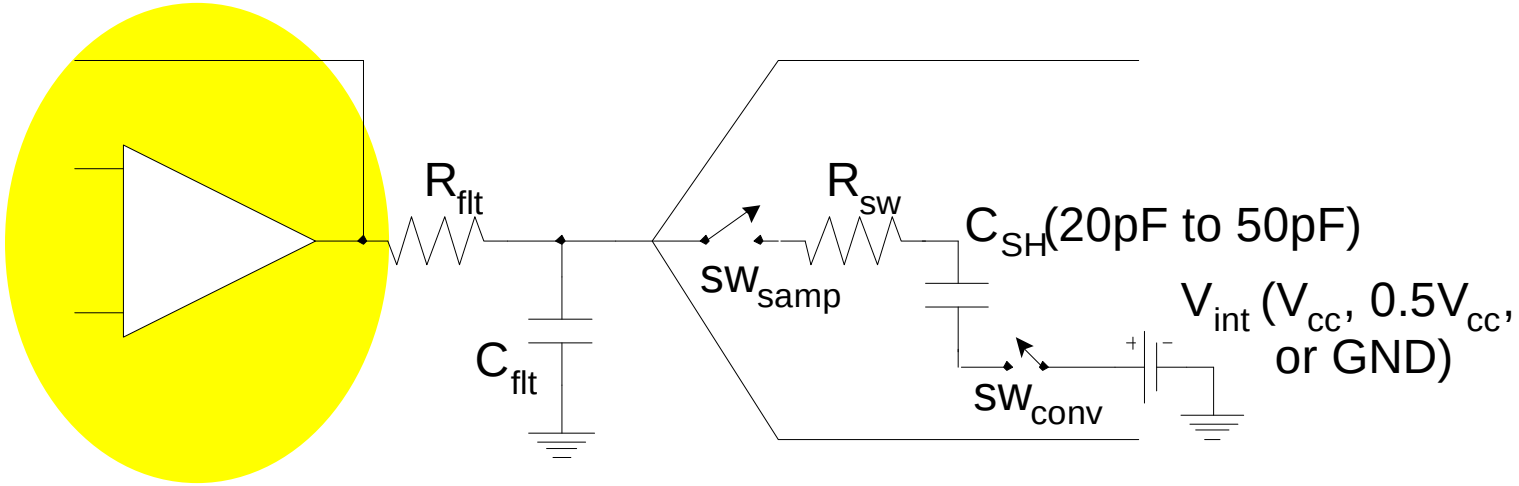
Output Stage Concerns

See Appendix



Rail-to-Rail Output

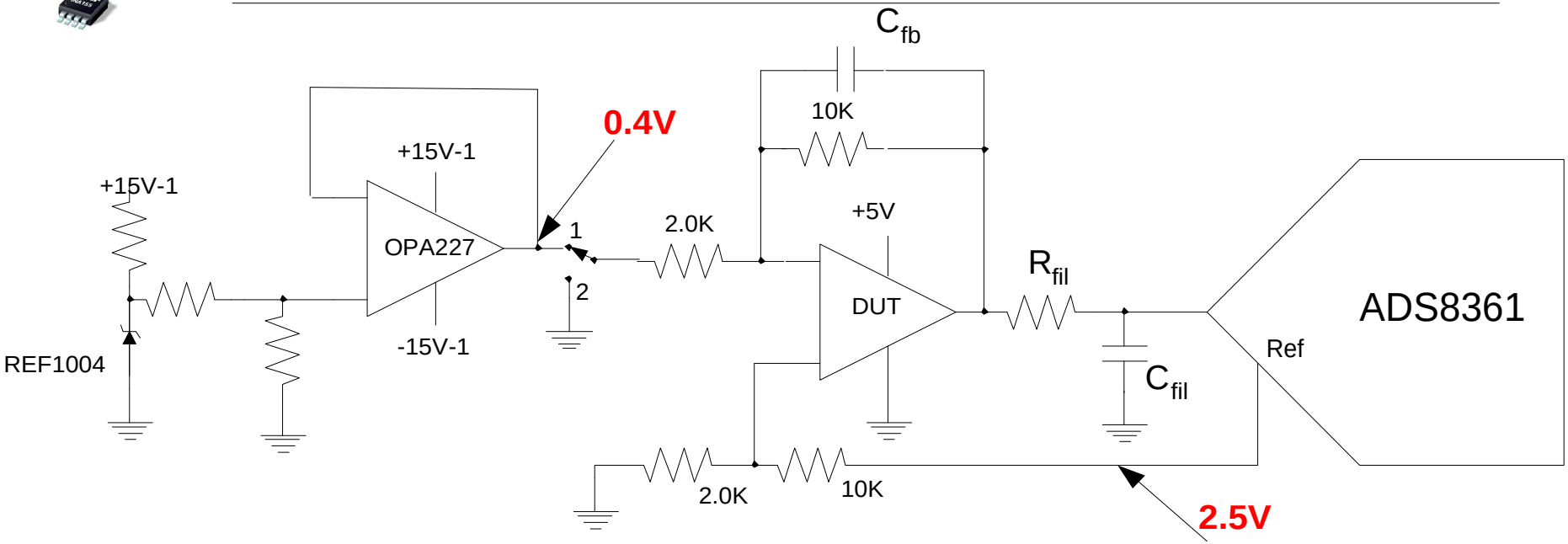
How Fast does that Op Amp Settle

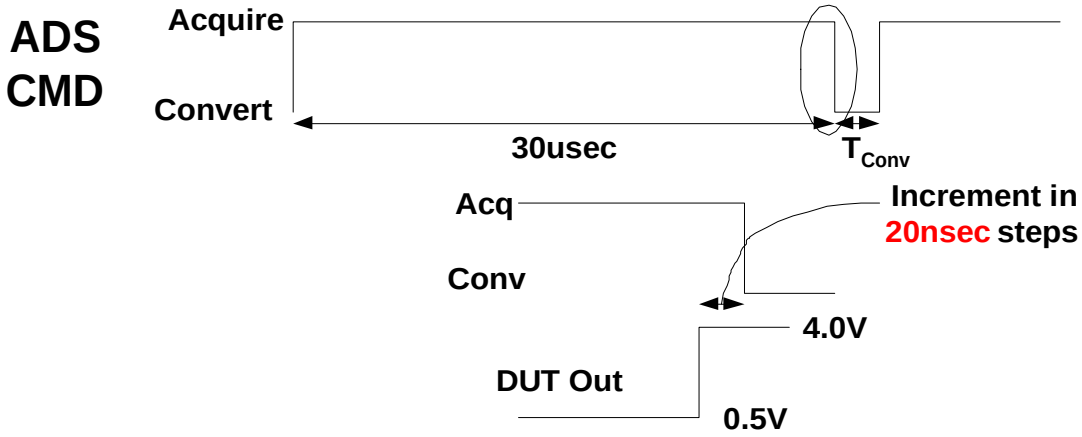


What Settling Time?

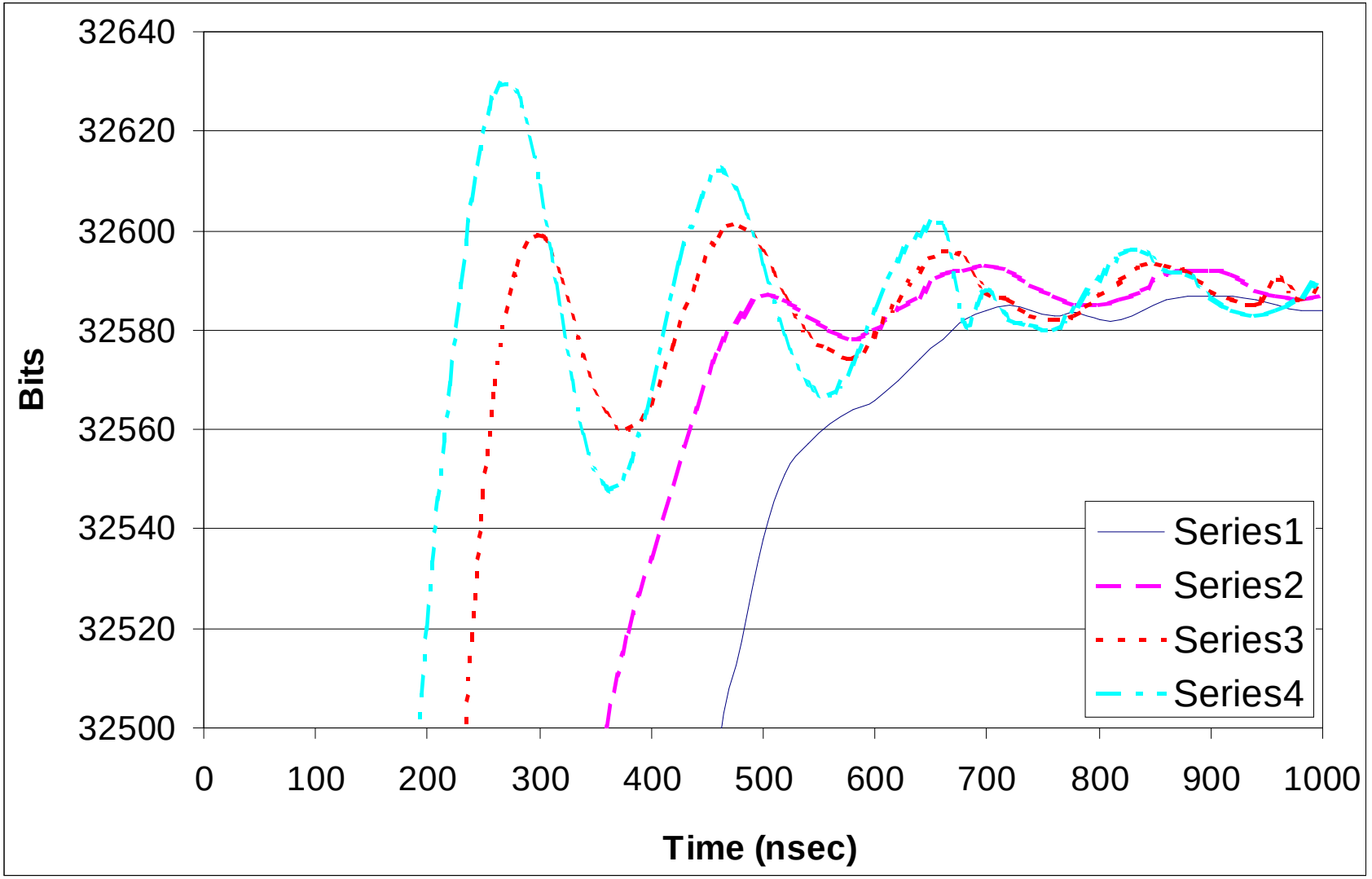
- *Think of a linear voltage regulator, there are **TWO** Settling Times.*
  - *Line Transient*
  - *Load Transient*
- ***Same** applies here.*
- *Data sheets report settling time to 0.01% at best.*

The Test Circuit

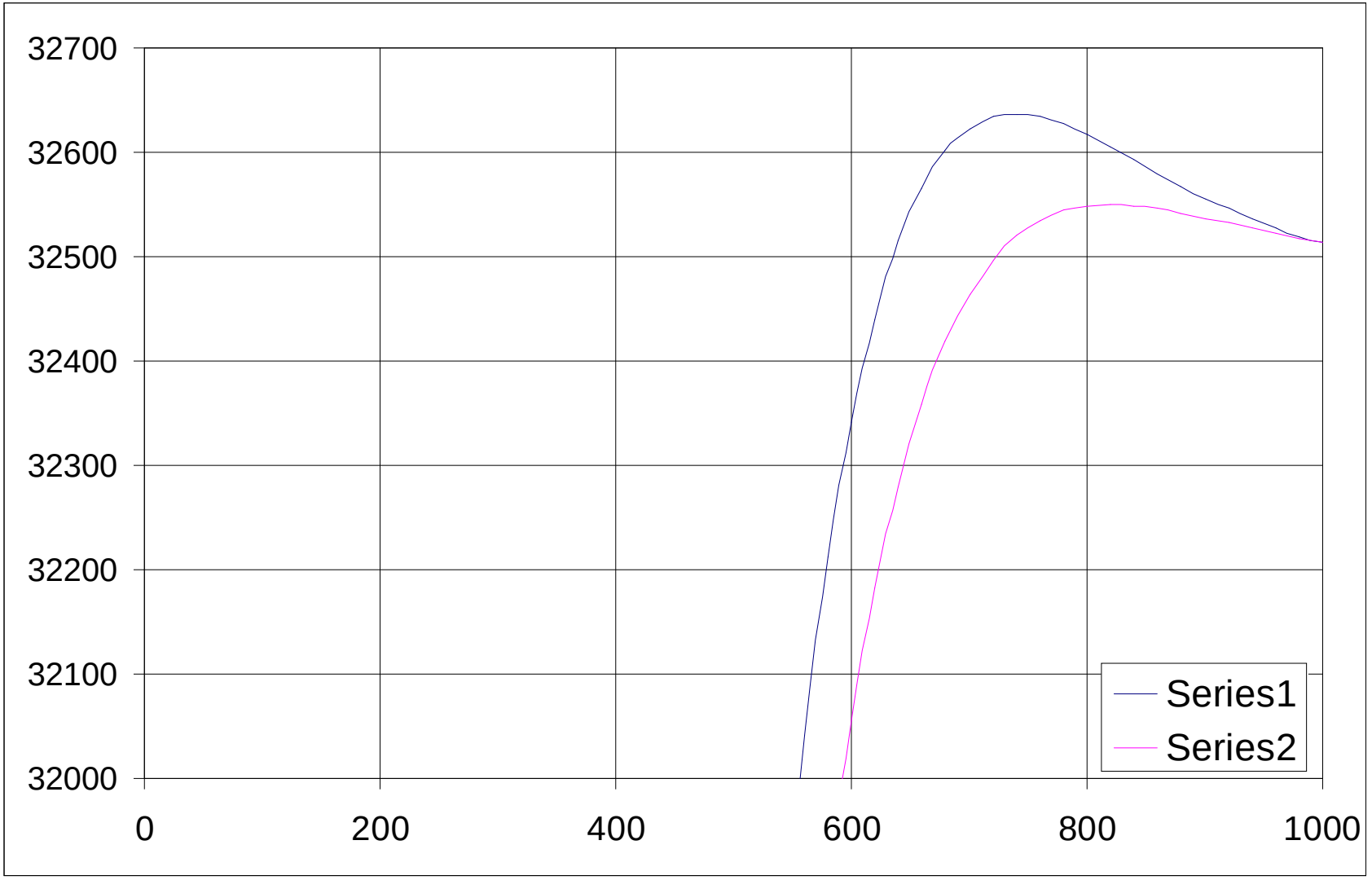




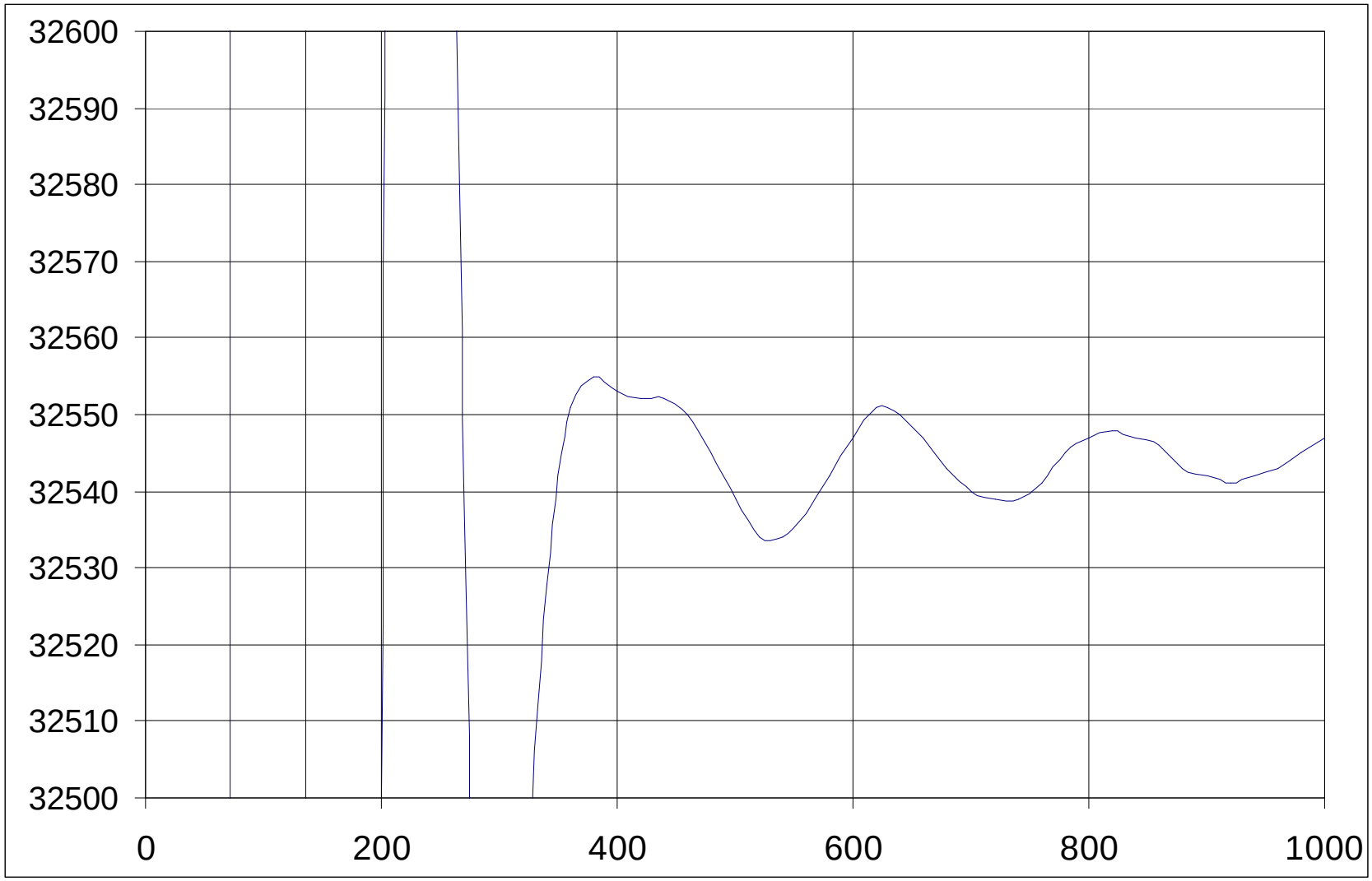
OPA300



OPA340



OPA350



Line Transient Becomes

- *Response to change in input signal*
- *Includes Slew Rate.*
- *Op Amp data sheets MAY address Settling Time to 0.01%*
- *But we need 0.0007629% for a 16 bit system*

Required Settling Time

Number of bits	0.5LSB
10	0.0488281%
12	0.0122070%
14	0.0030518%
16	0.0007629%
18	0.0001907%
20	0.0000477%
22	0.0000119%
24	0.0000030%

See appendix for calculations

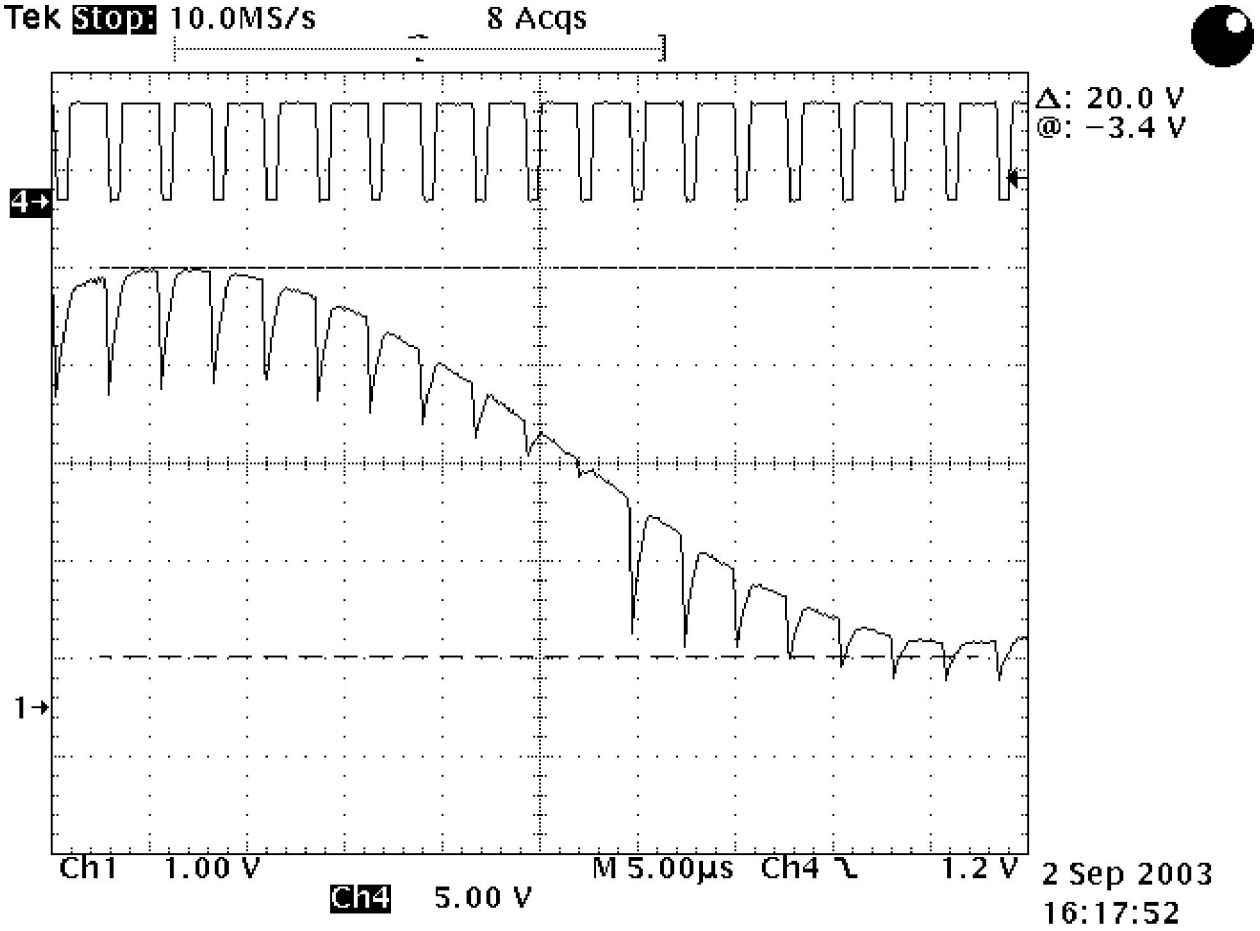
Load Transient is UNKNOWN

- *We know the load is the input capacitance of the A/D*
- *We do NOT know the starting voltage.*
  - *Possible voltages: GND, Mid-Rail, Random*
  - *Not given in data sheet*
- *The Op Amp data sheet does NOT even mention this settling time.*

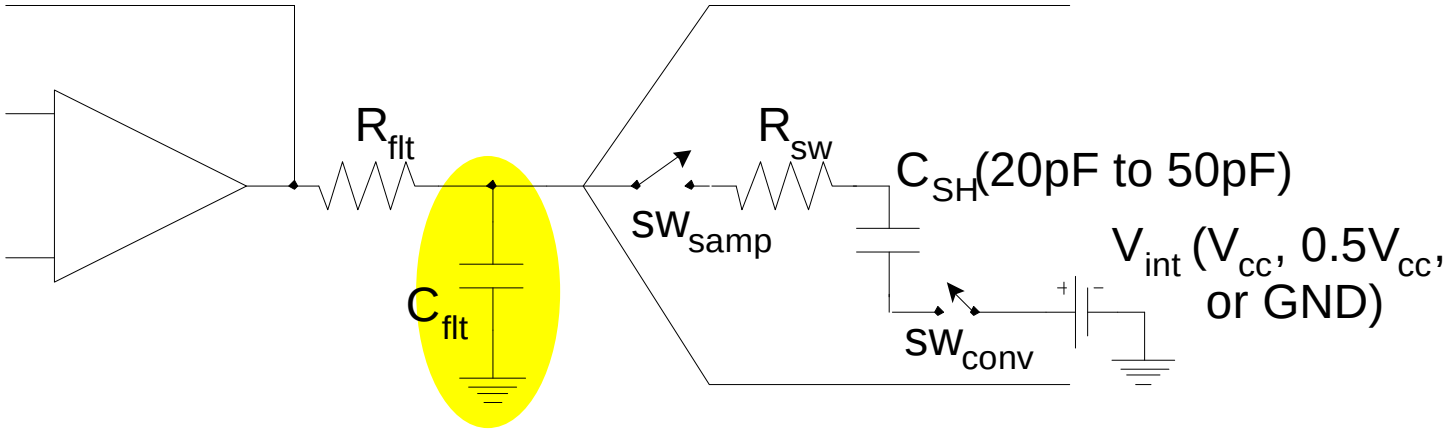
SAR A/D ≤ 500kHz

- *70% Applications*
  - *Slow Moving "Real World Process" Signals*
  - *Fast Acquisition & Conversion Allows More System Time For Processing, Computation, Decision Making*
  - *Multiplexed, Scanning Systems for Slow Moving Signals*
- *30% Applications*
  - *AC Fast Moving Dynamic Signals*
  - *"Real Time" Processing of Input Signals*

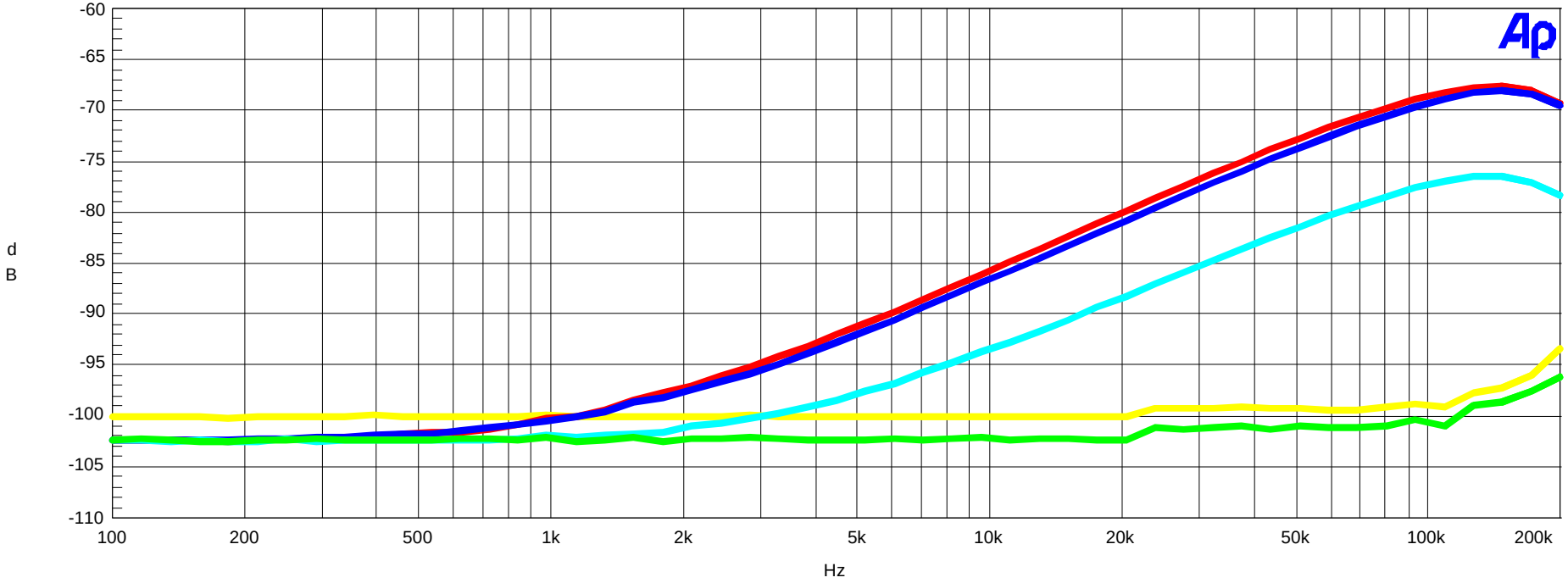
Look at the Charge Transients



Capacitor Type is Critical



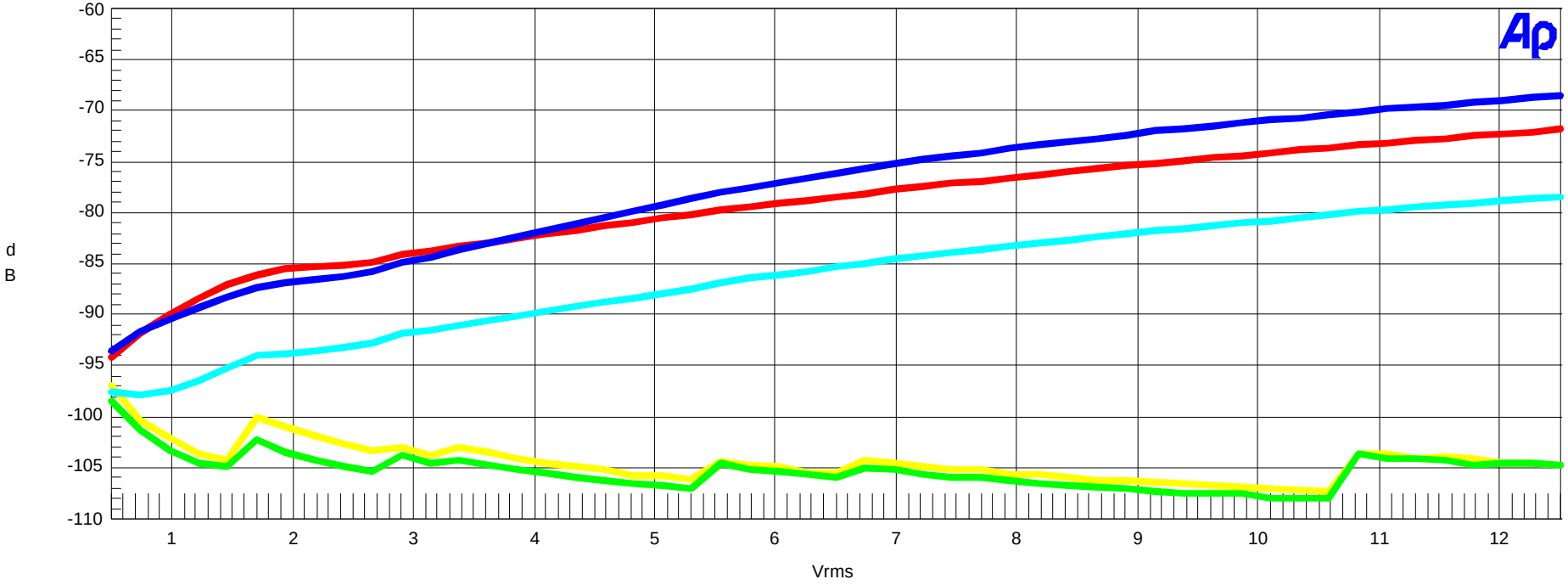
THD+N vs. Frequency for Various Capacitor types



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Yellow	Solid	1	Anlr.THD+N Ratio	Left	C = 0
2	1	Red	Solid	1	Anlr.THD+N Ratio	Left	C1
3	1	Blue	Solid	1	Anlr.THD+N Ratio	Left	C2
4	1	Cyan	Solid	1	Anlr.THD+N Ratio	Left	C3
5	1	Green	Solid	1	Anlr.THD+N Ratio	Left	C4

R = 100 ohm, C = 3.3 nF, Vp-p = 5V f(-3dB) = 482 kHz

THD+N vs. Voltage for Various Capacitor Types



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Yellow	Solid	1	Anlr.THD+N Ratio	Left	C = 0
2	1	Red	Solid	1	Anlr.THD+N Ratio	Left	C1
3	1	Blue	Solid	1	Anlr.THD+N Ratio	Left	C2
4	1	Cyan	Solid	1	Anlr.THD+N Ratio	Left	C3
5	1	Green	Solid	1	Anlr.THD+N Ratio	Left	C4

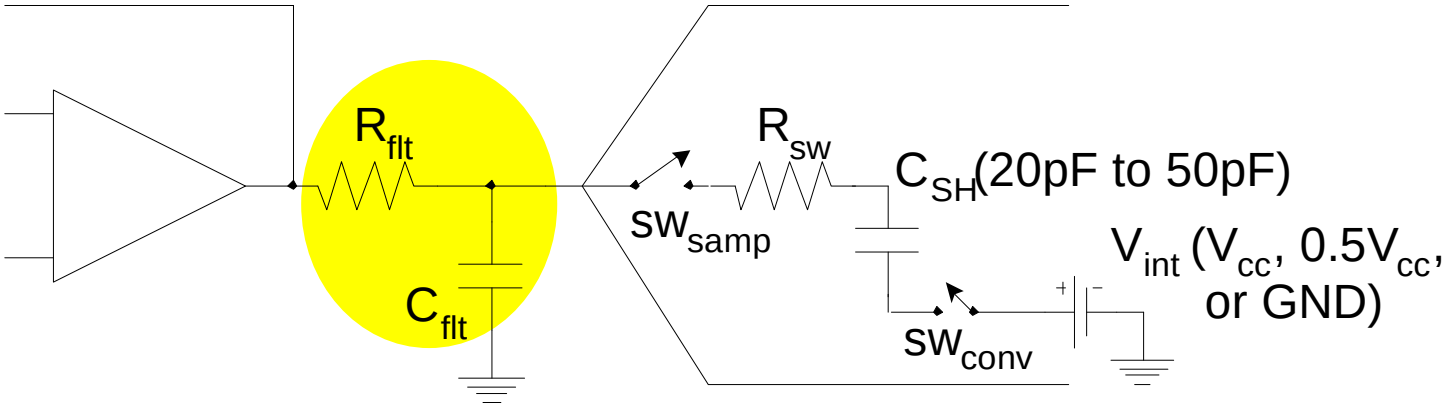
R = 100 ohm, C = 3.3 nF, f = 10 kHz, f(-3dB) = 482 kHz

Conclusions on “C” Type

- *Best performance: Sliver Mica or COG(NPO)*
- *Avoid all other*

- *Others may cost less and be smaller but can distort signal*

Selecting the Fly-wheel Values



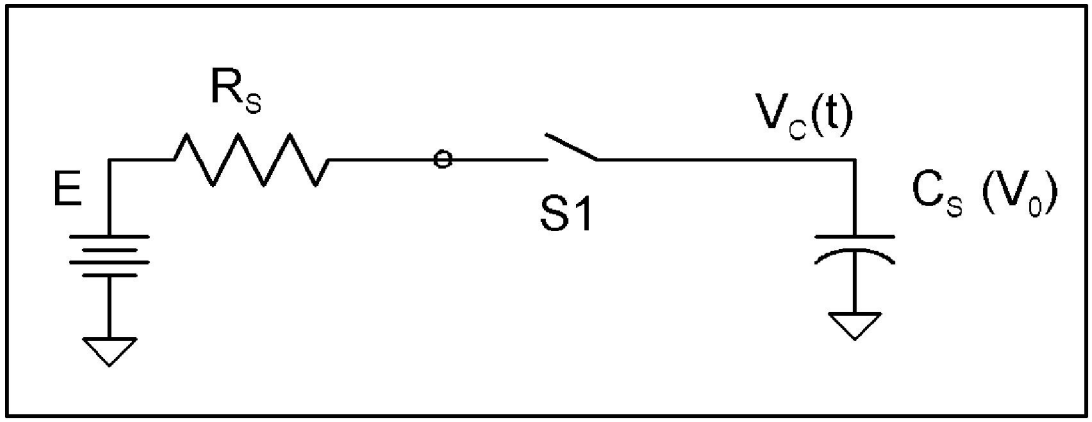
Fly Wheel Component Selection

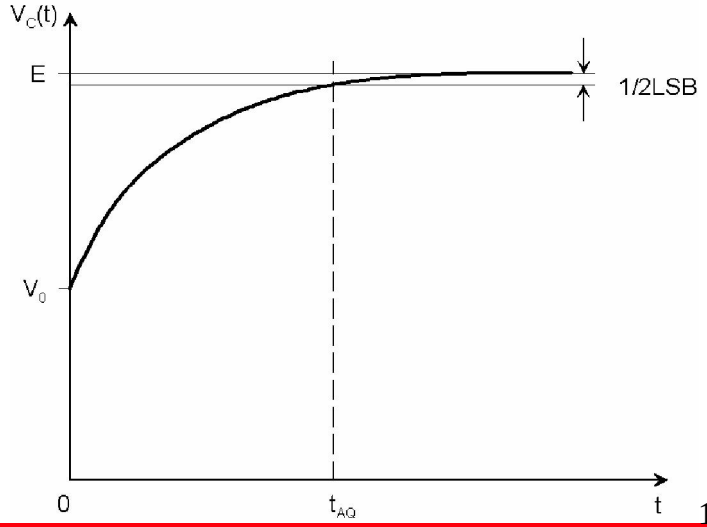
- *Pick C_{flt} =20*C_{SH} (See Appendix for proof)*
- *R_{flt} Calculation*

  - *$t_{flt\_settle} = t_{SAMPL} = 12\ \tau_{FLT}$*
    Theoretical Minimum
  - *Practical results*
    - *Use t =18τ_{FLT} Margin for:*
      - *Op Amp Output Load Transient*
      - *Op Amp Output Small Signal Settling Time*
  - *$R_{flt} = t_{SAMPL}/18\ C_{flt}$*

ADC Sampling Considerations

Voltage on the sampling capacitor during sampling period





$$V_C(t) = V_0 + (E - V_0) \times (1 - e^{-\frac{t}{\tau}})$$

$$E - V_C(t_{AQ}) \le \frac{1}{2} LSB$$

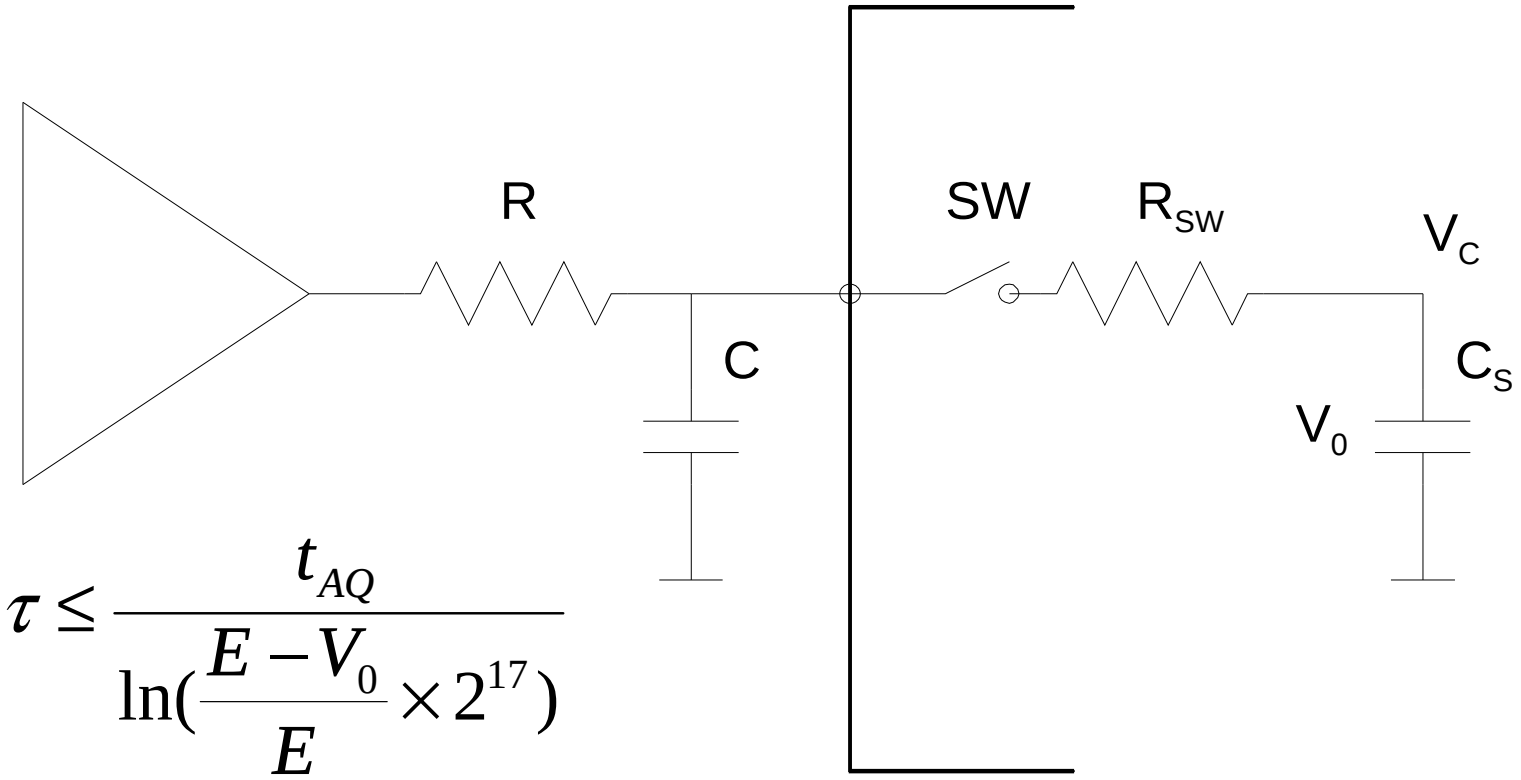
$$V_C(t_{AQ}) \ge E \times (1 - \frac{1}{2^{17}})$$

$$\tau \le \frac{t_{AQ}}{\ln(\frac{E - V_0}{E} \times 2^{17})}$$

1)

ADC Sampling Considerations

Suggested input sampling switch transient-immunity RC filter



$$\tau \le \frac{t_{AQ}}{\ln\left(\frac{E - V_0}{E} \times 2^{17}\right)}$$

Required Settling Time

Number of bits	0.5LSB	Time Constants
10	0.0488281%	8
12	0.0122070%	9
14	0.0030518%	11
16	0.0007629%	12
18	0.0001907%	13
20	0.0000477%	15
22	0.0000119%	17
24	0.0000030%	18

See appendix for calculations

Establish Op Amp Specs

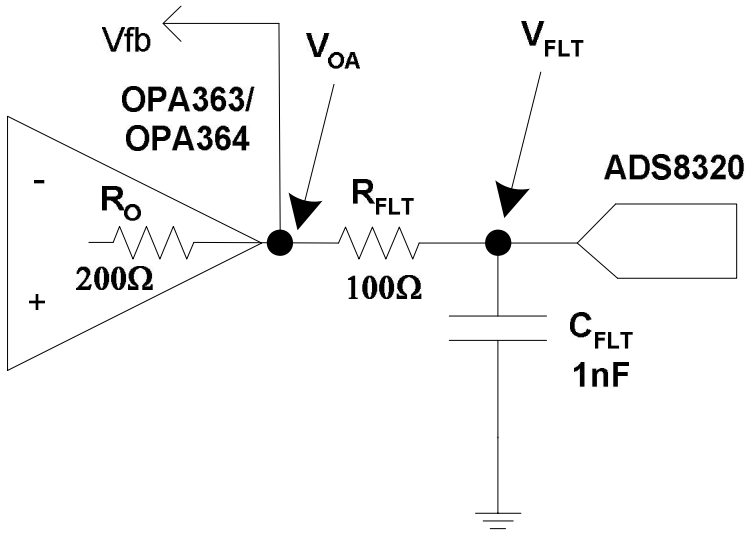
Determine Op Amp specs needed based on system values set in design.

Op Amp specs to be determined:

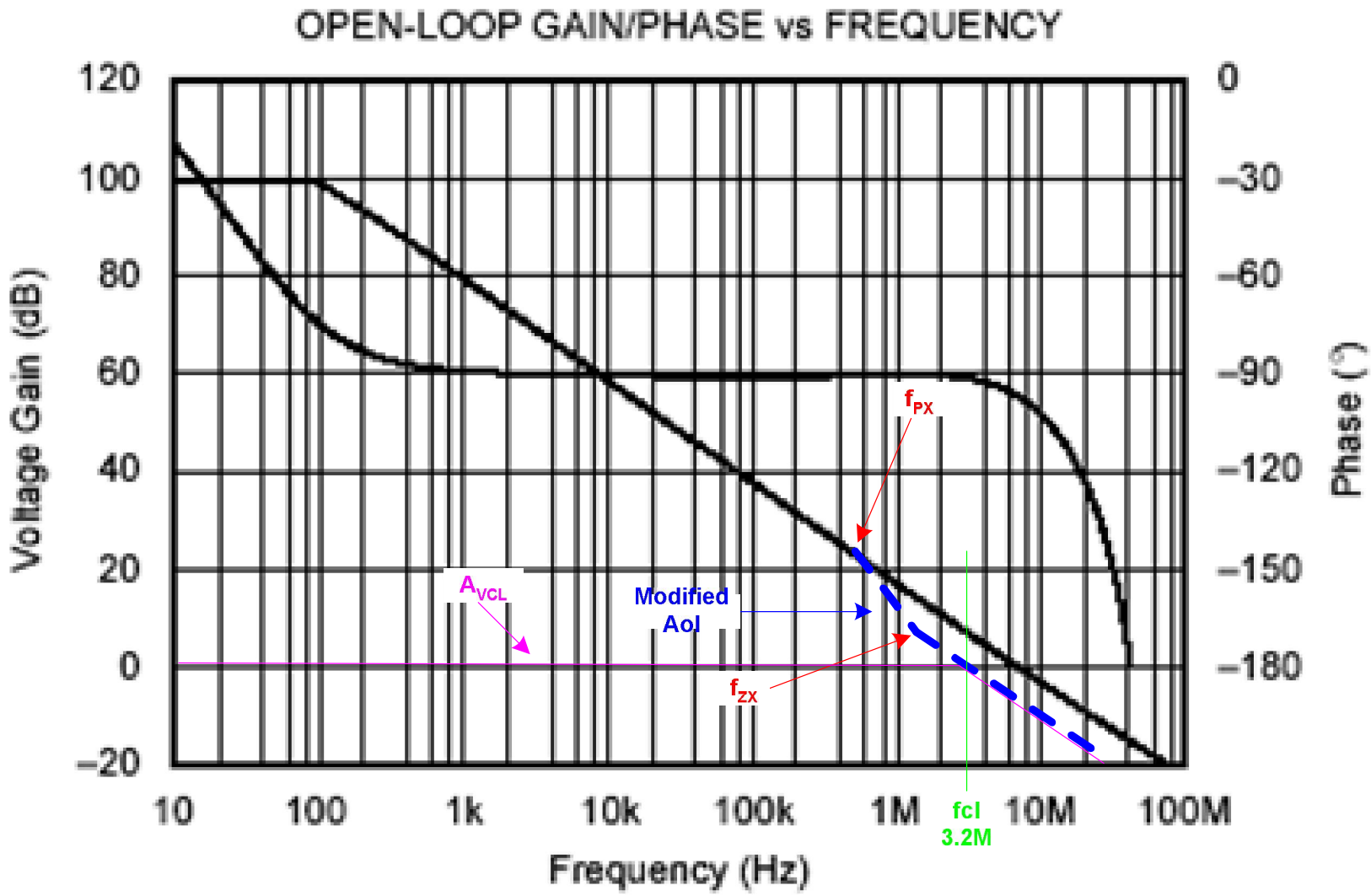
- *UGBW*
- *Slew Rate*
- I_{out}

Impact on UGBW

- *Modified A_{ol} due to R_{FLT} & C_{FLT}*
  - $f_{PX} = 1/[2\,\Pi(R_O + R_{FLT})C_{FLT}]$
  - $f_{ZX} = 1/[2\,\Pi\,R_{FLT}C_{FLT}]$
- *Stability Check*
  - *At f_{cl} "Rate-of-closure" is 20dB/decade à f_{ZX} cancels f_{PX} before f_{cl}*
  - *f_{PX} and f_{ZX} are ≤ decade apart*
    - *Phase of pole will be cancelled by phase of zero*
  - *This implies: $R_{FLT} < 9\,R_O$*
- *Impact on UGBW*
  - $UGBW_{mod} = UGBW_{orig} - (f_{ZX} - f_{PX})$



Impact on UGBW-cont



Op Amp Specs to Check

- $UGBW_{mod} > 2 * 1/[2 \Pi R_{FLT} C_{FLT}]$
- *Op Amp Transient Output Drive to R_{FLT} & C_{FLT}*
  - $I_{Opk\ max} = (5\%\ V_{REF})/(R_{FLT})$

Interface Design Check List

- *Op Amp Common Mode Voltage*
- *Op Amp Output Swing to Rail*
- *Op Amp Settling Time*
- *Filter Capacitor Type*
- *Filter Component Values*
- *Op Amp Specifications*

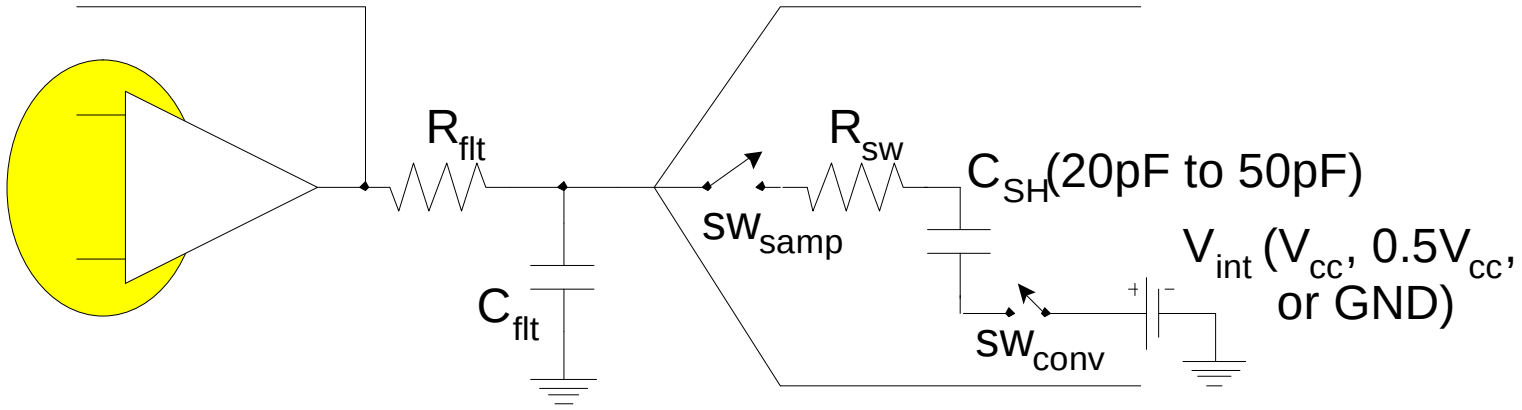
Appendix – Calculation Details

1. C_{flt} as a Function of C_{sh}
2. Open Loop Output Resistance

   vs.

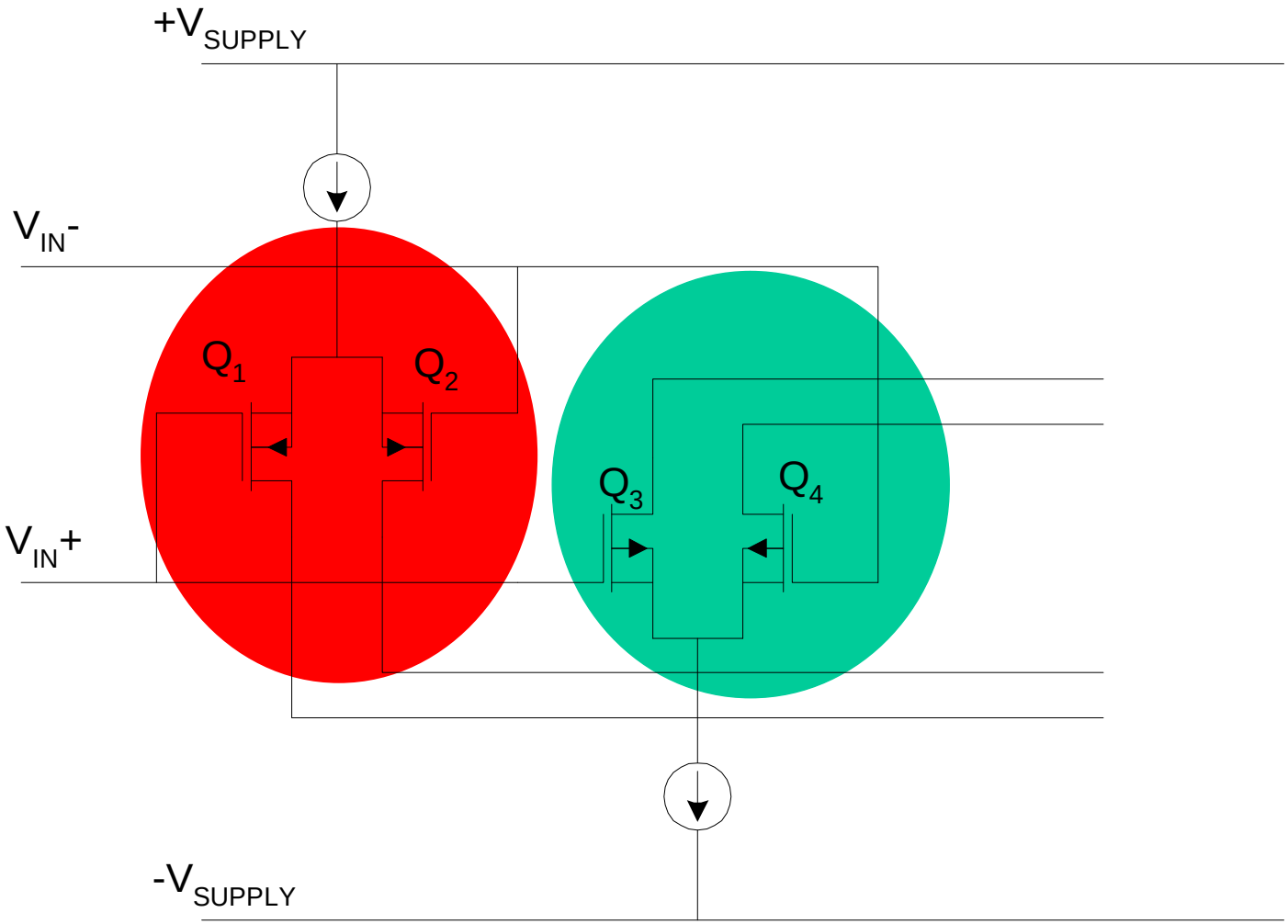
   Closed Loop Output Resistance
3. Modified A_{ol} Calculations
4. Time to Charge Capacitor

Op Amp Input Concerns

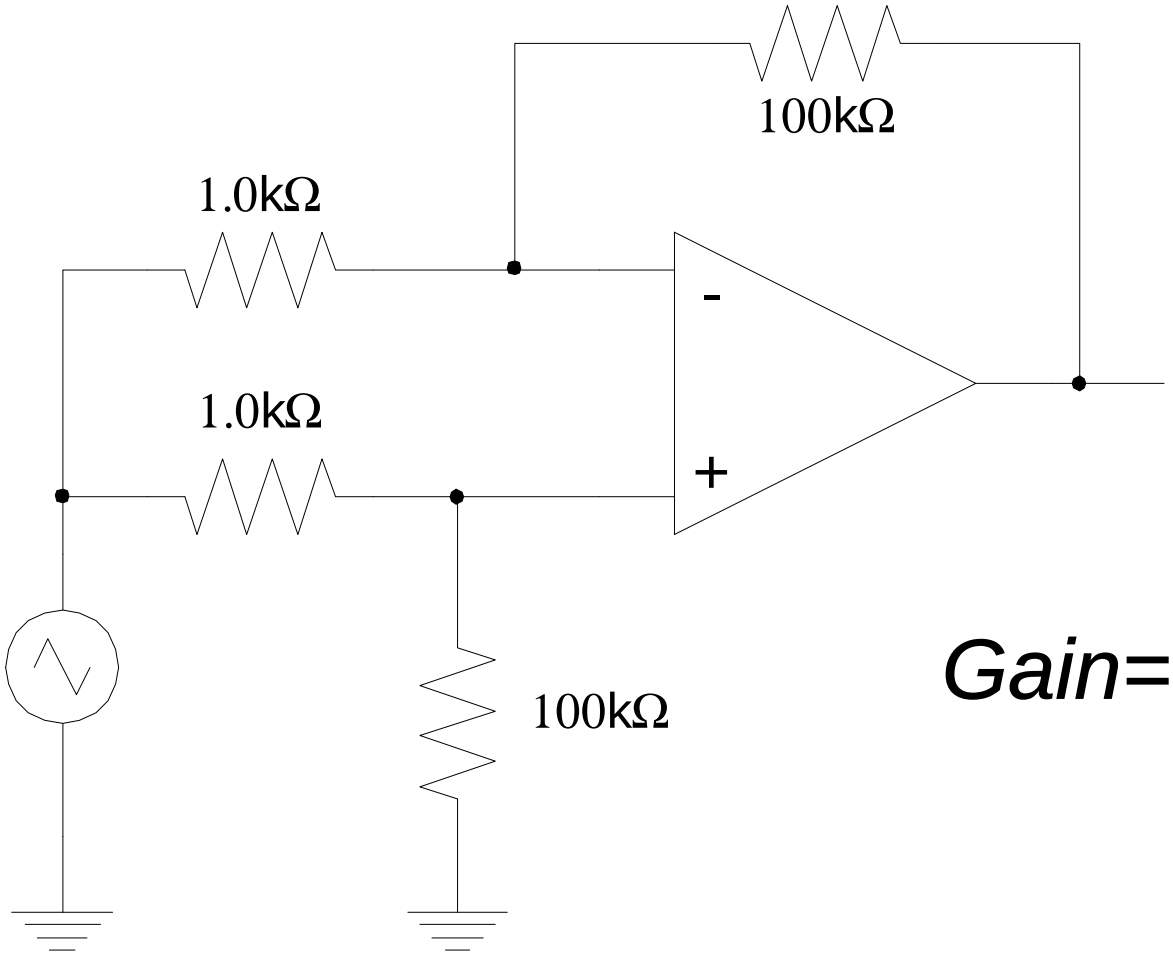


Rail-to-Rail Input

Input Stage-Parallel P-ch & N-ch



Looking at Input Stage Performance

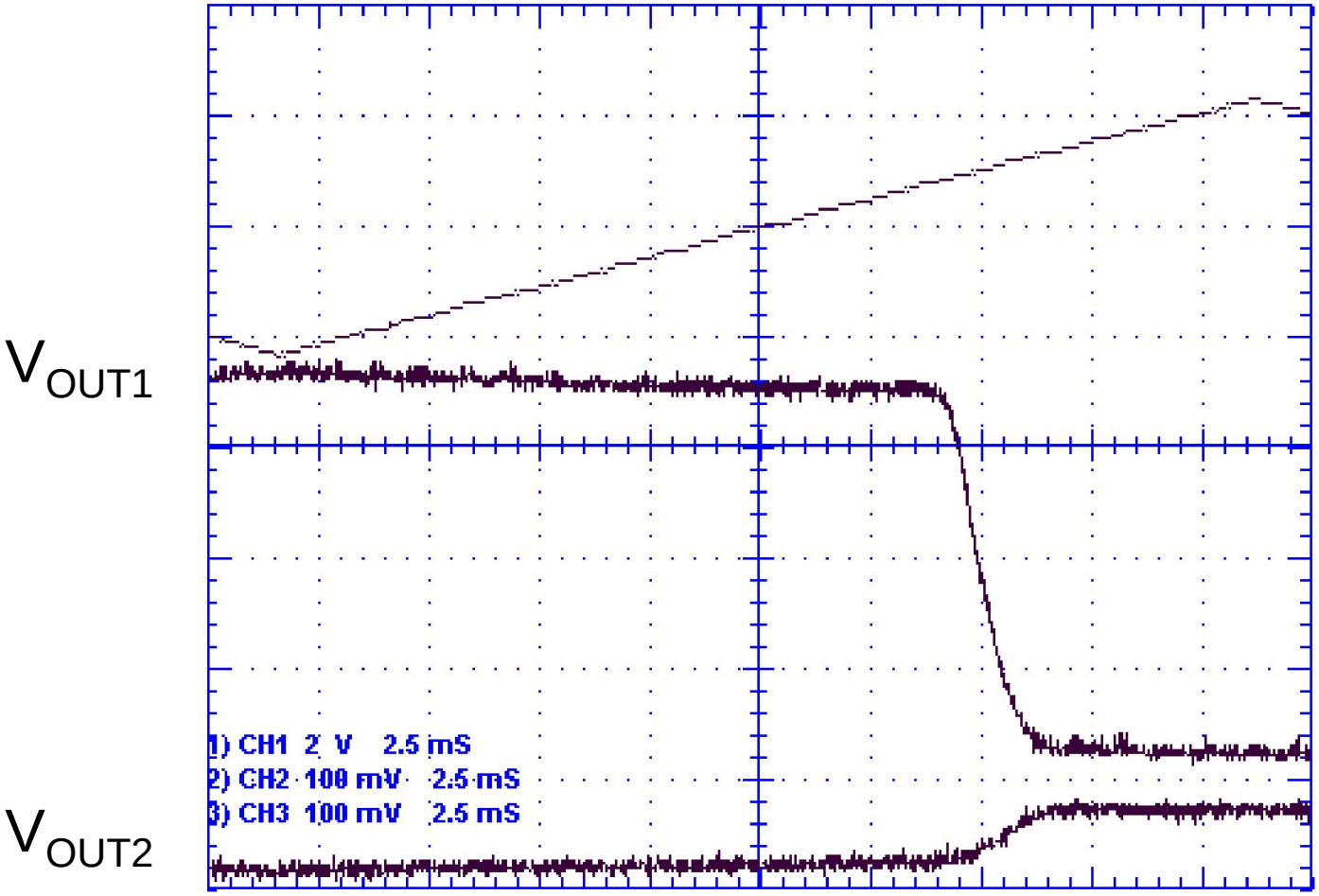


Gain=100

Single Supply RRI Plot-V_{OS} vs CMV

(Most RRI Op Amps Except OPA363/OPA364)

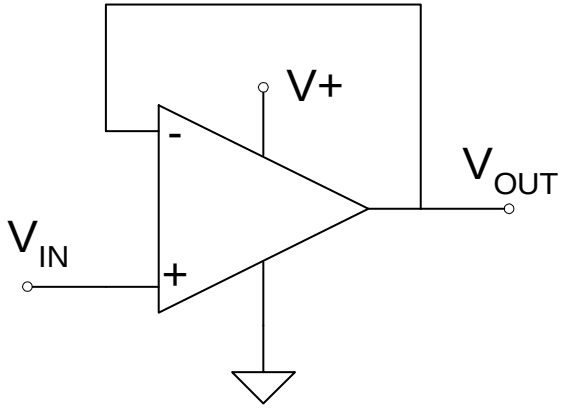
OPA2340 (Dual: V_{OUT1} & V_{OUT2} from different halves)



Performance Requirements

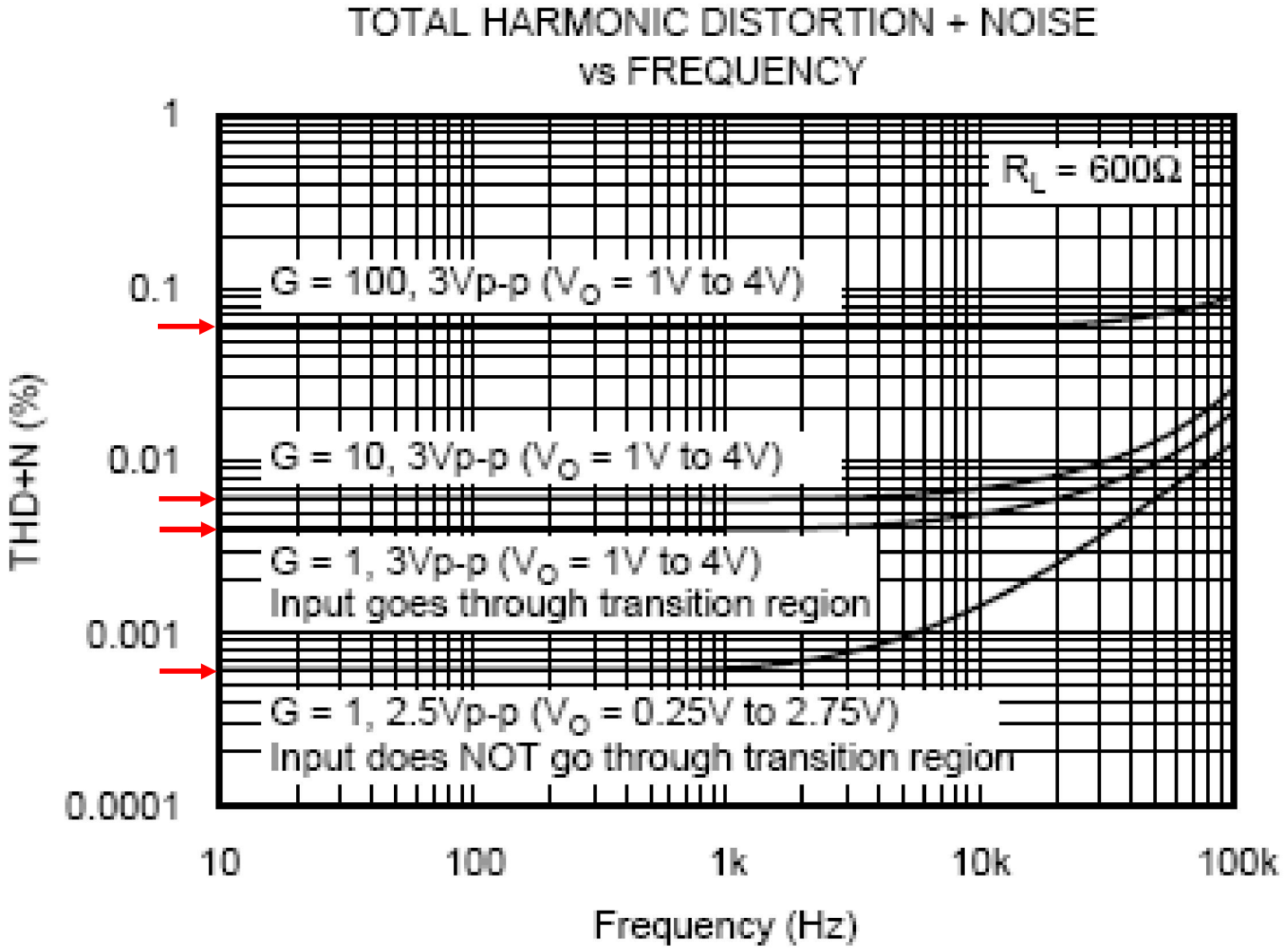
The simple buffer stage.

Most accurate unity gain.

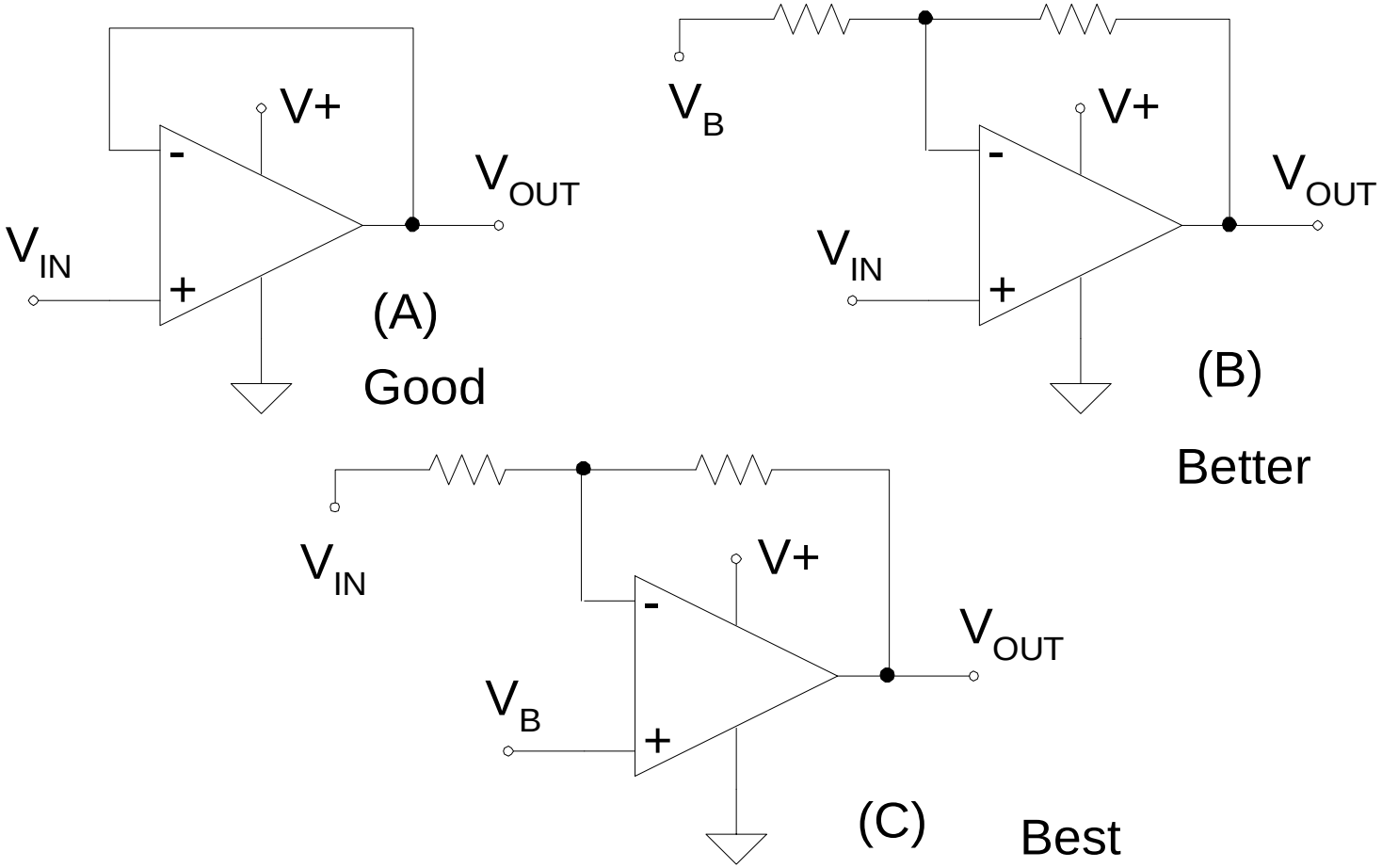


Bits	(mV)	(dB)
10	2.44	66.2
12	0.61	78.3
16	0.0382	102.3

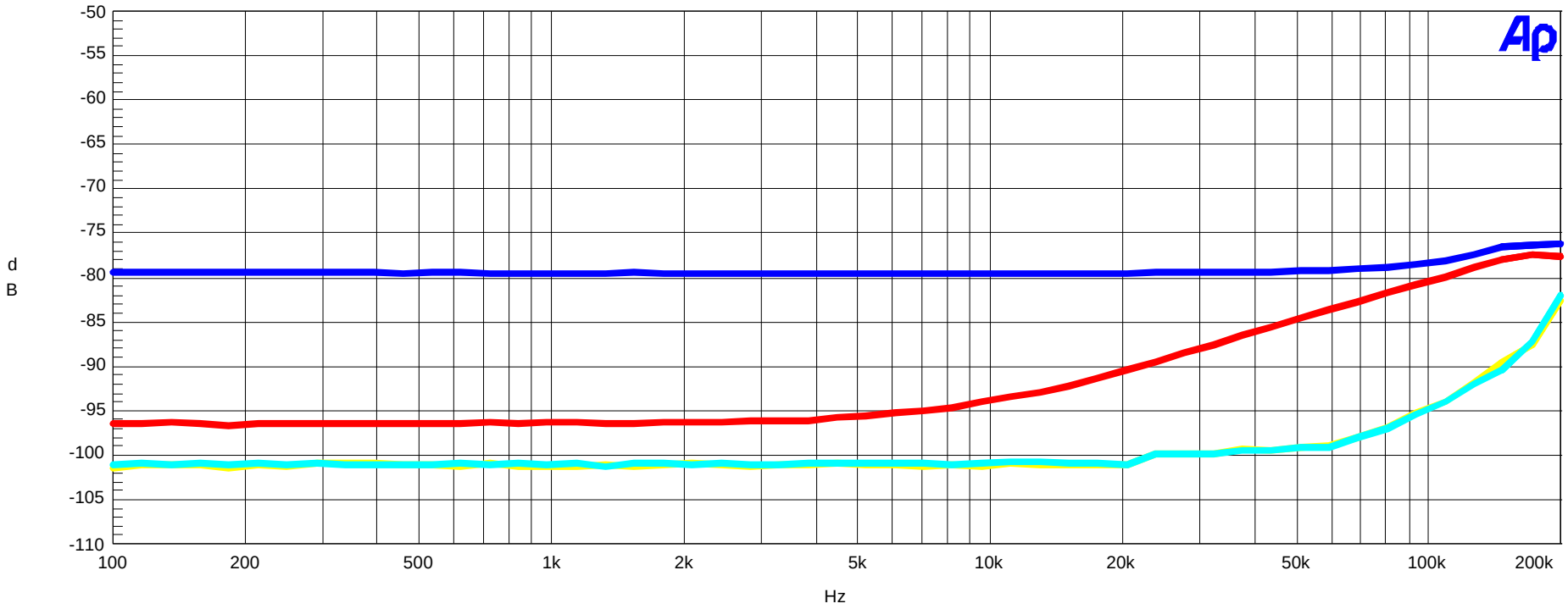
OPA350 Data Sheet THD+N



Possible Input Schemes



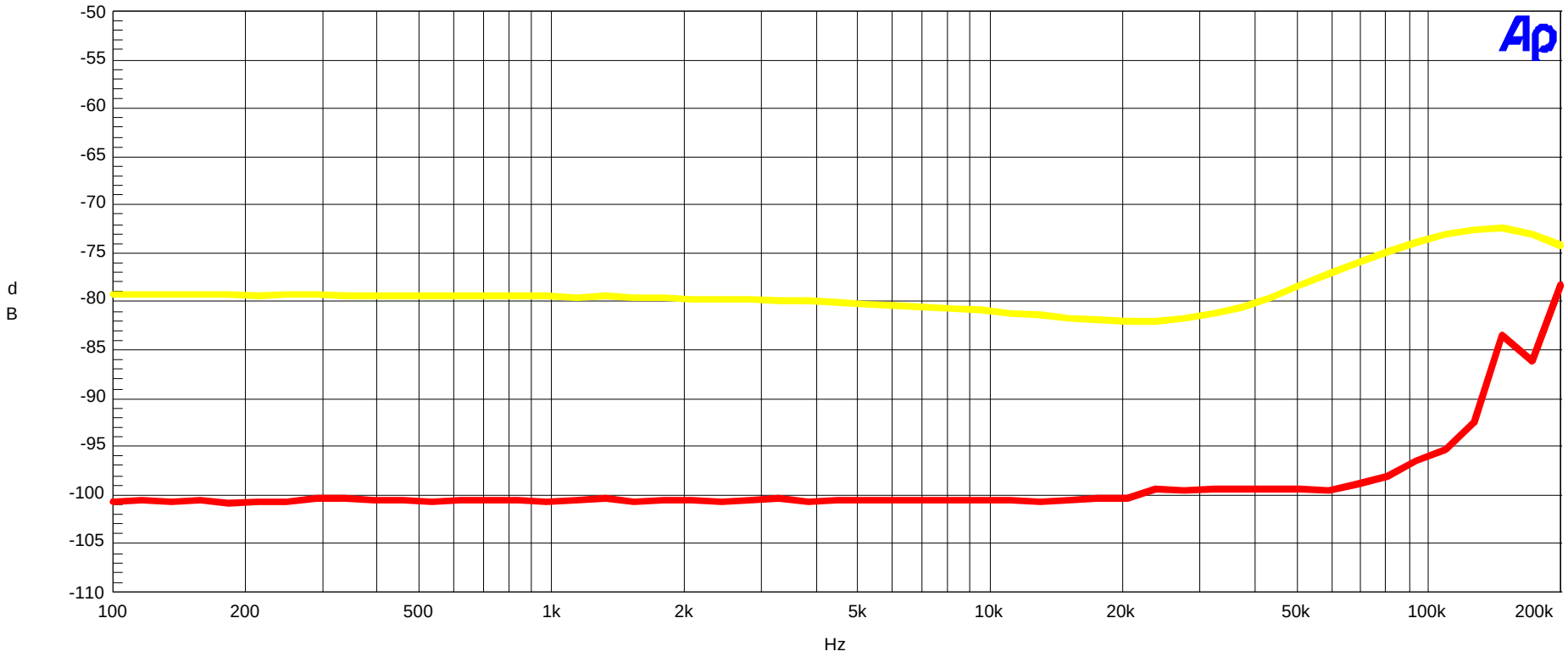
OPA350 THD+N vs Frequency



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Yellow	Solid	1	Anlr.THD+N Ratio	Left	OPA350 High CMRR G=-1
2	1	Red	Solid	1	Anlr.THD+N Ratio	Left	OPA350 High CMRR G=+1
3	1	Blue	Solid	1	Anlr.THD+N Ratio	Left	OPA350 Low CMRR G=+1
4	1	Cyan	Solid	1	Anlr.THD+N Ratio	Left	OPA350 Low CMRR G=-1

OPA 350, R = 0 ohm, C = 0 nF, Vp-p = 4 V, G = +1or -1

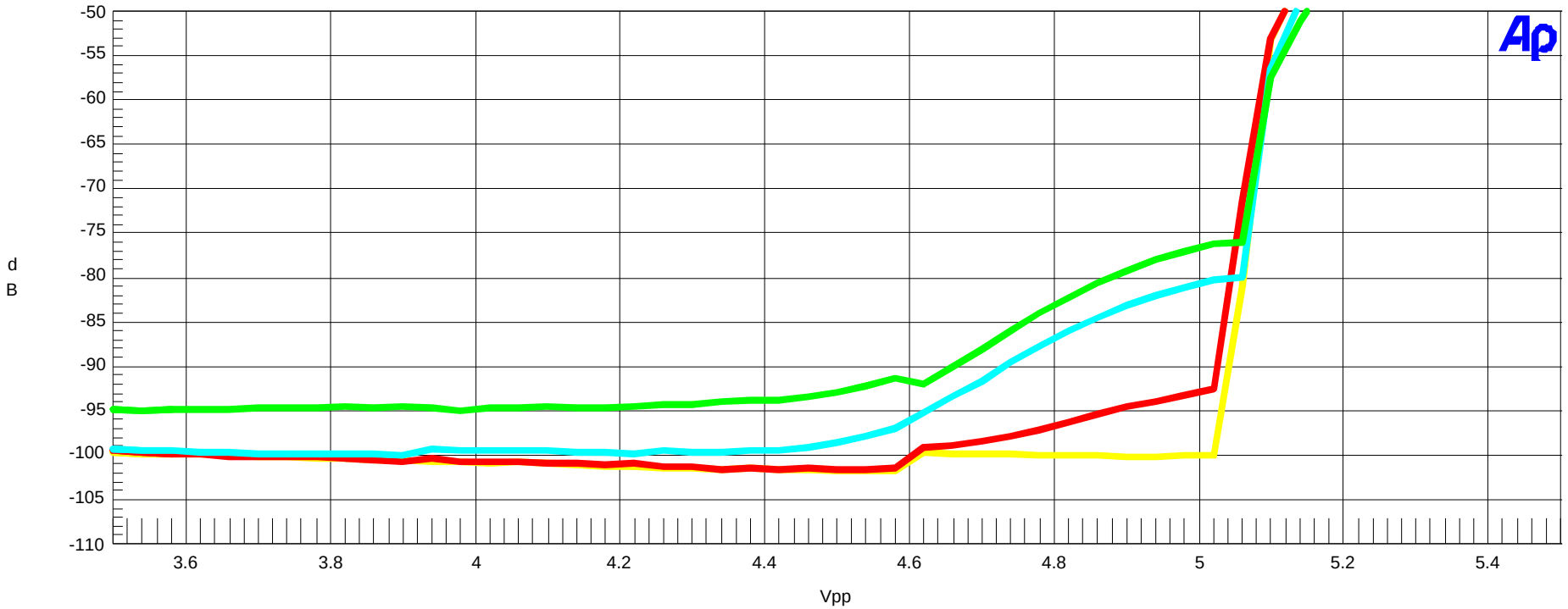
OPA350 with RC, THD+N vs Frequency



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Yellow	Solid	1	Anlr.THD+N Ratio	Left	OPA350 Low CMRR G=+1 C1
2	1	Red	Solid	1	Anlr.THD+N Ratio	Left	OPA350 Low CMRR G=-1 C4

OPA 350, R = 100 ohm, C = 3.3 nF, Vp-p = 4 V, f(-3dB) = 482 kHz, G = +1or -1

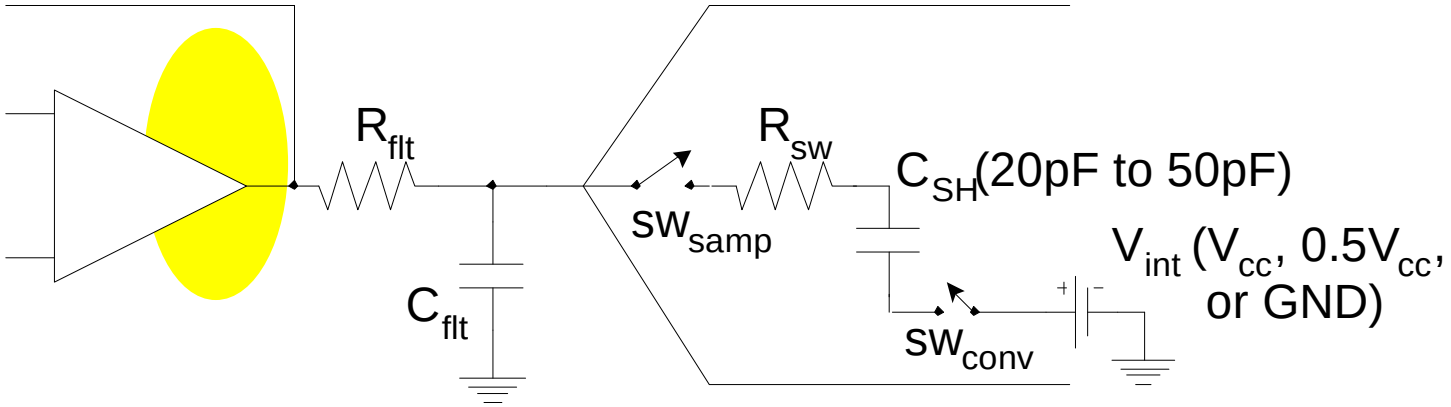
OPA350 THD+N vs Input Voltage



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Yellow	Solid	1	Anlr.THD+N Ratio	Left	OPA350 Low CMRR 1kHz
2	1	Red	Solid	1	Anlr.THD+N Ratio	Left	OPA350 Low CMRR 10kHz
3	1	Cyan	Solid	1	Anlr.THD+N Ratio	Left	OPA350 Low CMRR 50kHz
4	1	Green	Solid	1	Anlr.THD+N Ratio	Left	OPA350 Low CMRR 100kHz

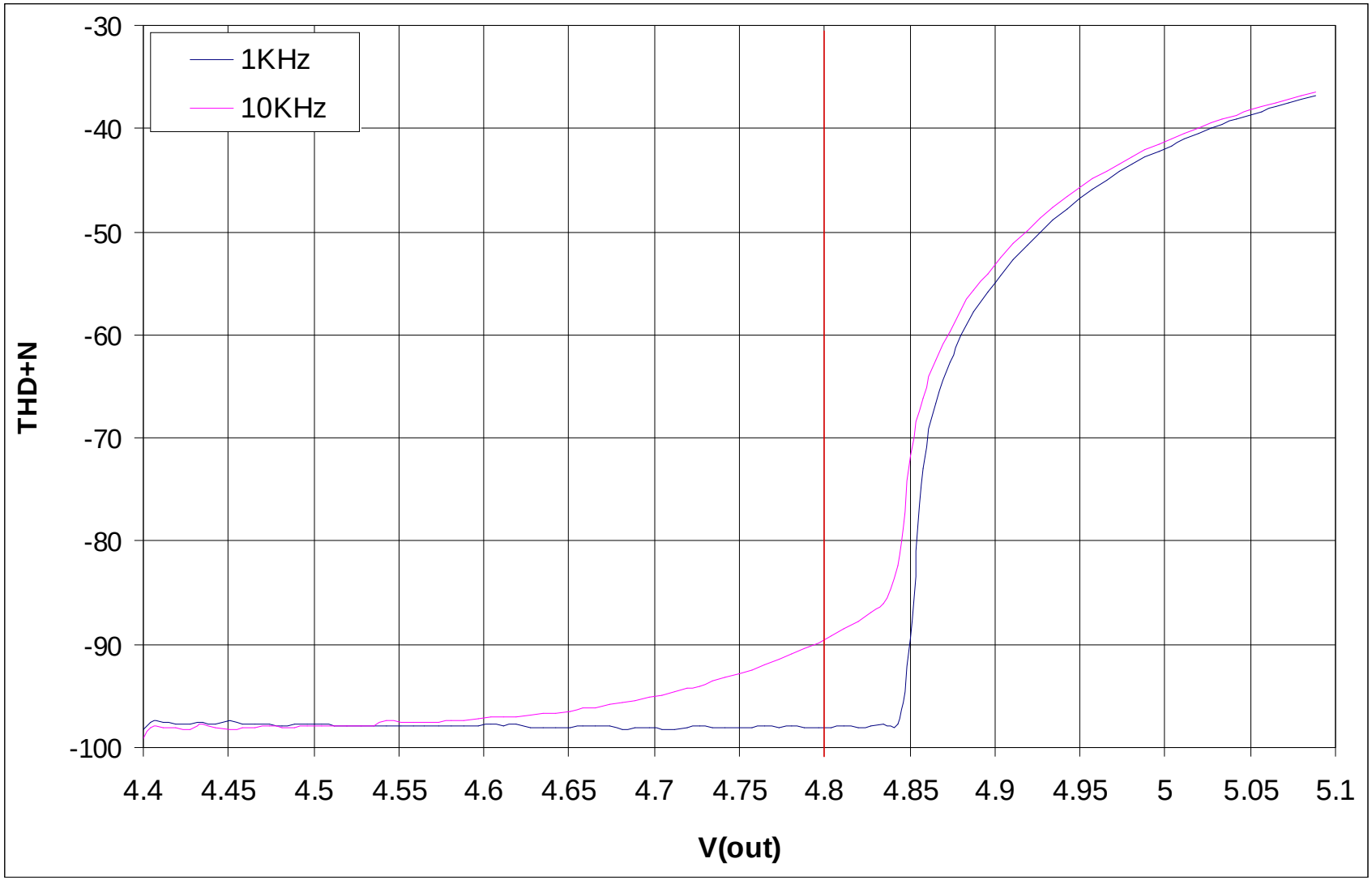
OPA 350, R = 0 ohm, C = 0 nF, G = -1

Output Stage Concerns

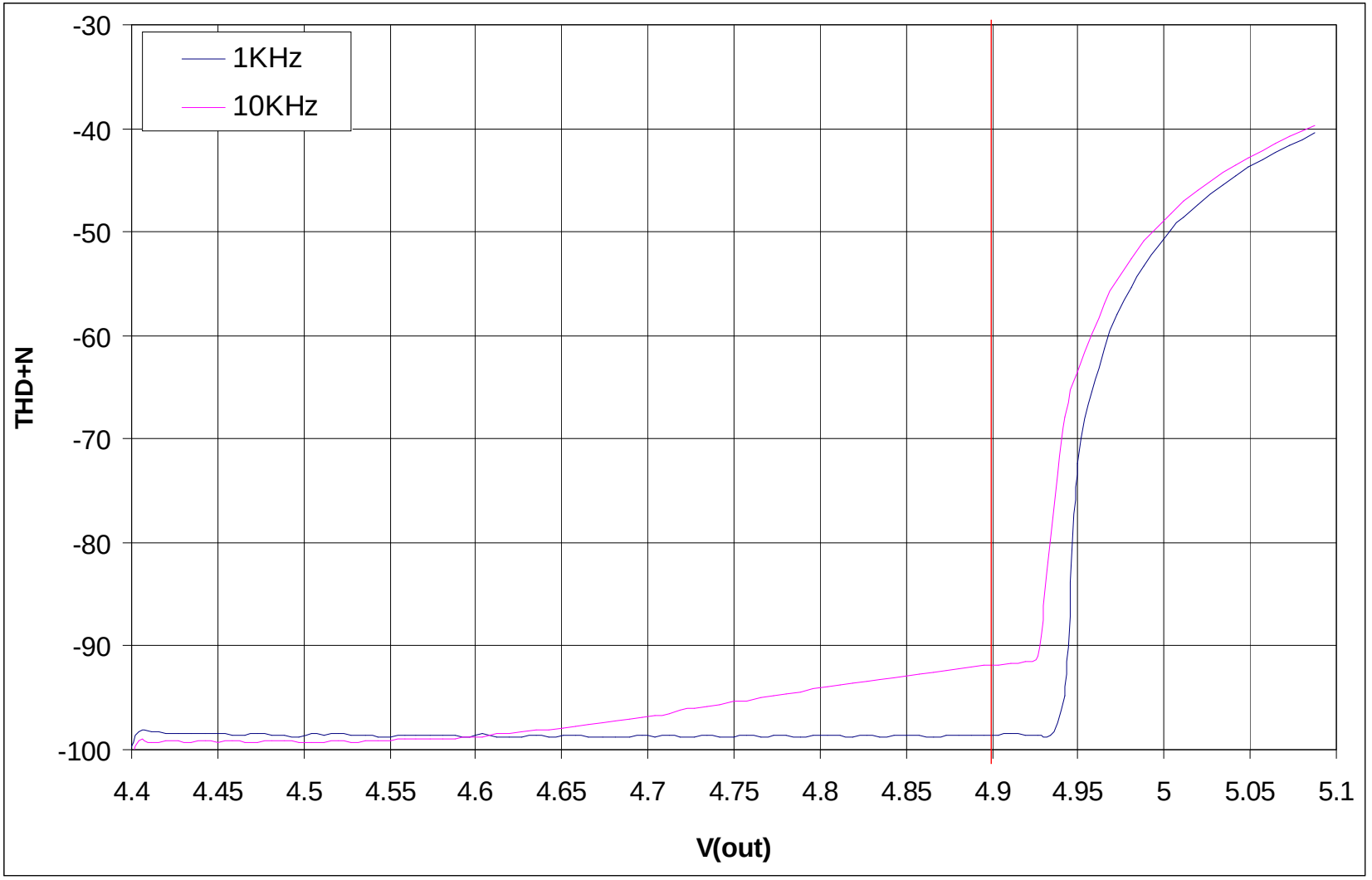


Rail-to-Rail Output

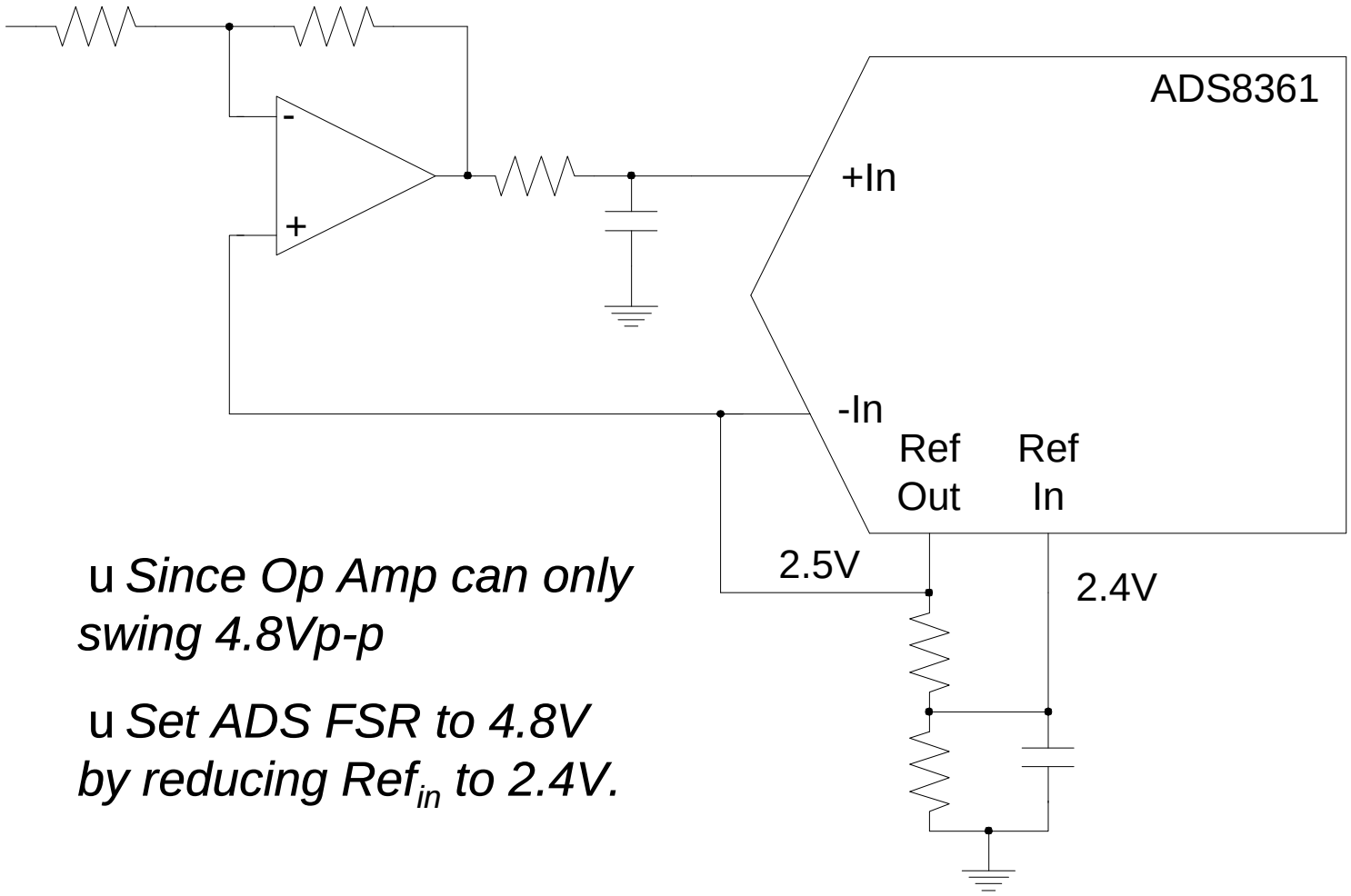
OPA300



OPA350

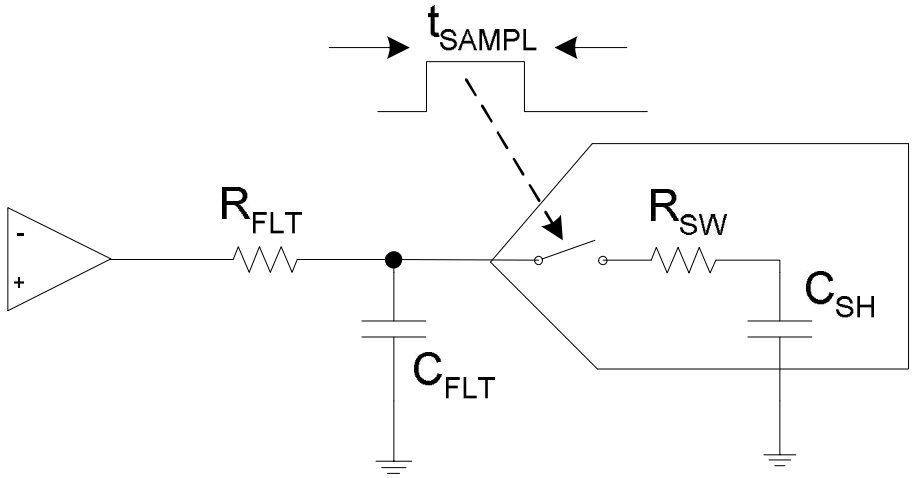


Solution Circuit



- *Since Op Amp can only swing 4.8Vp-p*
- *Set ADS FSR to 4.8V by reducing Ref_{in} to 2.4V.*

Filter Design Example



- R_{SW} = 100Ω (Not needed for Buffer & Filter Calculations)
- C_{SH} = 50pF [for ADS8361]
- Worst case ΔV across C_{SH} is V_{REF}
  - V_{REF} = +5V
- t_{SAMPL} = 1.88µs [for ADS8361]

Filter Design Example(cont)

- *Charge Transfer Equation: Q = CV*
- *Charge required to charge C_{SH} to V_{REF}*
  - $Q_{SH} = C_{SH}V_{REF}$
  - $Q_{SH} = 50pF \cdot 5V = 250pC$
- *IDEAL C_{FLT}*
  - *"Charge Bucket" to fill C_{SH} with only a 76µV (1/2LSB) droop on C_{FLT}*
  - $Q_{FLT} = Q_{SH}$
  - $Q_{FLT} = C_{FLT}$ (38µV)
  - $250pC = C_{FLT}$ (38µV) → $C_{FLT} = 6.6\mu F$
- *IDEAL $C_{FLT} = 6.6\mu F$*
  - *Not a good, small, cheap high frequency ceramic capacitor*
  - *Not practical for Op Amp to drive directly (stability, transient current)*
  - *Isolation resistor likely not large enough to help isolate Cload and still meet necessary filter time constant*

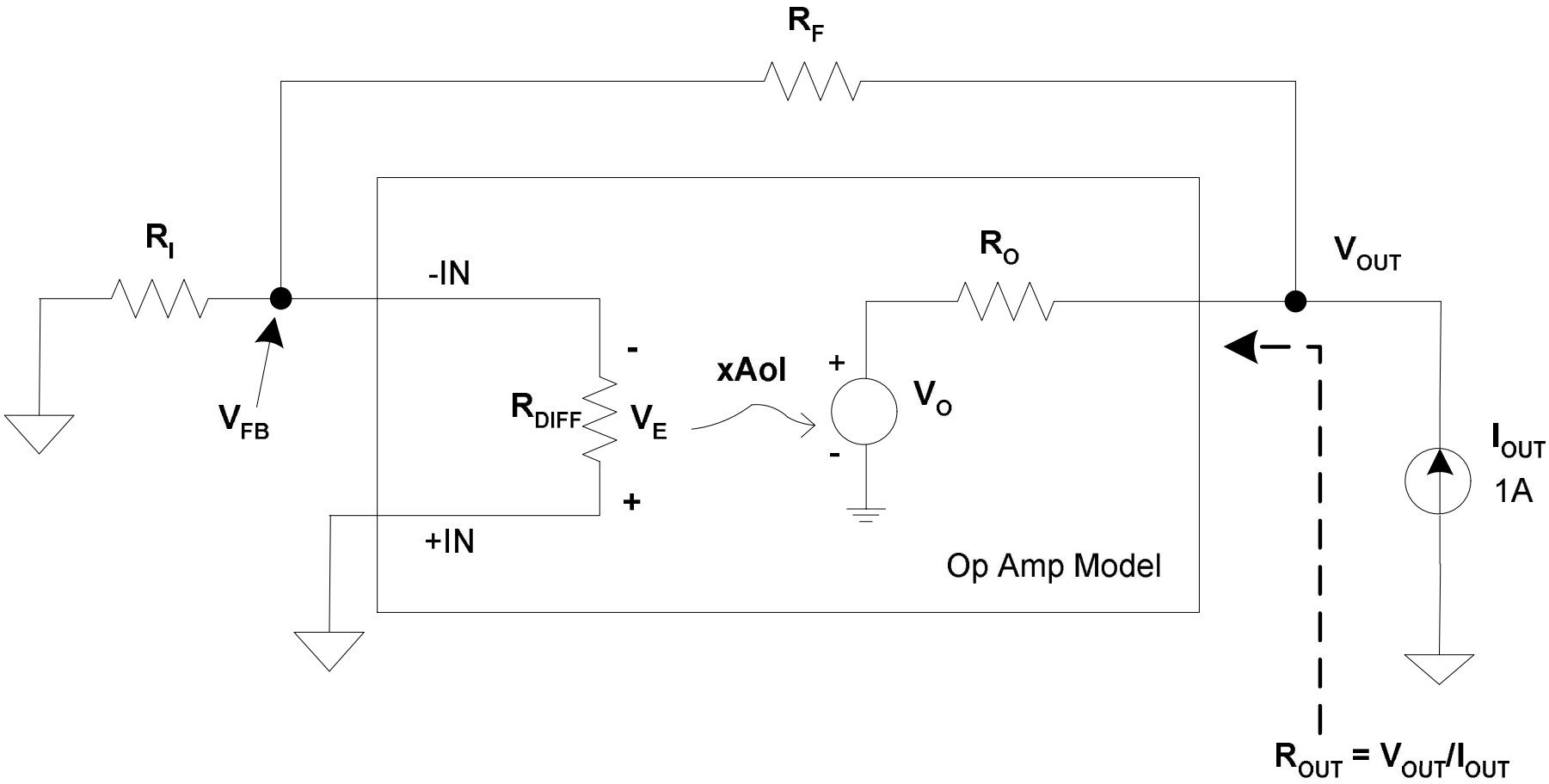
Filter Design Example(cont)

- *Partition the "Charge Bucket"*
  - *95% from C_{FLT}*
  - *5% from Op Amp*

- *C_{FLT} value required to provide Q_{SH} with <5% droop on C_{FLT}*
  - *$Q_{FLT} = Q_{SH}$*
  - *$Q_{FLT} = C_{FLT}\,(0.05V_{REF})$*
  - *$250pC = C_{FLT}\,(0.05 \cdot 5V) \rightarrow C_{FLT} = 1nF$*

- *During t_{SAMPL} the Op Amp must provide 5% V_{REF} to C_{FLT}*
  - *Ensure C_{FLT} is at least 10X > C_{SH}*
    - *This implies dominant load for Op Amp Buffer is C_{FLT}*
    - *1nF = 20 X 50pF à $C_{FLT} = 20X\ C_{SH}$*

Op Amp Model for Derivation of R_{OUT}



Derivation of R_{OUT} (Closed Loop Output Resistance)

$$\beta = V_{FB}/V_{OUT} = [V_{OUT}(R_I / \{R_F + R_I\})]/V_{OUT} = R_I / (R_F + R_I)$$

$$R_{OUT} = V_{OUT}/I_{OUT}$$

$$V_O = -V_E \, AoI$$

$$V_E = V_{OUT}[R_I/(R_F + R_I)]$$

$$V_{OUT} = V_O + I_{OUT}R_O$$

$$V_{OUT} = -V_E AoI + I_{OUT}R_O$$

$$V_{OUT} = -V_{OUT}[R_I/(R_F + R_I)] \, AoI + I_{OUT}R_O$$

$$V_{OUT} + V_{OUT}[R_I/(R_F + R_I)] \, AoI = I_{OUT}R_O$$

$$V_{OUT} = I_{OUT}R_O / \{1+[R_I AoI/(R_F+R_I)]\}$$

$$R_{OUT} = V_{OUT}/I_{OUT} = I_{OUT}R_O / \{1+[R_I A_{OL}/(R_F+R_I)]\}$$

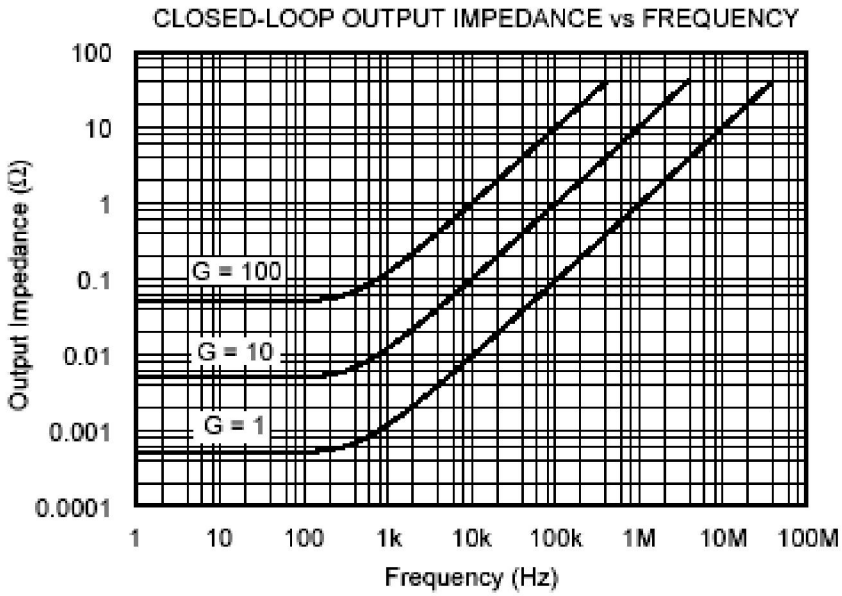
$$R_{OUT} = R_O / (1+AoI\beta)$$

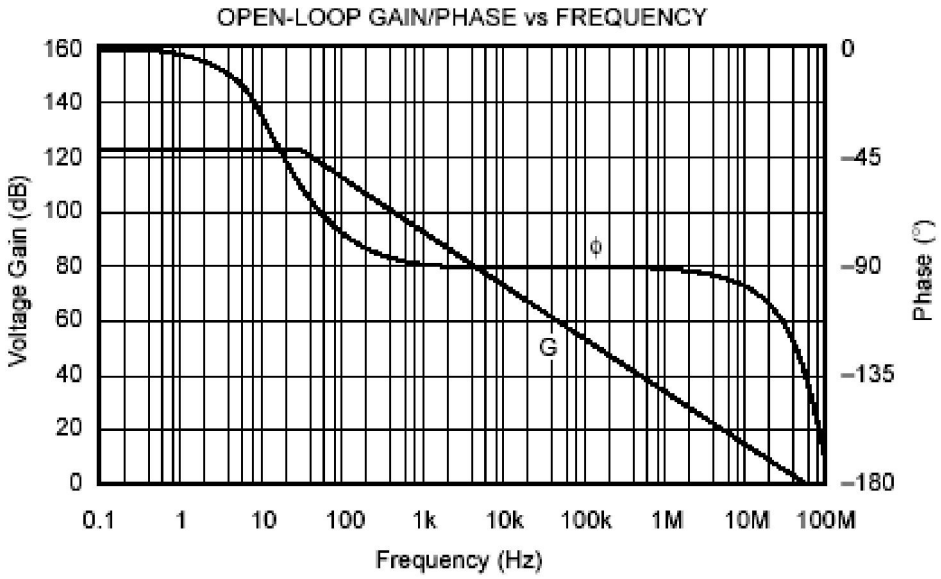
OPA353 Specifications

R_O = 40Ω

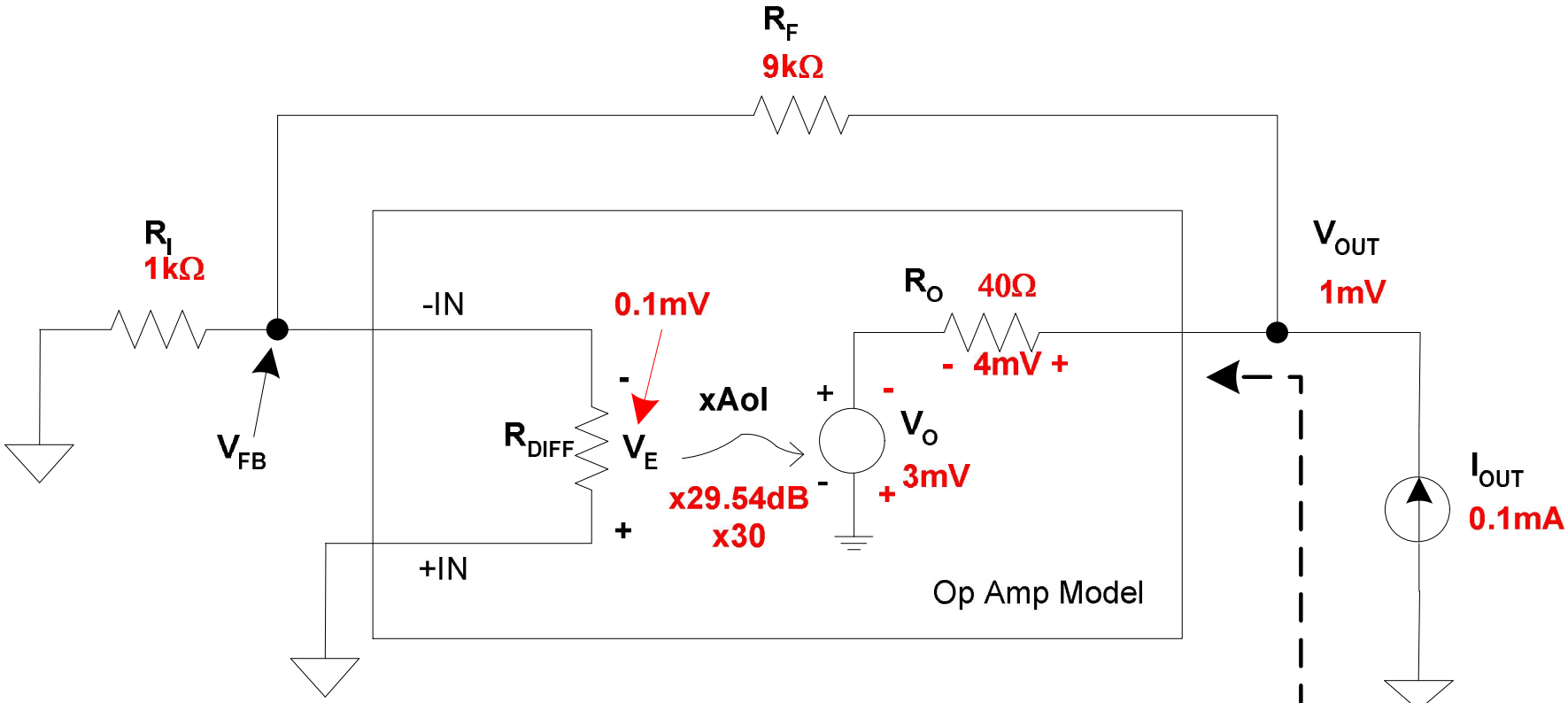
R_{OUT} (@1MHz, G=10) = 10Ω

AoI @1MHz = 29.54dB = x30





OPA353 R_{OUT} Calculation



R_O = 40Ω

R_{OUT} (@1MHz, G=10) = 10Ω

Aol @10mHz = 29.54dB = x30

$R_{OUT} = V_{OUT}/I_{OUT}$

R_{OUT} = 1mV/0.1mA

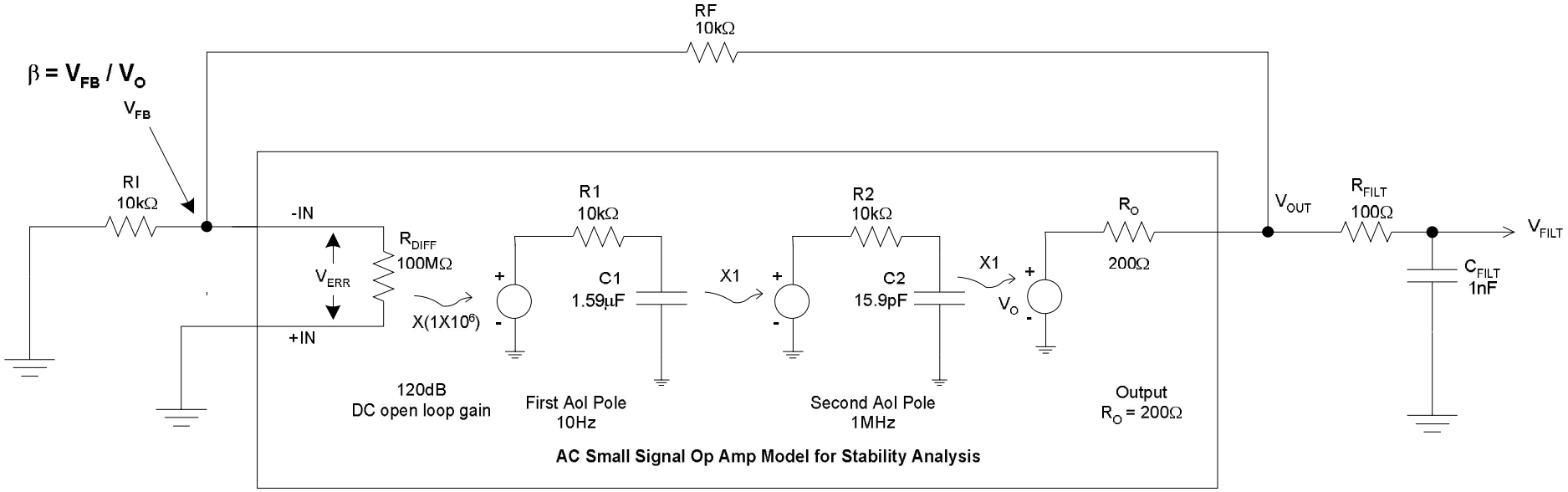
R_{OUT} = 10Ω

R_{OUT} vs R_O

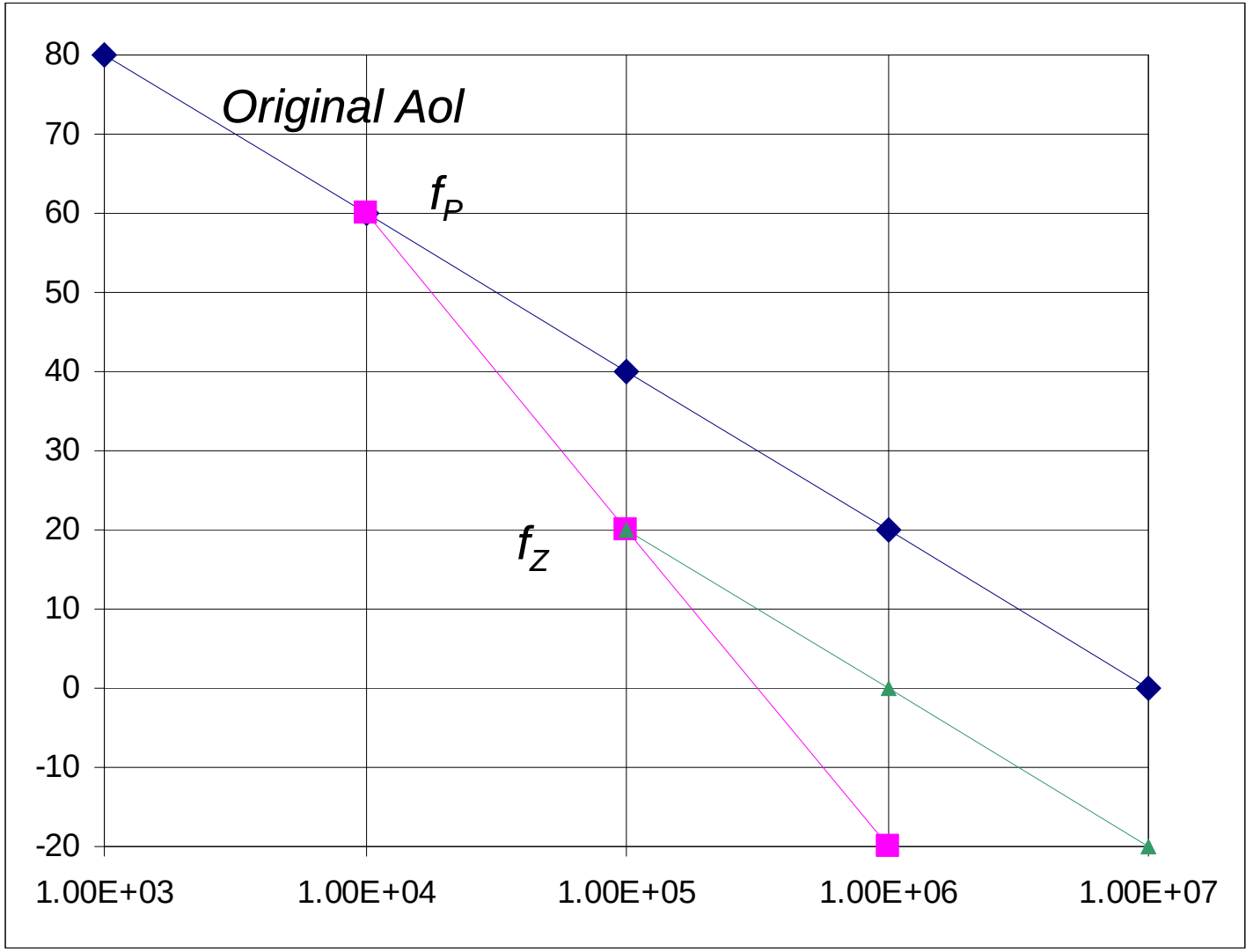
- R_O does not change when feedback is used to close the loop
- Closed loop feedback forces V_O to increase/decrease
- The increase/decrease in V_O appears at V_{OUT} as a reduction in R_O
- R_{OUT} is the net effect of R_O and closed loop feedback controlling V_O

Op Amp Model for AC Stability Analysis

- R_O *is constant over the Op Amp's bandwidth*
- R_O *is defined as the Op Amp's Open Loop Output Resistance*
- R_O *is measured at* I_{OUT} *= 0 Amps, f = 1MHz*
- R_O *is included in* β *calculation*



Aol Modified by Filter



Modified Aol-The Math

$$V_{OUT} = \frac{V_O\left(R_{flt} + \frac{1}{sC_{flt}}\right)}{R_O + R_{flt} + \frac{1}{sC_{flt}}}$$

$$\frac{V_{OUT}}{V_O} = K = \frac{\left(R_{flt} + \frac{1}{sC_{flt}}\right)}{R_O + R_{flt} + \frac{1}{sC_{flt}}}$$

$$\frac{V_{OUT}}{V_O} = K = \frac{sC_{flt}R_{flt} + 1}{sC_{flt}\left(R_O + R_{flt}\right) + 1}$$

$$\frac{V_{OUT}}{V_O} = K = \frac{s + \frac{1}{C_{flt}R_{flt}}}{\frac{C_{flt}\left(R_O + R_{flt}\right)}{C_{flt}R_{flt}}s + \frac{1}{C_{flt}R_{flt}}}$$

Modified Aol-The Math – cont.

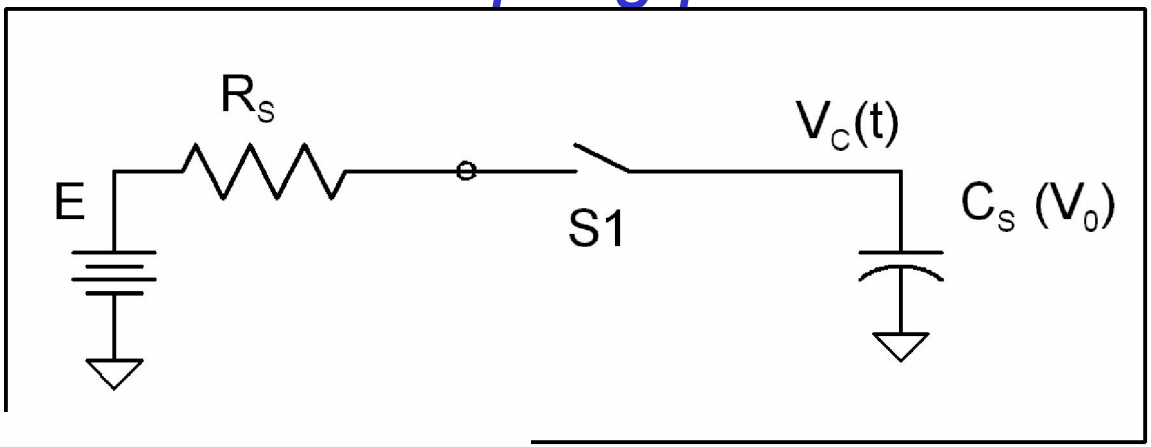
$$\frac{V_{OUT}}{V_O} = K = \frac{\left(s + \frac{1}{C_{flt}R_{flt}}\right)\left(\frac{C_{flt}R_{flt}}{C_{flt}(R_O + R_{flt})}\right)}{s + \left(\frac{1}{C_{flt}R_{flt}}\right)\left(\frac{C_f R_f}{C_{flt}(R_O + R_{flt})}\right)}$$

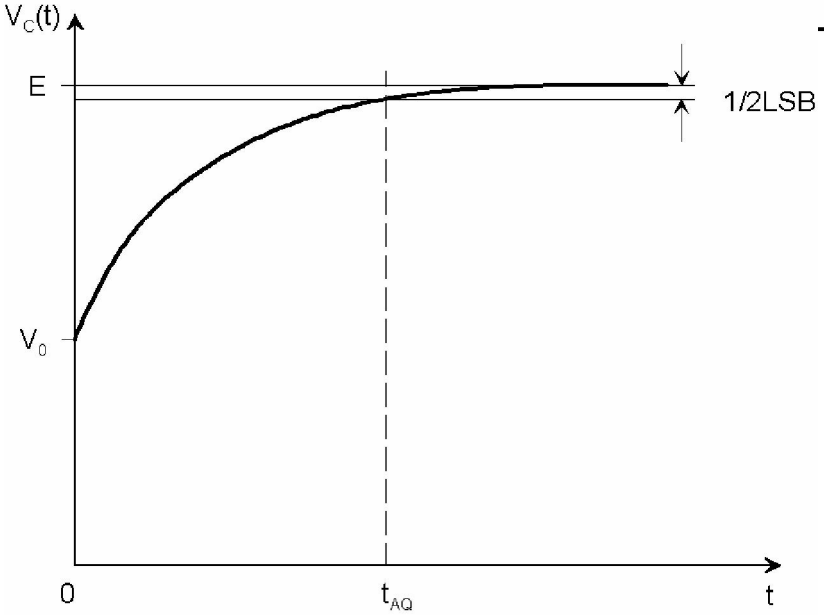
$$\frac{V_{OUT}}{V_O} = K = \frac{\left(s + \frac{1}{C_{flt}R_{flt}}\right)\left(\frac{R_{flt}}{(R_O + R_{flt})}\right)}{s + \left(\frac{1}{C_{flt}R_{flt}}\right)\left(\frac{R_{flt}}{(R_O + R_{flt})}\right)}$$

$$\frac{V_{OUT}}{V_O} = K = \left(\frac{R_{flt}}{(R_O + R_{flt})}\right)\frac{\left(s + \frac{1}{C_{flt}R_{flt}}\right)}{\left(s + \frac{1}{C_{flt}(R_O + R_{flt})}\right)}$$

$$f_p = \frac{1}{2\Pi C_{flt}(R_O + R_{flt})};\ f_z = \frac{1}{2\Pi C_{flt}R_{flt}}$$

Voltage on the sampling capacitor during sampling period





$$V_C(t) = V_0 + (E - V_0) \times (1 - e^{-\frac{t}{\tau}})$$

$$E - V_C(t_{AQ}) \le \frac{1}{2} LSB$$

$$V_C(t_{AQ}) \ge E \times (1 - \frac{1}{2^{17}})$$

$$\tau \le \frac{t_{AQ}}{\ln(\frac{E - V_0}{E} \times 2^{17})}$$