Operational Amplifier
Stability

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HPA Linear Applications
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The Culprits

Capacitive Loads!

Reference Buffers!

High Feedback Network Impedance!

Transimpedance Amplifiers!

High-Source Impedance or Low-Power Circuits!

Attenuators!

Cable/Shield Drive!

MOSFET Gate Drive!
Just Plain Trouble!

Inverting Input Filter??

Output Filter??

Oscillator

\[ \begin{align*}
\text{Vin} &\quad \text{Cin 1u} \\
\text{Rg 10k} &\quad \text{Rf 100k} \\
\text{OPA} &\quad \text{Vout} \\
\text{R1 10k} &\quad \text{R2 49k} \\
\text{C1 10u} &\quad \text{C5 100n} \\
\end{align*} \]
Recognize Amplifier Stability Issues on the Bench

• **Required Tools:**
  - Oscilloscope
  - Step Generator

• **Other Useful Tools:**
  - Gain / Phase Analyzer
  - Network / Spectrum Analyzer
Recognize Amplifier Stability Issues

- Oscilloscope - Transient Domain Analysis:
  - Oscillations or Ringing
  - Overshoots
  - Unstable DC Voltages
  - High Distortion
Recognize Amplifier Stability Issues

- Gain / Phase Analyzer - Frequency Domain: Peaking, Unexpected Gains, Rapid Phase Shifts
Quick Op-Amp Theory and Bode Plot Review
Poles and Bode Plots

- **Pole Location** = $f_p$
- **Magnitude** = -20dB/Decade Slope
  - Slope begins at $f_p$ and continues down as frequency increases
  - Actual Function = -3dB down @ $f_p$
- **Phase** = -45°/Decade Slope through $f_p$
  - Decade Above $f_p$ Phase = -84.3°
  - Decade Below $f_p$ Phase = -5.7°
Zeros and Bode Plots

- **Zero Location** = $f_Z$
- **Magnitude** = +20dB/Decade Slope
  - Slope begins at $f_Z$ and continues up as frequency increases
  - Actual Function = +3dB up @ $f_Z$
- **Phase** = +45°/Decade Slope through $f_Z$
  - Decade Above $f_Z$ Phase = +84.3°
  - Decade Below $f_Z$ Phase = 5.7°
Capacitor Intuitive Model

- **DC $X_C$**
  - OPEN

- **DC < $X_C$ < Hi-f**
  - frequency controlled resistor
  - $X_C = 1/(2\pi fC)$

- **Hi-f $X_C$**
  - SHORT
Inductor Intuitive Model

DC $X_L$

- SHORT

DC < $X_L$ < Hi-f

- frequency controlled resistor
  
  $X_L = 2\pi fL$

Hi-f $X_L$

- OPEN
Op-Amp Intuitive Model

\[ K(f) \]
\[ Ro \]
\[ Rin \]
\[ Vo \]
\[ Vout \]
\[ V_{\text{diff}} \]
\[ + \]
\[ - \]
\[ \text{IN}_+ \]
\[ \text{IN}_- \]

**OPEN-LOOP GAIN/PHASE vs FREQUENCY**

- **Gain**
- **Phase**

**Frequency (Hz)**

- 0.1
- 1
- 10
- 100
- 1k
- 10k
- 100k
- 1M
- 10M

0
-20
-60
-100
-140
-180

160
140
120
100
80
60
40
20
0
-20
-40
-60
-80
-100
-140
-180
Op-Amp Loop Gain Model

\[ V_{OUT}/V_{IN} = Acl = Aol/(1+Aol\beta) \]

If \( Aol >> 1 \) then \( Acl \approx 1/\beta \)

\( Aol \): Open Loop Gain
\( \beta \): Feedback Factor
\( Acl \): Closed Loop Gain
Amplifier Stability Criteria

\[ \frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{A_{\text{o}l}}{1 + A_{\text{o}l}\beta} \]

If: \( A_{\text{o}l}\beta = -1 \)
Then: \( \frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{A_{\text{o}l}}{0} \rightarrow \infty \)

If \( \frac{V_{\text{OUT}}}{V_{\text{IN}}} = \infty \rightarrow \text{Unbounded Gain} \)

Any small changes in \( V_{\text{IN}} \) will result in large changes in \( V_{\text{OUT}} \) which will feed back to \( V_{\text{IN}} \) and result in even larger changes in \( V_{\text{OUT}} \rightarrow \text{OSCILLATIONS \rightarrow INSTABILITY} !! \)

\( A_{\text{o}l}\beta: \text{Loop Gain} \)

\( A_{\text{o}l}\beta = -1 \rightarrow \text{Phase shift of } \pm 180^\circ, \text{Magnitude of } 1 \text{ (0dB)} \)

\( f_{\text{cl}}: \text{frequency where } A_{\text{o}l}\beta = 1 \text{ (0dB)} \)

\( f_{\text{cl}}: \text{frequency where } A_{\text{o}l}\beta = 1 \text{ (0dB)} \)

Stability Criteria:
At \( f_{\text{cl}} \), where \( A_{\text{o}l}\beta = 1 \text{ (0dB)} \), Phase Shift \( < \pm 180^\circ \)
Desired Phase Margin (distance from \( \pm 180^\circ \) Phase Shift) \( \geq 45^\circ \)
What causes amplifier stability issues???
Fundamental Cause of Amplifier Stability Issues

- Too much delay in the feedback network
Cause of Amplifier Stability Issues

- Example circuit with too much delay in the feedback network
Cause of Amplifier Stability Issues

- Real circuit translation of too much delay in the feedback network
Cause of Amplifier Stability Issues

- Same results as the example circuit
How do we determine if our system has too much delay??
Phase Margin

- Phase Margin is a measure of the “delay” in the loop.

![Diagram of phase margin and open-loop gain](image-url)
Damping Ratio vs. Phase Margin

Small-Signal Overshoot vs. Damping Ratio

\[ c(t) \]

\[ \zeta = 0.1 \]

\[ \zeta = 0.2 \]

\[ \zeta = 0.4 \]

\[ \zeta = 0.7 \]

\[ \zeta = 1.0 \]

\[ \zeta = 2.0 \]

\[ \omega_n t \]

<table>
<thead>
<tr>
<th>Phase Margin</th>
<th>Overshoot</th>
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<tbody>
<tr>
<td>90°</td>
<td>0</td>
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<tr>
<td>80°</td>
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<td>70°</td>
<td>5%</td>
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<td>60°</td>
<td>10%</td>
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<td>50°</td>
<td>16%</td>
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<td>37%</td>
</tr>
<tr>
<td>20°</td>
<td>53%</td>
</tr>
<tr>
<td>10°</td>
<td>73%</td>
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</tbody>
</table>

AC Peaking vs. Damping Ratio

Phase Margin | AC Peaking @Wn
---|---
90° | -7dB
80° | -5dB
70° | -4dB
60° | -1dB
50° | +1dB
40° | +3dB
30° | +6dB
20° | +9dB
10° | +14dB

Rate of Closure: Rate at which 1/Beta and AOL intersect

ROC = Slope(1/Beta) − Slope(AOL)

ROC = 0 dB/decade − (-20 dB/decade) = 20 dB/decade
Rate of Closure and Phase Margin

Relationship between the AOL and 1/Beta rate of closure and Loop-Gain (AOL*B) phase margin

- Rate of Closure = 20 dB/decade
- Phase Margin ≥ 45 degrees!
Rate of Closure and Phase Margin

So a pole in AOL or a zero in 1/Beta inside the loop will decrease AOL*B Phase!!

40dB/decade

AOL pole

1/B zero

40dB/decade

1/Beta
Rate of Closure and Phase Margin

AOL Pole

1/Beta Zero

Rate of Closure = 40dB/decade!

Phase Margin ≈ 0 degrees!

Zero in 1/B

Phase Margin ≈ 0 degrees!
Testing for Rate of Closure in SPICE

- Break the feedback loop and inject a small AC signal

Short out the input source

Break the loop with L1 at the inverting input

Inject an AC stimulus through C1
Breaking the Loop
Plotting AOL, 1/Beta, and Loop Gain

AOL = Vo/Vin

1/Beta = Vo/Vfb

AOL*B = Vfb/Vin

Gain (dB)
-40.00
-20.00
0.00
20.00
40.00
60.00
80.00
100.00
120.00

Frequency (Hz)
1.00 14.14k 200.00M

Phase (degree)
0.00
45.00
90.00
135.00
180.00

Phase Margin = 80 degrees
Noise Gain

• Understanding Noise Gain vs. Signal Gain

Signal Gain, $G = -1$

$$\text{NG} = 1 + ISGI = 2$$

Signal Gain, $G = 2$

$$\text{NG} = SG = 2$$

Both circuits have a **NOISE GAIN** (NG) of 2.
Noise Gain

- Noise Gain vs. Signal Gain

Gain of -0.1V/V, Is it Stable?

Signal Gain, $G = -0.1$

Noise Gain, $NG = 1.1$

If it’s unity-gain stable then it’s stable as an inverting attenuator!!!
Capacitive Loads
Capacitive Loads

Unity Gain Buffer Circuits

Circuits with Gain

Vin (V)

Vo (V)

Time (seconds)

Vin (V)

Vo (V)

Time (seconds)
Capacitive Loads – Unity Gain Buffers - Results

Determine the issue:

Pole in AOL!!

ROC = 40dB/decade!!

Phase Margin 0!!

NG = 1V/V = 0dB

AOL + AOL*B

1/B

Pole in AOL

Rate of Closure = 40dB/decade!

Phase Margin = 0.2 degrees!

Phase Margin = 0.2 degrees!
Capacitive Loads – Unity Gain Buffers - Theory

Vin
\( \rightarrow \)
L1 1T
\( \rightarrow \)
C4 1T
\( \rightarrow \)
Vin

\( V^+ \)
\( V^- \)

U1 OPA627E

Vo
\( \rightarrow \)
CLoad 1u

Ro 54

AOL

Vin
\( \rightarrow \)
L1
\( \rightarrow \)
C1
\( \rightarrow \)
Vin

Loaded AOL

Vo
\( \rightarrow \)
CLoad 1u

Ro 54

 Loaded AOL

AOL 1M

C1
 plurals
Capacitive Loads – Unity Gain Buffers - Theory

Transfer function:
\[ W(s) = \frac{1}{1 + R_o C_{\text{load}} s} \]

Loaded AOL Pole

Gain (dB)

Frequency (Hz)

Phase (degrees)

\[ f(pole) = \frac{1}{2 \pi R_o C_{\text{Load}} s} \]
Capacitive Loads – Unity Gain Buffers - Theory

AOL

Loaded AOL =

Gain (dB)

Phase (degrees)

Frequency (Hz)

AOL Load

Gain (dB)

Phase (degrees)

Frequency (Hz)
Stabilize Capacitive Loads – Unity Gain Buffers
Stability Options

Unity-Gain circuits can only be stabilized by modifying the AOL load.
Method 1: Riso
Method 1: Riso - Results

**Theory:** Adds a zero to the Loaded AOL response to cancel the pole

---

Gain (dB)
-40.00
-20.00
0.00
20.00
40.00
60.00
80.00
100.00
120.00

Frequency (Hz)
1.00 10.00 100.00 1.00k 10.00k 100.00k 1.00M 10.00M 100.00M

Phase (degrees)
0.00
45.00
90.00
135.00
180.00

---

Phase Margin = 87.5 degrees!

Rate of Closure = 20 dB/decade

---

Gain (dB) of AOL + AOL*B

Rate of Closure = 20 dB/decade

Phase Margin = 87.5 degrees!
Method 1: Riso - Results

When to use: Works well when DC accuracy is not important, or when loads are very light
Method 1: Riso - Theory
Method 1: Riso - Theory

Transfer function:

\[ \text{Loaded AOL}(s) = \frac{1 + C_{\text{Load}} \cdot R_{\text{iso}} \cdot s}{1 + (R_o + R_{\text{iso}}) \cdot C_{\text{Load}} \cdot s} \]

Pole Equation:

\[ f(\text{pole}) = \frac{1}{2 \pi (R_o + R_{\text{iso}}) \cdot C_{\text{Load}} \cdot s} \]

Zero Equation:

\[ f(\text{zero}) = \frac{1}{2 \pi R_{\text{iso}} \cdot C_{\text{Load}} \cdot s} \]
Method 1: Riso - Theory
Method 1: Riso - Design

Ensure Good Phase Margin:

1.) Find: \( f_{cl} \) and \( f(\text{AOL} = 20\,\text{dB}) \)
2.) Set Riso to create AOL zero:
   - Good: \( f(\text{zero}) = f_{cl} \) for PM \( \approx 45 \) degrees.
   - Better: \( f(\text{zero}) = f(\text{AOL} = 20\,\text{dB}) \) will yield slightly less than 90 degrees phase margin

\[ f_{cl} = 222.74\,\text{kHz} \]
\[ f(\text{AOL} = 20\,\text{dB}) = 70.41\,\text{kHz} \]

Zero Equation:
\[ f(\text{zero}) = \frac{1}{2\cdot\pi\cdot R_{iso}\cdot C_{Load}\cdot s} \]
Method 1: Riso - Design

Ensure Good Phase Margin: Test

\[ f(AOL = 20\, \text{dB}) = 70.41\, \text{kHz} \]

→ \( Riso = 2.26\, \text{Ohms} \)

\[ f(zero) = \frac{1}{2 \cdot \pi \cdot Riso \cdot C_{Load} \cdot s} \]

\[ fcl = 222.74\, \text{kHz} \]

→ \( Riso = 0.715\, \text{Ohms} \)

Zero Equation:
\[ f(zero) = \frac{1}{2 \cdot \pi \cdot Riso \cdot C_{Load} \cdot s} \]

Pole Equation:
\[ f(pole) = \frac{1}{2 \cdot \pi \cdot (R_o + Riso) \cdot C_{Load} \cdot s} \]

Transfer function:
\[ \text{Loaded AOL}(s) = \frac{1}{1 + C_{Load} \cdot Riso \cdot s} \]
\[ 1 + (R_o + Riso) \cdot C_{Load} \cdot s \]

\[ F(zero) = 70.41\, \text{kHz} \]

\[ PM = 84^\circ \]

\[ F(zero) = 222.74\, \text{kHz} \]

\[ PM = 52^\circ \]

Ensure Good Phase Margin: Test
Method 1: Riso - Design

Prevent Phase Dip:

Place the zero less than 1 decade from the pole, no more than 1.5 decades away

Good: 1.5 Decades: \( F(\text{zero}) \leq 35 \times F(\text{pole}) \) \( \rightarrow \) \( Riso \geq \frac{Ro}{34} \) \( \rightarrow \) 70° Phase Shift

Better: 1 Decade: \( F(\text{zero}) \leq 10 \times F(\text{pole}) \) \( \rightarrow \) \( Riso \geq \frac{Ro}{9} \) \( \rightarrow \) 55° Phase Shift

\[ \text{Gain} \text{ (dB)} \]
\[ \text{Phase (deg)} \]
\[ \text{Frequency (Hz)} \]

\( \text{Gain} \text{ (dB)} \)
\[ -40 \]
\[ -20 \]
\[ 0 \]
\[ 20 \]
\[ 40 \]
\[ 60 \]
\[ 80 \]
\[ 100 \]
\[ 120 \]

\( \text{Phase (deg)} \)
\[ 0 \]
\[ 45 \]
\[ 90 \]
\[ 135 \]
\[ 180 \]

\( \text{Frequency (Hz)} \)
\[ 1 \]
\[ 10 \]
\[ 100 \]
\[ 1 \text{kHz} \]
\[ 10 \text{kHz} \]
\[ 100 \text{kHz} \]
\[ 1 \text{MHz} \]
\[ 10 \text{MHz} \]
\[ 100 \text{MHz} \]

\( \text{Riso} = \frac{Ro}{9} \)

\( \text{F(pole)} = 2.65 \text{kHz} \)

\( \text{F(zero)} = 26.5 \text{kHz} \)

\( \text{PM_{min}} = 35° \)

\( \text{Riso} = \frac{Ro}{34} \)

\( \text{F(pole)} = 2.86 \text{kHz} \)

\( \text{F(zero)} = 100.2 \text{kHz} \)

\( \text{PM_{min}} = 20° \)
Method 1: Riso - Design

Prevent Phase Dip: Ratio of Riso to Ro

If $\text{Riso} \geq 2\text{Ro} \rightarrow F(\text{zero}) = 1.5 F(\text{pole}) \rightarrow \sim 10^\circ \text{Phase Shift}$

**Almost completely cancels the pole.**

\[
\text{Riso} = \text{Ro} \times 2
\]

**Phase Shift vs. Riso/Ro**

**PM_{min} = 80^\circ**
Method 1: Riso – Design Summary

Summary:

1.) Ensure stability by placing Fzero \leq F(AOL=20dB)
2.) If Fzero is > 1.5 decades from F(pole) then increase Riso up to at least Ro/34
3.) If loads are very light consider increasing Riso > Ro for stability across all loads

Final Circuit

Gain (dB)

Phase (degrees)

Frequency (Hz)
Method 1: Riso - Disadvantage

Disadvantage:

Voltage drop across Riso may not be acceptable
Method 2: Riso + Dual Feedback

U1 OPA627E

Rf 49k

Cf 100n

VG1

V+ V-

VLoad

Riso 6

Vo

VLoad

CLoad 1u
Method 2: Riso + Dual Feedback

Theory: Features a low-frequency feedback to cancel the Riso drop and a high-frequency feedback to create the AOL pole and zero.

Gain (dB)
-40.00
-20.00
0.00
20.00
40.00
60.00
80.00
100.00
120.00

Frequency (Hz)
1.00 10.00 100.00 1.00k 10.00k 100.00k 1.00M 10.00M 100.00M

Phase [deg]
0.00
45.00
90.00
135.00
180.00

Rate of Closure = 20dB/decade
Phase Margin = 87.5 degrees!
Method 2: Riso + Dual Feedback

When to Use: Only practical solution for very large capacitive loads $\geq 10\mu F$

When DC accuracy must be preserved across different current loads
**Method 2: Riso + Dual Feedback - Design**

**Ensure Good Phase Margin:**

1.) Find: $f_{cl}$ and $f(AOL = 20dB)$
2.) Set Riso to create AOL zero:
   - Good: $f(\text{zero}) = Fcl$ for PM $\approx 45$ degrees.
   - Better: $f(\text{zero}) = F(AOL = 20dB)$ will yield slightly less than 90 degrees phase margin
3.) Set $R_f$ so $R_f >> Riso$
   \[ R_f \geq (Riso \times 100) \]
4.) Set $C_f \geq (200 \times Riso \times C_{load})/R_f$

\[ f_{cl} = 222.74kHz \]
\[ f(AOL = 20dB) = 70.41kHz \]

**Zero Equation:**
\[ f(\text{zero}) = \frac{1}{2 \cdot \pi \cdot R_{iso} \cdot C_{Load} \cdot s} \]
Method 2: Riso + Dual Feedback - Summary

Ensure Good Phase Margin (Same as “Riso” Method):

1.) Set Riso so \( f(\text{zero}) = F(\text{AOL} = 20\, \text{dB}) \)
2.) Set \( Rf \): \( Rf \geq (\text{Riso} \times 100) \)
3.) Set \( Cf \): \( Cf \geq (200 \times \text{Riso} \times \text{Cload})/Rf \)

Phase Margin \( = 87.5\, \text{degrees}! \)
Capacitive Loads – Circuits with Gain
Capacitive Loads – Circuits with Gain

![Circuit Diagram]

- $R_g = 4.99k$
- $R_f = 100k$
- $V_+\rightarrow V_G1\rightarrow 0$
- $C_{load} = 100n$
- $V_{out} = \text{Vo}$

![Graph]

- Voltage (V)
- Time (seconds)

- $V_+\rightarrow \text{U1 OPA627E}\rightarrow V_-$
- $V_{out} = \text{Vo}$
Capacitive Loads – Circuits With Gain - Results

Same Issues as Unity Gain Circuit

Pole in AOL!!

ROC = 40dB/decade!!

Phase Margin = 10°!!
Stabilize Capacitive Loads – Circuits with Gain
Stability Options – Circuits with Gain

Circuits with gain can be stabilized by modifying the AOL load and by modifying 1/Beta.
Method 1 + Method 2

Methods 1 and 2 work on circuits with gain as well!

Method 1: Riso

Method 2: Riso+Dual Feedback
Method 3: Cf
Method 3: Cf - Results

Theory: 1/Beta compensation. Cf feedback capacitor causes 1/Beta to decrease at -20dB/decade and if placed correctly will cause the ROC to be 20dB/decade.
Method 3: Cf - Results

When to use: Especially effective when NG is high, ≥ 30dB.

- Systems where a bandwidth limitation is not an issue
- Limits closed-loop bandwidth at 1/(2*π*Rf*Cf)
Method 3: Cf - Design

Ensure Good Phase Margin:

For 20dB/decade ROC, 1/Beta must intersect AOL while its slope is -20dB/decade. Therefore:

\[ f(1/B \text{ pole}) < f(\text{cl}_\text{unmodified}) \]
\[ f(1/B \text{ zero}) > f(AOL = 0dB) \]

\[ f(\text{cl}_\text{unmodified}) = 152.13kHz \]
\[ f(AOL = 0dB) = 704.06kHz \]

**1/B Pole Equation:**

\[ f(1/B \text{ pole}) = \frac{1}{2\pi R_f C_f} \]

**1/B Zero Equation:**

\[ f(1/B \text{ zero}) = \frac{1}{2\pi (R_g || R_f) C_f} \]
Method 3: Cf - Design

Ensure Good Phase Margin:

1.) Find \( f(AOL=0\text{dB}) \)
2.) Set \( f(1/B \text{ zero}) \) by choosing \( Cf \):
   - Good: Set \( f(1/B \text{ zero}) = f(AOL = 0\text{dB}) \) for \( PM \approx 45 \text{ degrees.} \)
   - Better: Set \( f(1/B \text{ zero}) \) so \( AOL @ f(cl) = \frac{1}{2} \) Low-Frequency NG in dB

\[ f(AOL = 0\text{dB}) = 704.06\text{kHz} \]

1/B Zero Equation:
\[
f(1/B \text{ zero}) = \frac{1}{2\pi R_g || R_f \cdot C_f}
\]
Method 3: Cf – Design - Summary

Summary:

1.) Ensure stability by placing:
   a) \( f(1/B \text{ zero}) \geq f(\text{AOL} = 0dB) \)
   b) \( f(1/B \text{ pole}) \leq f(\text{cl\_unmodified}) \)
2.) Try to adjust the zero location so the \( 1/B \) curve crosses the AOL curve in the middle of the \( 1/B \) span allowing for shifts in AOL

![Final Circuit](image)

![Graph](image)
Method 4: Noise-Gain

\[ \begin{align*}
    &\text{Rg } 4.99k \\
    &\text{Rn } 75 \\
    &\text{Cn } 820n \\
    &\text{VG1} \\
    &\text{Vo} \\
    &\text{Rf } 100k \\
    &\text{CLoad } 100n \\
\end{align*} \]
Method 4: Noise Gain - Results

Theory: 1/Beta compensation. Raise high-frequency 1/Beta so the ROC occurs before the AOL pole causes the AOL slope to change.

Gain (dB)
-40.00
-20.00
0.00
20.00
40.00
60.00
80.00
100.00
120.00

Frequency (Hz)
1.00 10.00 100.00 1.00k 10.00k 100.00k 1.00M 10.00M 100.00M

Phase (°)
0.00
45.00
90.00
135.00
180.00

ROC = 20 dB/decade
PM = 56°
**Method 4: Noise Gain - Results**

**When to use:** Better for lighter capacitive loading

When \( \text{AOL} @ f(\text{AOL pole}) < (\text{Closed loop gain} + 20\text{dB}) \)

Due to the increase in noise gain, this approach may not be practical when required noise gain is greater than the low-frequency signal gain by more than \(~25-30\text{dB}.)\n
---

![Circuit Diagram](image)
Method 4: Noise Gain - Design

Ensure Good Phase Margin:

For 20dB/decade ROC, 1/Beta must intersect AOL above the AOL pole. Therefore:

$$|\text{High-Freq NG}| > |\text{AOL}| @ f(\text{AOL pole})$$

$$f(1/B \text{ zero}) < f(\text{AOL} = \text{High-Freq NG})$$

$$|\text{AOL}| @ f(\text{AOL pole}) = 52.11\text{dB}$$

$$f(\text{AOL pole}) = 29.49\text{kHz}$$

High-Freq Noise-Gain Equation:

$$\text{HF NG} = \frac{R_f}{(R_g || R_n)}$$

1/B Zero Equation:

$$f(1/B \text{ zero}) = \frac{1}{2 \pi R_n C_n}$$

1/B Pole Equation:

$$f(1/B \text{ pole}) = \frac{1}{2 \pi (R_n + (R_g || R_f) C_f)}$$

Frequency (Hz)

Voltage (V)

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<th>Frequency (Hz)</th>
<th>Voltage (V)</th>
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<tbody>
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<td>1.00</td>
<td>-40.00</td>
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<tr>
<td>10.91</td>
<td>-20.00</td>
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<tr>
<td>118.92</td>
<td>0.00</td>
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<tr>
<td>1.30k</td>
<td>20.00</td>
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<tr>
<td>14.14k</td>
<td>40.00</td>
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<tr>
<td>154.22k</td>
<td>60.00</td>
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<tr>
<td>1.68M</td>
<td>80.00</td>
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<tr>
<td>18.34M</td>
<td>100.00</td>
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<td>200.00M</td>
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Gain (dB)

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<thead>
<tr>
<th>Frequency (Hz)</th>
<th>Gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>100</td>
</tr>
<tr>
<td>10.91</td>
<td>10</td>
</tr>
<tr>
<td>118.92</td>
<td>1</td>
</tr>
<tr>
<td>1.30k</td>
<td>100k</td>
</tr>
<tr>
<td>14.14k</td>
<td>10k</td>
</tr>
<tr>
<td>154.22k</td>
<td>1k</td>
</tr>
<tr>
<td>1.68M</td>
<td>10M</td>
</tr>
<tr>
<td>18.34M</td>
<td>100M</td>
</tr>
<tr>
<td>200.00M</td>
<td>1M</td>
</tr>
</tbody>
</table>
Method 4: Noise Gain - Design

Ensure Good Phase Margin:

1.) Find \( f(AOL \text{ pole}) \) and \(|AOL| @ f(AOL \text{ pole})\)

2.) Set High-Freq Noise-Gain by choosing \( R_n \):
   
   Good: \( |HF \ NG| \geq |AOL| @ f(AOL \text{ pole}) \)
   
   Better: \( |HF \ NG| \geq |AOL| @ f(AOL \text{ pole}) + 10\text{dB} \)

\[ |AOL| @ f(AOL \text{ pole}) = 52.11\text{dB} \]

\( f(AOL \text{ pole}) = 29.49\text{kHz} \)

High-Freq Noise-Gain Equation:

\[ HF \ NG = \frac{R_f}{(R_g || R_n)} \]
Method 4: Noise Gain - Design

Ensure Good Phase Margin:

3.) Find $f(\text{cl}\_\text{modified}) = f(\text{AOL} @ |\text{HF NG}|)$
4.) Set $f(1/B \text{ zero})$ by choosing $C_n$:
   - Good: $f(1/B \text{ zero}) \leq f(\text{cl}\_\text{modified})$
   - Better: $f(1/B \text{ zero}) \leq f(\text{cl}\_\text{modified}) / 3.5$ (~ ½ decade)

\[ f(\text{cl}\_\text{modified}) = 29.49kHz \]

High-Freq Noise-Gain Equation:

\[ \text{HF NG} = \frac{R_f}{(R_g \parallel R_n)} \]
Method 4: Noise Gain - Summary

Summary:

1.) Ensure stability by setting:
   a) \(|HF \text{ NG}| \geq (|AOL| @ f(AOL pole) + 10\, \text{dB})
   b) \(f(1/B \text{ zero}) \leq f(\text{cl_modified}) / 3.5\)

Final Circuit

![Final Circuit Diagram](attachment://diagram.png)

Gain (dB) vs Frequency (Hz)

-40.00 -20.00 0.00 20.00 40.00 60.00 80.00 100.00 120.00

-40 -20 0 20 40 60 80 100 120

Phase (degrees) vs Frequency (Hz)

0.00 45.00 90.00 135.00 180.00

PM = 56°

Frequency (Hz)

1.00 10.00 100.00 1.00k 10.00k 100.00k 1.00M 10.00M 100.00M
Method 4: Noise Gain

Quick reminder that inverting and non-inverting noise gain circuits are different!

![Noise Gain Diagram]

![Time vs Voltage Graph]
Circuits with High Feedback Network Impedance
Circuits with High Feedback Network Impedance
Circuits with High Feedback Network Impedance

Determine the issue:
Zero in 1/Beta!!
ROC = 40dB/decade!!
Phase Margin 2!!
Circuits with High Feedback Network Impedance - Theory
Circuits with High Feedback Network Impedance - Theory

Beta Pole & 1/Beta Zero Equation:
\[ f(B \text{ pole}) = f(1/B \text{ zero}) = \frac{1}{2\pi R_g R_f C_{in}} \]

Gain (dB)

\[ \begin{array}{c|c|c|c|c|c|c|c|c|c|c|c} \hline \text{Frequency (Hz)} & 1 & 10 & 100 & 1k & 10k & 100k & 1M & 10M & 100M \\ \hline \text{Gain (dB)} & -80.00 & -60.00 & -40.00 & -20.00 & 0.00 \\ \hline \end{array} \]

Phase (degrees)

\[ \begin{array}{c|c|c|c|c|c|c|c|c|c|c} \hline \text{Frequency (Hz)} & 1 & 10 & 100 & 1k & 10k & 100k & 1M & 10M & 100M \\ \hline \text{Phase (degrees)} & -90.00 & -45.00 & 0.00 \\ \hline \end{array} \]
Stabilize Circuits With High Feedback Network Impedance
Stability Options – Zero in 1/Beta

The only practical option is to add a pole to cancel the 1/Beta Zero
Method 1: Cf

![Circuit Diagram]

- **U1 OPA627E**
- **Rf 499k**
- **Rg 499k**
- **Cf 21p**
- **Cstray 20p**
- **VG1**
- **Vo**
Method 1: Cf - Results

Theory: 1/Beta compensation. Cf feedback places a pole in 1/Beta to cancel the zero from the input capacitance.
Method 1: Cf - Results

When to use: Almost always a safe design practice.
Limits gain at $1/(2\pi Rf Cf)$

When to use: Almost always a safe design practice.
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When to use: Almost always a safe design practice.
Limits gain at $1/(2\pi Rf Cf)$
Method 1: Cf - Design

Ensure Good Phase Margin:

For 20dB/decade ROC, the $1/\text{Beta}$ pole must flatten the $1/\text{Beta}$ Zero before $f(\text{cl})$. Therefore $f(1/\text{Beta pole}) \leq f(\text{cl})$

\[ f(\text{cl}) = 445.6\text{kHz} \]

1/B Pole Equation:
\[ f(1/B \text{ pole}) = \frac{1}{2\pi R_f C_f} \]

1/B Zero Equation:
\[ f(1/B \text{ zero}) = \frac{1}{2\pi \left(R_g || R_f\right) C_{in}} \]
Method 1: Cf - Design

Ensure Good Phase Margin:

1.) Find \( f(\text{cl}) \)
2.) Set \( f(1/B \text{ pole}) \) by setting \( \text{Cf} \):
   - Good: \( f(1/B \text{ pole}) \leq f(\text{cl}) \)
   - Better: \( f(1/B \text{ pole}) \leq f(\text{cl})/3.5 \) (~ \( \frac{1}{2} \) decade)

1/B Pole Equation:
\[
f(1/B \text{ pole}) = \frac{1}{2\pi R_f C_f}
\]

1/B Zero Equation:
\[
f(1/B \text{ zero}) = \frac{1}{2\pi (R_g + R_f)} C_{\text{in}}
\]
Method 1: Cf - Summary

Summary:

1.) Ensure stability by setting $f(1/B \text{ pole}) \leq f(\text{cl})/3.5$ ($\sim \frac{1}{2}$ decade)
Ro vs. Zo
When Ro is really Zo!!

Vos 80.0432u
U1 OPA627E
Vo
Vos -25.3845uV
U1 OPA2376
Vo

Open-Loop Output Impedance vs Frequency

Open-Loop Output Resistance vs Frequency

400μA Load
2mA Load
With Complex Zo, Accurate Models are Key!

Gain (dB)
-60.00
-40.00
-20.00
0.00
20.00
40.00
60.00
80.00
100.00
120.00
140.00

Phase (degrees)
-90.00
-45.00
0.00
45.00
90.00
135.00
180.00

Frequency (Hz)
1.00 10.00 100.00 1.00k 10.00k 100.00k 1.00M 10.00M 100.00M

PM = -77°!!
ROC = 60dB/decade!
AOL + AOL*B

Vo (V)

Vin (V)

Time (seconds)

V1

Vin

Vo

AOL*B

Phase

Vo (V)

Vin (V)

Time (seconds)

Gain (dB)

Phase (degrees)
With Complex Zo, Accurate Models are Key!

Vos -25.3845uV

U1 OPA2376

Gain (dB)

Frequency (Hz)
Questions/Comments?

Thank you!!

Special Thanks to:
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PA Apps Team