Op Amp Glossary of Terms
Part I: Chart Specs
Thatcher Klumpp, Aug. 22, 1995

Table of Contents

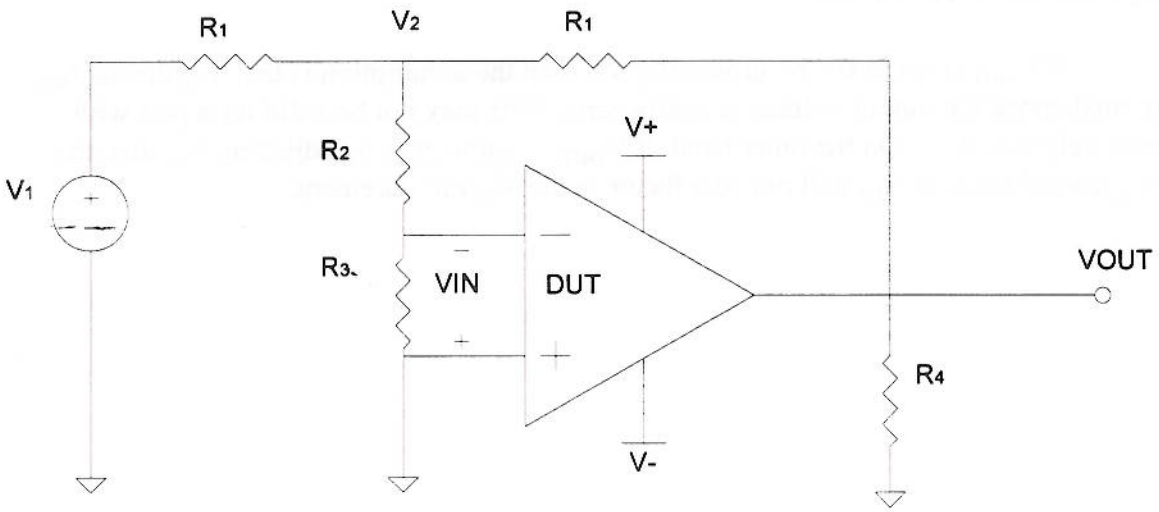
Parameter: Input Offset Voltage (V_{OS})

Definition: The differential input voltage required for zero output voltage when the common-mode voltage is zero, power supplies are at the specified level and the temperature is 25 °C.

See Appendix A for a discussion of the components of the differential input voltage V_{IN}.

Test Circuit:

See Appendix B for suggested resistor values and a discussion of the assumptions associated with the circuit below.



Test Conditions:

- Set the power supplies to the specified value.
- Adjust V_1 for $V_{OUT} = 0V$.
- Choose R_4 to establish the specified load: $R_{LOAD} \cong R_4 || R_1$.
- T = 25 °C

Test Method:

- Measure V_2.
- Calculate V_{OS}.

$$V_{OS} = \frac{-V_2}{1 + \frac{R_2}{R_3}}$$

Special Considerations:

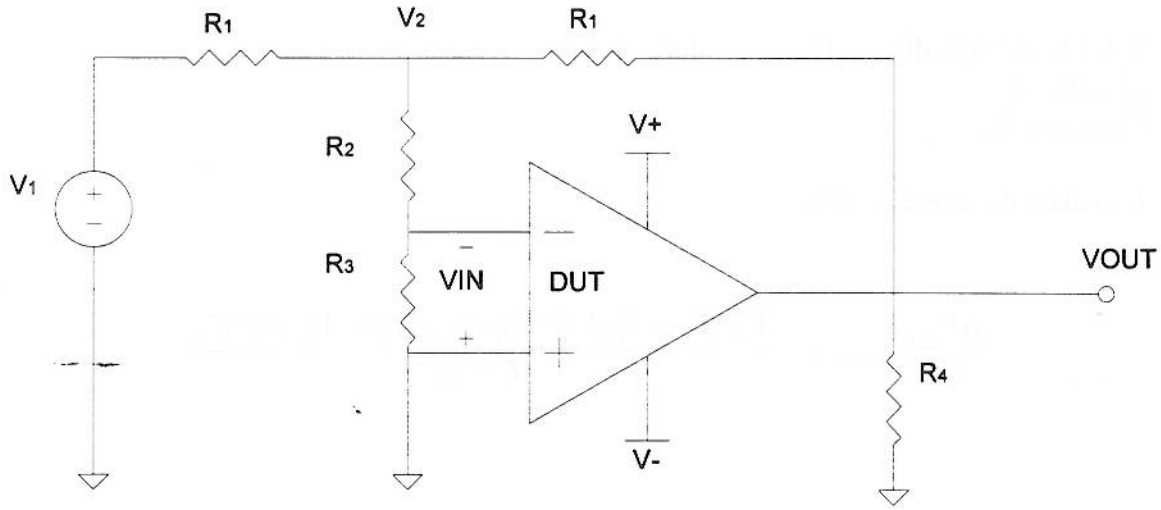
If V_{OUT} is set to 0V by grounding V_1, then the assumption is that V_{IN} due to A_{OL} is small since the output voltage is nearly zero. This may not be valid for a part with relatively low A_{OL}. On the other hand, if V_{OUT} is set to zero by adjusting V_1, then the A_{OL} contribution to V_{IN} will not be a factor in the V_{IN} measurement.

Parameter: Input Offset Voltage Drift (due to temperature)

Definition: The change of V_{OS} with temperature:

$$DRIFT_{TEMP} = \frac{\Delta V_{OS}}{\Delta T}$$

Test Circuit:



Test Conditions:

- Set the power supplies to the specified value.
- Adjust V_1 for $V_{OUT} = 0V$.
- Choose R_4 to establish the specified load: $R_{LOAD} \cong R_4 || R_1$.

Test Method:

The test procedure outlined below describes a three-point averaging technique of V_{OS} drift with temperature. V_{OS} is measured at three points; they are the specified hot temperature, the specified cold temperature and room temperature (25 °C). The subsequent calculation averages the absolute drift of V_{OS} over two temperature ranges: room temperature to the specified hot temperature and room temperature to the specified cold temperature.

- Set T = 25 °C.
- Measure V_2.
- Calculate V_{OS}(25 °C):

$$V_{OS}(25°C) = \frac{-V_2}{1 + \frac{R_2}{R_3}}$$

- Set T to the specified hot temperature (T_1).
- Measure V_2.
- Calculate $V_{OS}(T_1)$.

- Set T to the specified cold temperature (T_2).
- Measure V_2.
- Calculate $V_{OS}(T_2)$.

- Calculate the average drift.

$$\frac{\Delta V_{OS}}{\Delta T}\Big|_{AVERAGE} = \frac{|V_{OS}(T_1) - V_{OS}(25°C)| + |V_{OS}(T_2) - V_{OS}(25°C)|}{|T_1 - T_2|}$$

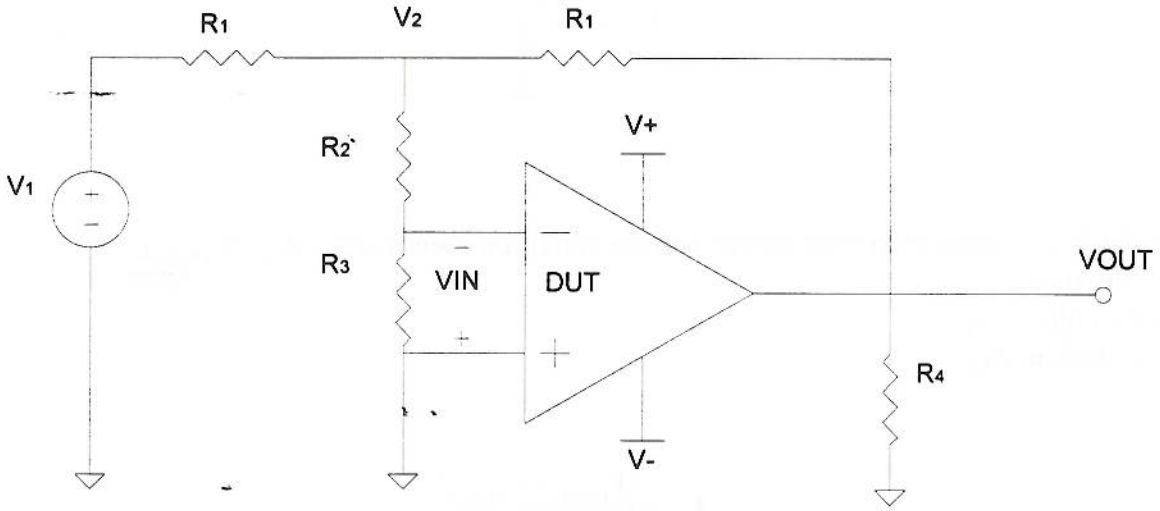
Special Considerations:

Parameter: Open-Loop Voltage Gain (A_{OL})

Definition: The change of V_{OUT} with V_{IN}.

$$A_{OL} = \frac{\Delta V_{OUT}}{\Delta V_{IN}}$$

Test Circuit:



Test Conditions:

- Set the power supplies to the specified value.
- Choose R_4 to establish the specified load: $R_{LOAD} \cong R_4 \| R_1$.
- T = 25 °C

Test Method:

- Set V_{OUT} to the maximum output voltage condition specified for A_{OL} (V_{OUT1}).
- Measure V_2.
- Calculate V_{IN1}.

$$V_{IN} = \frac{-V_2}{1 + \frac{R_2}{R_3}}$$

- Set V_{OUT} to the minimum output voltage condition specified for A_{OL} (V_{OUT2}).
- Measure V_2.
- Calculate V_{IN2}.
- Calculate A_{OL}:

$$A_{OL} = \left| \frac{V_{OUT1} - V_{OUT2}}{V_{IN1} - V_{IN2}} \right|$$

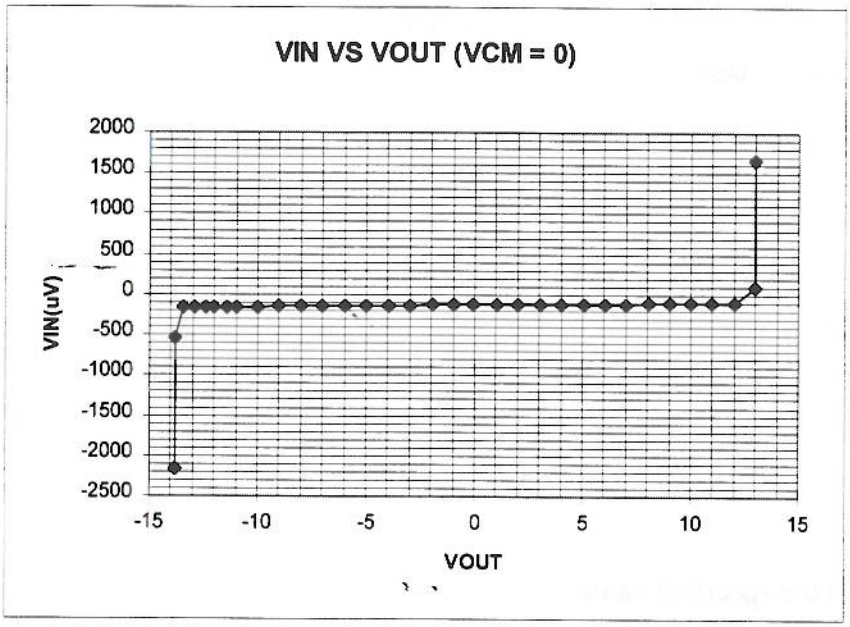
Special Considerations:

< Burr-Brown Notes >

- Use more than two points to test units known to have a unique V_{IN} versus V_{OUT} characteristic.

- Determining V_{OUT1} and V_{OUT2}.

Use the test method described for A_{OL} to generate a plot of V_{IN} versus V_{OUT}.

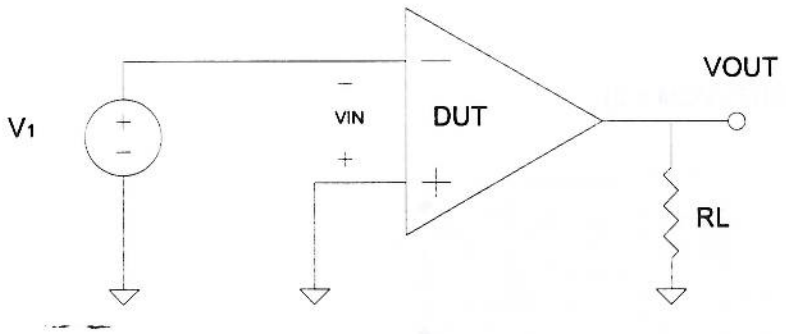


Draw a line with positive slope equal to the guaranteed minimum A_{OL} and passing through V_{IN} at V_{OUT} = 0V. Draw a second line with negative slope equal in magnitude to the guaranteed minimum A_{OL} and passing through V_{IN} at V_{OUT} = 0V. The resulting "butterfly graph" defines the linear operation of the unit. The output voltage at the points where the plot exits the allowable error band delimits the A_{OL} test conditions.

Parameter: Voltage Output (Positive, Negative)

Definition: Positive Output Voltage: The output voltage when V_{IN} is 500 mV.
Negative Output Voltage: The output voltage when V_{IN} is -500 mV.

Test Circuit:



Test Conditions:

- Set the power supplies to the specified value.
- Choose R_L to establish the specified load.
- T = 25 °C

Test Method:

- Set V_1 to +500mV.
- Measure V_{OUT}. This is the negative output voltage swing.
- Set V_1 to -500mV.
- Measure V_{OUT}. This is the positive output voltage swing.

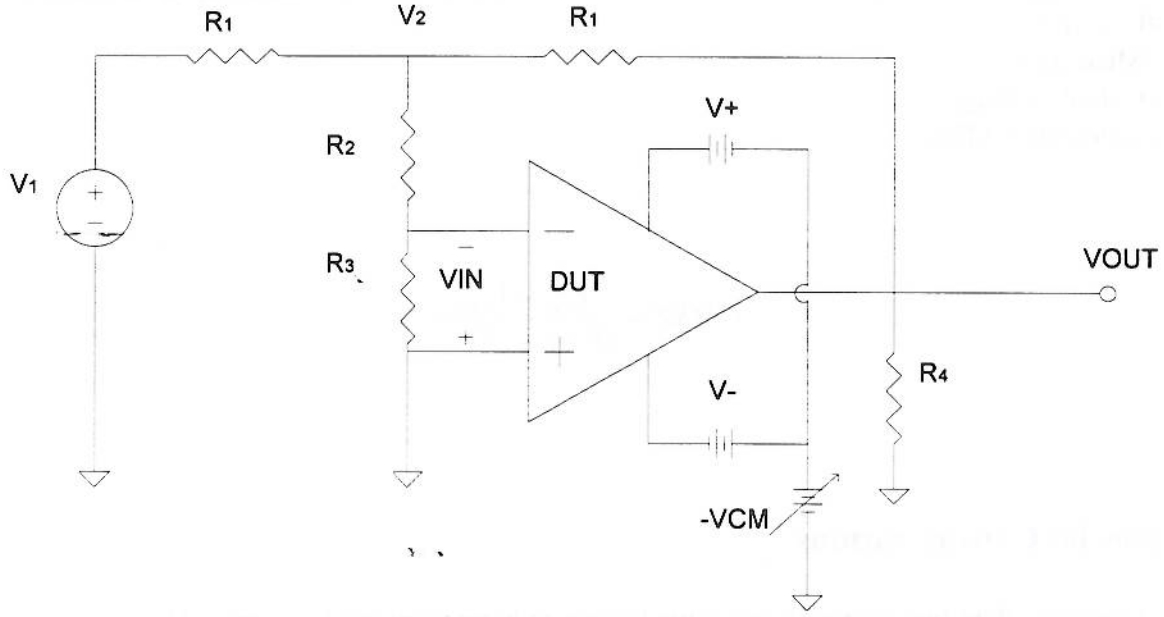
Special Considerations:

Parameter: Common-Mode Rejection Ratio (CMRR)

Definition: The change of V_{IN} with V_{CM}:

$$CMRR = \frac{\Delta V_{IN}}{\Delta V_{CM}}$$

Test Circuit:



Test Conditions:

- Set V+ and V- to the specified values.
- Choose R_4 to establish the specified load: $R_{LOAD} \cong R_4 || R_1$.
- T = 25 °C

Test Method:

- Set $-V_{CM}$ to the negative of the maximum guaranteed common-mode voltage.
- Set V_{OUT} equal to $-V_{CM}$ by adjusting V_1. This equivalent to maintaining the condition of $V_{OUT} = 0$.
- Measure V_2.
- Calculate V_{IN1}.

$$V_{IN} = \frac{-V_2}{1 + \frac{R_2}{R_3}}$$

- Set $-V_{CM}$ to the negative of the minimum guaranteed common-mode voltage.
- Set V_{OUT} equal to $-V_{CM}$ by adjusting V_1. This is equivalent to maintaining the condition of $V_{OUT} = 0$.
- Measure V_2.
- Calculate V_{IN2}.
- Calculate CMRR.

$$CMRR = \frac{V_{IN1} - V_{IN2}}{(V+)_1 - (V+)_2}$$

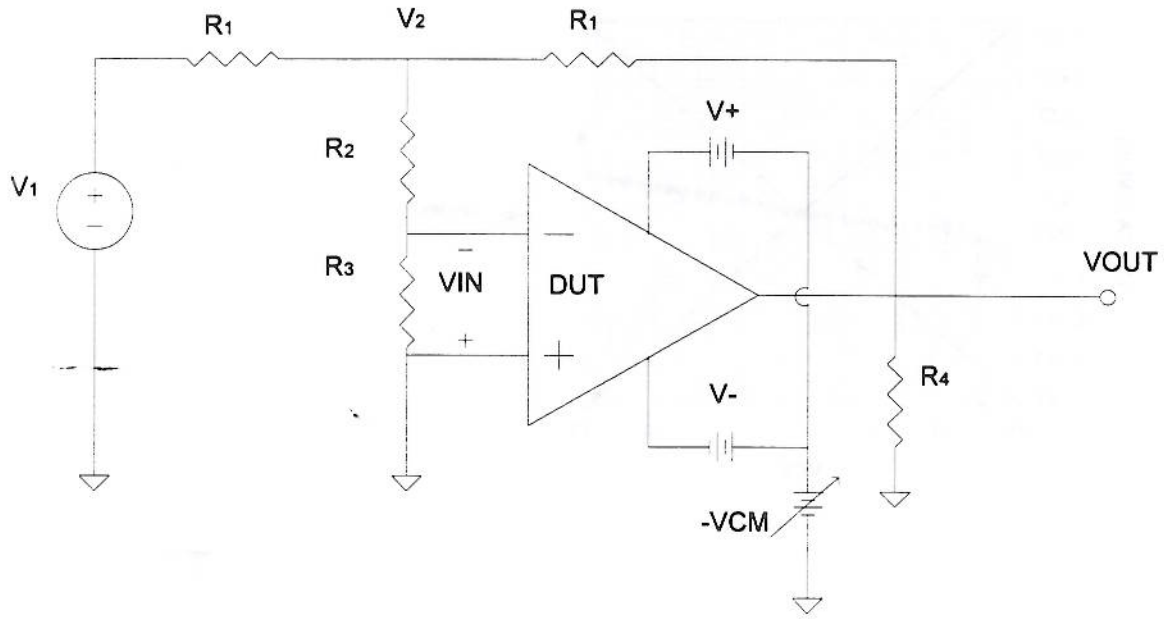
Special Considerations:

- Use more than two points to test units known to have a unique V_{IN} versus V_{CM} characteristic.

Parameter: Common-Mode Voltage Range

Definition: The maximum and minimum voltage levels common to both the inverting and noninverting inputs that may be applied without exceeding an error band defined by the minimum CMRR specification.

Test Circuit:

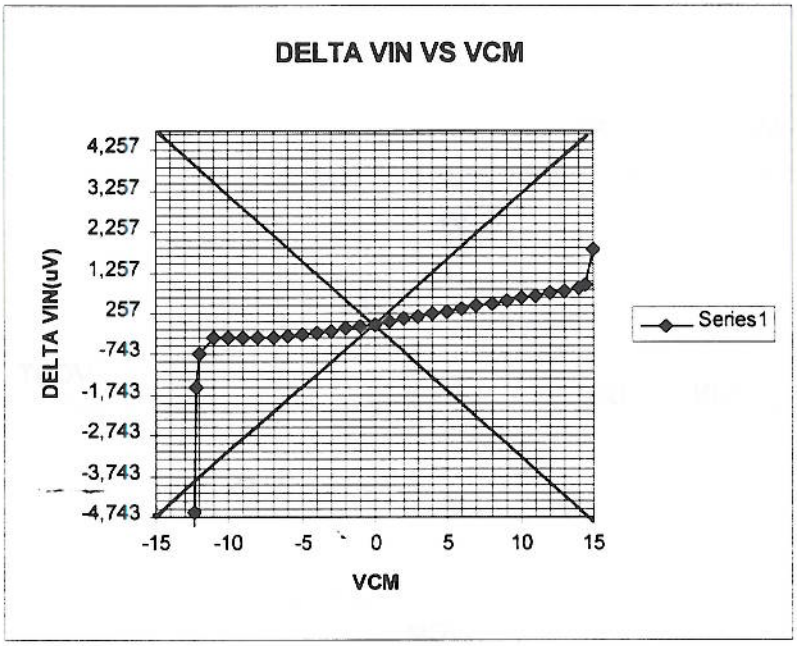


Test Conditions:

- Set V+ and V- to the specified values.
- Adjust V_1 for $V_{OUT} = 0V$.
- Choose R_4 to establish the specified load: $R_{LOAD} \cong R_4 \| R_1$.
- T = 25 °C

Test Method:

-Use the test method for CMRR to generate a plot of ΔV_{IN} versus V_{CM}:
- Plot the difference between the differential input voltage at a given common-mode voltage and the initial offset voltage.



Draw a line with positive slope equal to the guaranteed minimum CMRR and passing through V_{IN} at V_{CM} = 0V. Draw a second line with negative slope equal in magnitude to the guaranteed minimum CMRR and passing through V_{IN} at V_{CM} = 0V. The resulting "butterfly graph" defines the allowable error band of the unit. The common-mode voltage at the points where the plot exits the allowable error band delimits the common-mode range of the op amp.

Special Considerations:

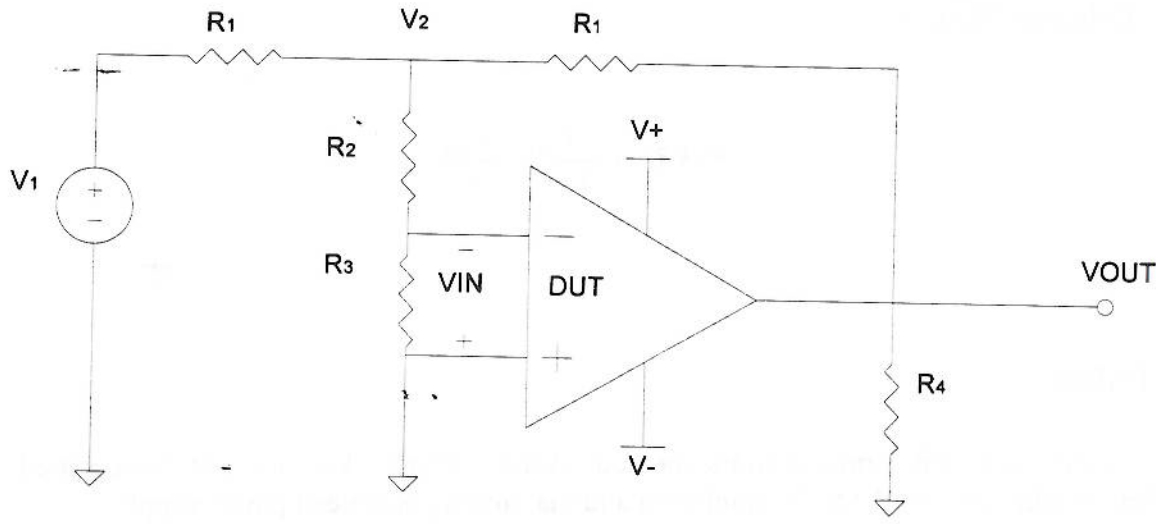
Parameter: Power Supply Rejection Ratio (PSRR)

Definition: The change of V_{IN} with V+ or V-:

$$PSRR^{+} = \frac{\Delta V_{IN}}{\Delta(V+)}$$

$$PSRR^{-} = \frac{\Delta V_{IN}}{\Delta(V-)}$$

Test Circuit:



Test Conditions:

- Adjust V_1 for $V_{OUT} = 0V$.
- Choose R_4 to establish the specified load: $R_{LOAD} \cong R_4 || R_1$.
- T = 25 °C

Test Method:

$PSRR^+$

- Set (V-) to the specified value.
- Set (V+) to the maximum guaranteed supply voltage level $(V+)_1$.
- Measure V_2.
- Calculate V_{IN1}.

$$V_{IN} = \frac{-V_2}{1 + \frac{R_2}{R_3}}$$

- Set (V+) to the minimum guaranteed supply voltage level $(V+)_2$.
- Measure V_2.
- Calculate V_{IN2}.
- Calculate $PSRR^+$:

$$PSRR^+ = \frac{V_{IN1} - V_{IN2}}{(V+)_1 - (V+)_2}$$

$PSRR^-$

- Determine $PSRR^-$ similarly to the method given for $PSRR^+$; keep (V+) at the specified level while setting (V-) to the minimum and maximum guaranteed power supply voltages.

$$PSRR^- = \frac{V_{IN1} - V_{IN2}}{(V-)_1 - (V-)_2}$$

PSRR

- Determine PSRR similarly to the method given for $PSRR^+$ and $PSRR^-$; set both (V+) and (V-) to the minimum and maximum guaranteed power supply voltages.

$$PSRR = \frac{V_{IN1} - V_{IN2}}{2((V+)_1 - (V+)_2)}$$

Special Considerations:

- Use more than two points to test units known to have a unique V_{IN} versus (V+) or (V-) characteristic.

Parameter: Power Supply Operating Voltage Range

Definition: Text to come from Bruce Trump.

Parameter: Input Bias Current (I_B^+ and I_B^-)

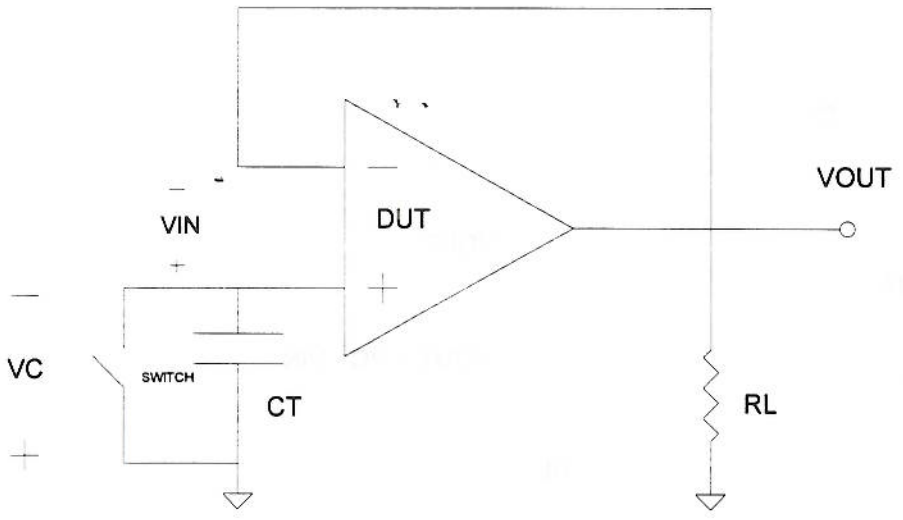
Definition: I_B^+: The current that flows into the noninverting input of the op amp.
I_B^-: The current that flows into the inverting input of the op amp.

Note: Two approaches are given to measure bias current. One implements a capacitor integration technique and the other uses a large resistor to establish a measurable voltage drop. The integration method should be used for FET-input amplifiers and the large resistor method should be used for bipolar-input amplifiers.

Test Conditions:

- Set the power supplies to the specified value.
- Choose R_4 to establish the specified load: $R_{LOAD} \cong R_4 || R_1$.
- T = 25 °C

Test Circuit (I_B^+):(Integration method)



VOUT = -(VC + VIN)

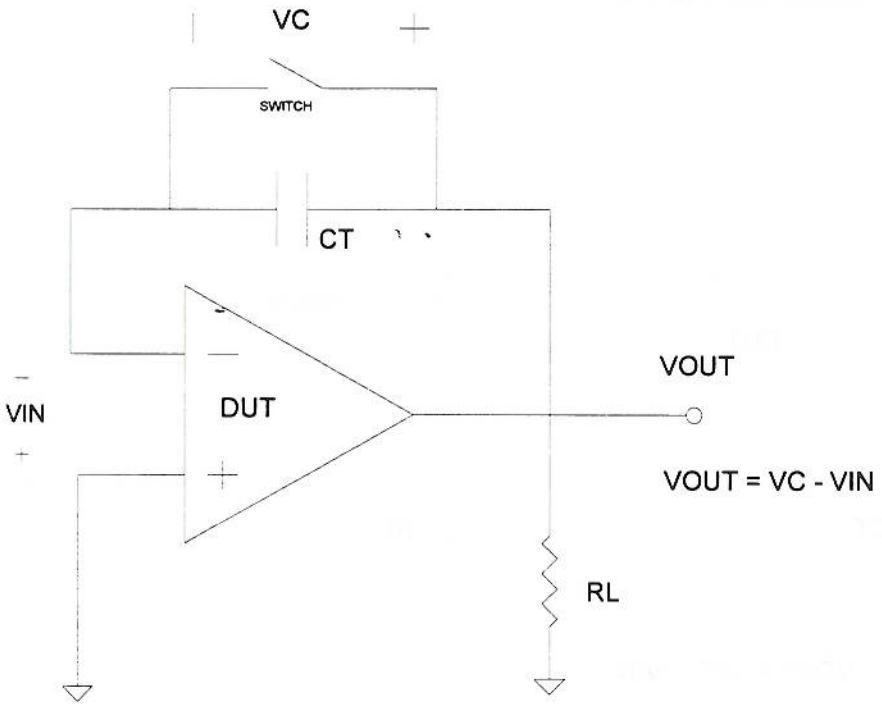
Test Method (I_B^+) (stopwatch integration):

- Select a proper value for C_T.
- Close switch and measure V_{OUT1}.
- Open switch and start timing simultaneously.
- Stop timing when V_{OUT} reaches V_{OUT2}.
- Calculate I_B^+:

$$I_B^+ = -C_T \frac{V_{OUT2} - V_{OUT1}}{\Delta t}$$

Note: The negative sign in this equation serves to yield the correct polarity of the input bias current. Also, the above equation assumes that the voltage across capacitor C_T increases linearly with time. Further, Δt should be large, possibly 60 seconds, in order to reduce reaction time error. The common-mode input voltage should be kept small in the case of parts that show a significant rise in input bias current with increasing common-mode voltage. C_T must be chosen in order to meet these conditions. For instance, an op amp with an input bias current of four picoamps, an integration time of 60 seconds and a ΔV_{OUT} of approximately 50 mV would require the value of C_T to be about 4,800 pF.

Test Circuit (I_B^-)



Test Method (I_B^-) (stopwatch integration)

- Determine I_B^- similarly to I_B^+ except for the final calculation:

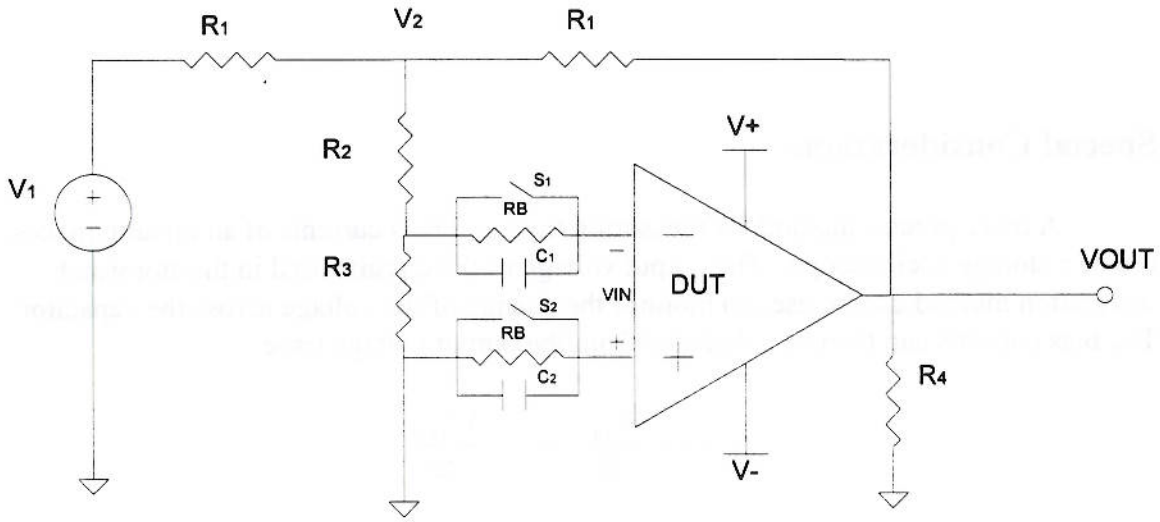
$$I_B^- = C_T \frac{V_{OUT2} - V_{OUT1}}{\Delta t}$$

Special Considerations:

A more precise method for measuring the input bias currents of an op amp makes use of a storage oscilloscope. The output voltage of the circuits used in the stopwatch integration method can be used to monitor the change of the voltage across the capacitor. The bias currents can then be calculated from the output voltage trace:

$$I_B = C_T \frac{\partial V_{OUT}}{\partial t} = C_T \frac{\Delta V_{OUT}}{\Delta t}$$

Test Circuit (I_B^+): (Large resistor method)



Test Conditions:

- Set the power supplies to the specified value.
- Adjust V_1 for $V_{OUT} = 0V$.
- Choose R_4 to establish the specified load: $R_{LOAD} \cong R_4 \| R_1$.
- T = 25 °C
- Choose R_B that results in a measurable change in V_2.
- Choose C_1 and C_2 to maintain stability. A suggested R-C time constant is 1 ms for the R_B and C combinations.

Test Method (I_B^+ and I_B^-)(Large resistor method)

- Close switches S_1 and S_2.
- Measure V_2:V_{2o}

- Open switch S_2.
- Measure V_2:V_{2+}
- Close switch S_2.

- Calculate I_B^+:

$$I_B^+ = \frac{V_{2o} - V_{2+}}{R_B\left(1 + \frac{R_2}{R_3}\right)}$$

- Open switch S_1.
- Measure V_2:V_{2-}
- Calculate I_B^-:

$$I_B^- = \frac{V_{2-} - V_{2o}}{R_B\left(1 + \frac{R_2}{R_3}\right)}$$

Special Considerations:

Parameter: Input Offset Current (I_{OS})

Definition: The difference between I_B^+ and I_B^-.

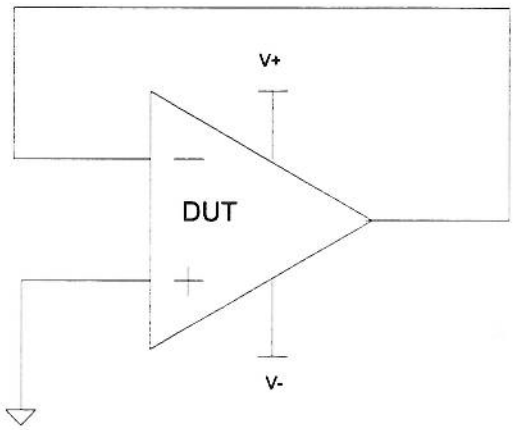
Calculation: I_{OS} is found by a simple calculation:

$$I_{OS} = I_B^+ - I_B^-$$

Parameter: Quiescent Current

Definition: The current delivered to the amplifier by one of the power supplies when the output current of the amplifier is zero.

Test Circuit:



Test Conditions:

- Set the power supplies to the specified value.
- T = 25 °C

Test Method:

The quiescent current flows into the V+ terminal and out of the V- terminal. In order to determine the quiescent current, only one measurement of the current in the V+ terminal or V- terminal is needed since they are equal.

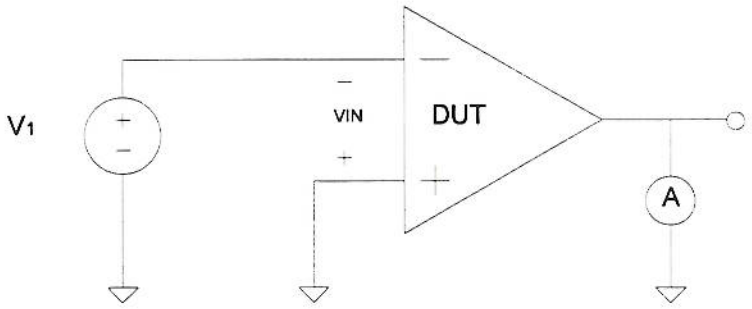
- Place an ammeter in series with the either the positive power supply or negative power supply to measure the quiescent current.

Special Considerations:

Parameter: Short Circuit Current

Definition: The output current of the amplifier when the output is shorted to ground.

Test Circuit:



Test Conditions:

- Set the power supplies to the specified value.
- T = 25 °C

Test Method:

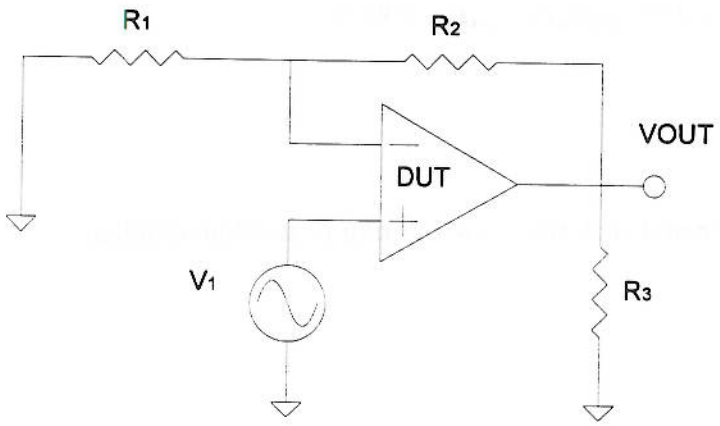
- Set V_1 to -500 mV.
- Measure the current flowing out of the output terminal of the amplifier with an ammeter as shown. This is the positive output current.
- Set V_1 to 500 mV.
- Measure the current flowing into the output terminal of the amplifier with an ammeter as shown. This is the negative output current.

Special Considerations:

Parameter: Gain-Bandwidth Product (GBW)

Definition: The product of the specified dc gain and the -3 dB frequency at the specified gain.

Test Circuit:



Test Conditions:

- Set the power supplies to the specified value.
- Choose R_3 to establish the specified load: $R_{LOAD} \cong R_2 || R_3$.
- T = 25 °C

Test Method:

- Choose R_1 and R_2 to establish desired gain:

$$DC\_GAIN = 1 + \frac{R_2}{R_1}.$$

Note: The dc gain of the test circuit should be 100 V/V when testing a unit where the gain bandwidth product specification does not include a specified gain.

- Use a function generator to set V_1.
- Sweep the frequency of V_1 and use an oscilloscope or Gain-Phase analyzer to determine the 3 dB frequency of the configuration.
- Calculate the Gain-Bandwidth Product:

$$GBW = DC\_GAIN \times -3dB\_FREQ$$

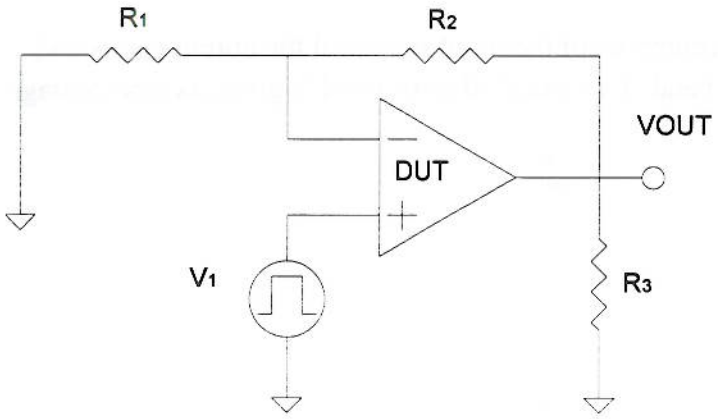
Special Considerations:

- The amplitude of V_1 must be selected such that slew limiting is avoided at higher frequencies.

Parameter: Slew Rate

Definition: The rate of change of the output for a large-signal input.

Test Circuit:



Test Conditions:

- Set the power supplies to the specified value.
- Choose R_3 to establish the specified load: $R_{LOAD} \cong R_2 \| R_3$.
- T = 25 °C

Test Method:

- Choose resistor values R_2 and R_3 to establish the specified gain or otherwise unity gain.
- Establish V_1 to be a square wave with a peak to peak amplitude as specified or typically ±5 V.
- Monitor V_{OUT} with an oscilloscope.
- Use the 10% and 90% points of the output wave form to calculate the slew rate:

$$SLEW\_RATE = \frac{\Delta V}{\Delta t}$$

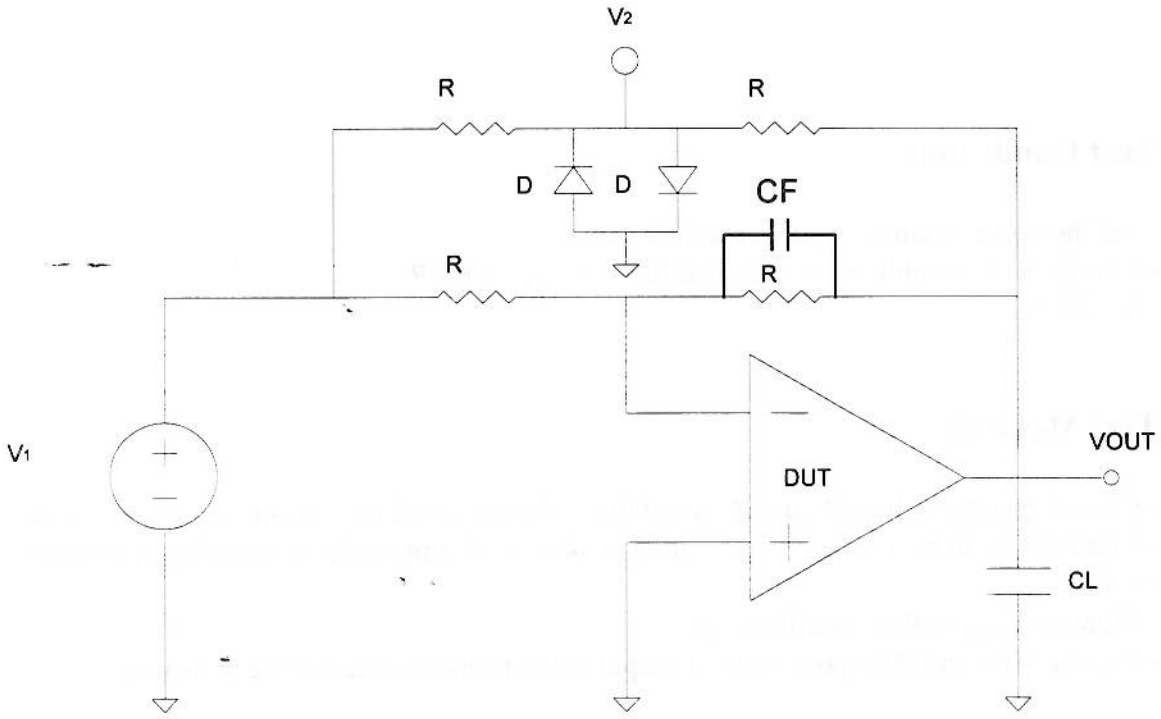
- Measure the slew rate for both positive and negative-going voltage transitions.
- Choose the lowest slew rate measurement, either the slew rate found on the positive transition or on the negative transition, to specify the slew rate of the op amp.

Special Considerations:

Parameter: Settling Time

Definition: The time from the occurrence of the input step until the output enters and remains within the specified error band. The specified error band is given as a percentage of the output voltage step.

Test Circuit:



About the Test Circuit:

- The voltage gain V_{OUT}/V_{IN} equals -1.
- V_2 equals $(V_{OUT}+V_{IN})/2$. This is a subtraction since V_{IN} is the negative of V_{OUT}.

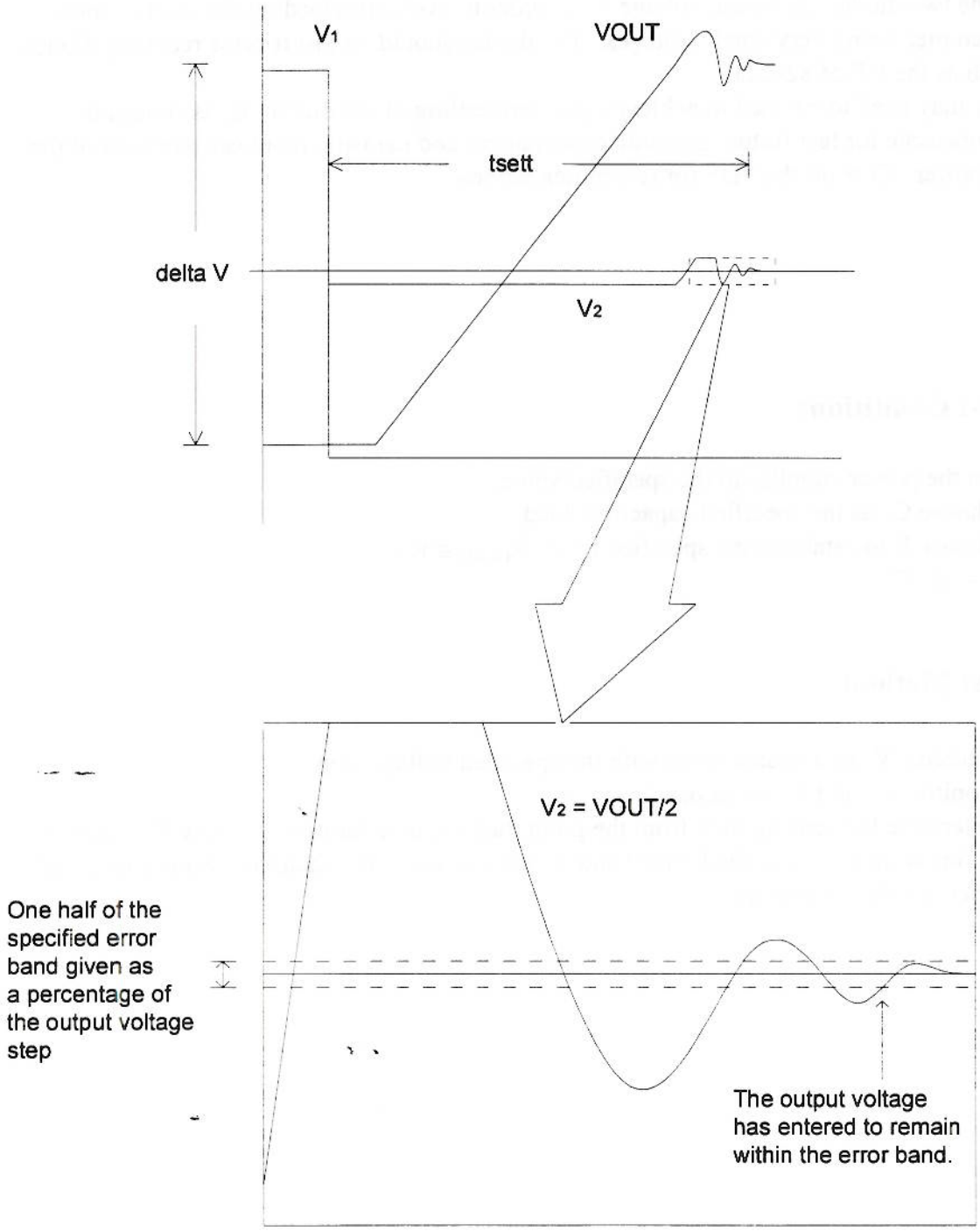
- The two diodes clamp the voltage V_2 in order to avoid overloading the oscilloscope when measuring very small voltages. The diodes should be fast reverse recovery diodes such as the HP-5082-2835.
- C_F may need to be used to achieve optimum settling of the output. C_F is chosen to compensate for test fixture parasitic capacitances and parasitic input capacitances of the amplifier. Consult the PDS for recommendations.

Test Conditions:

- Set the power supplies to the specified value.
- Choose C_L as the specified capacitive load.
- Choose R to establish the specified load: $R_{LOAD} \cong R/2$.
- T = 25 °C

Test Method:

- Establish V_1 as a square wave with the specified voltage step.
- Monitor V_{IN} and V_2 on an oscilloscope.
- Determine the settling time from the point that V_{IN} transitions to the time V_2 enters and remains within the specified error band divided by two. The factor of two is a result of V_2 being half of the output.

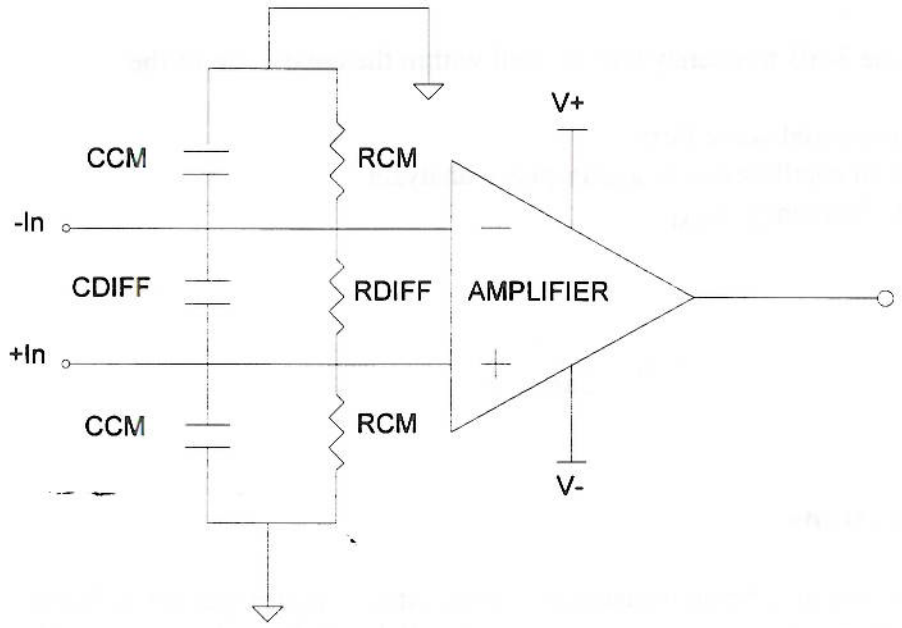


Special Considerations:

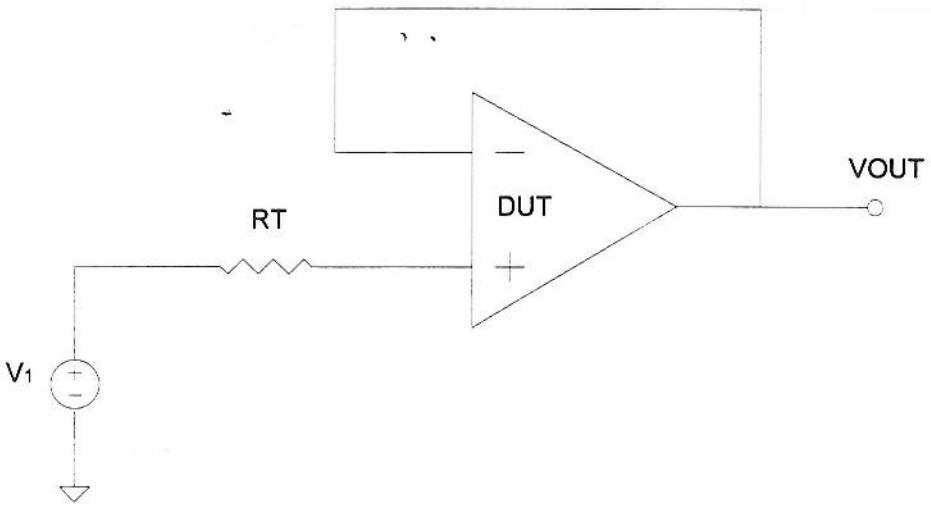
- V_2 must be measured with a very low capacitance probe. A 10 pF scope probe generally has too much capacitance to make this measurement.

Parameter: Common-Mode Input Capacitance (C_{CM})

Definition: The equivalent capacitance from an input terminal to ground. As shown in the circuit diagram below, common-mode input capacitance is one of several specified input impedances.



Test Circuit:



Test Conditions:

- Set the power supplies to the specified value.
- T = 25 °C

Test Method:

- Choose R_T so that the 3-dB frequency will be well within the bandwidth of the amplifier.
- Establish V_1 as a sinusoidal wave form.
- Monitor V_{OUT} with an oscilloscope or a gain-phase analyzer.
- Determine the 3-dB frequency, f_{CCM}.
- Calculate C_{CM}:

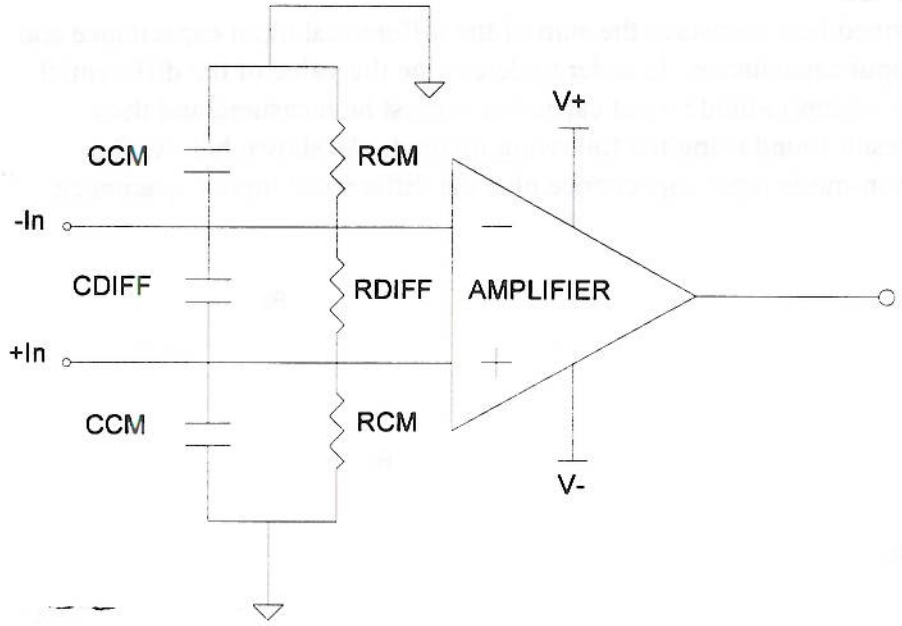
$$C_{CM} = \frac{1}{2\pi f_{CCM} R_T}$$

Special Considerations:

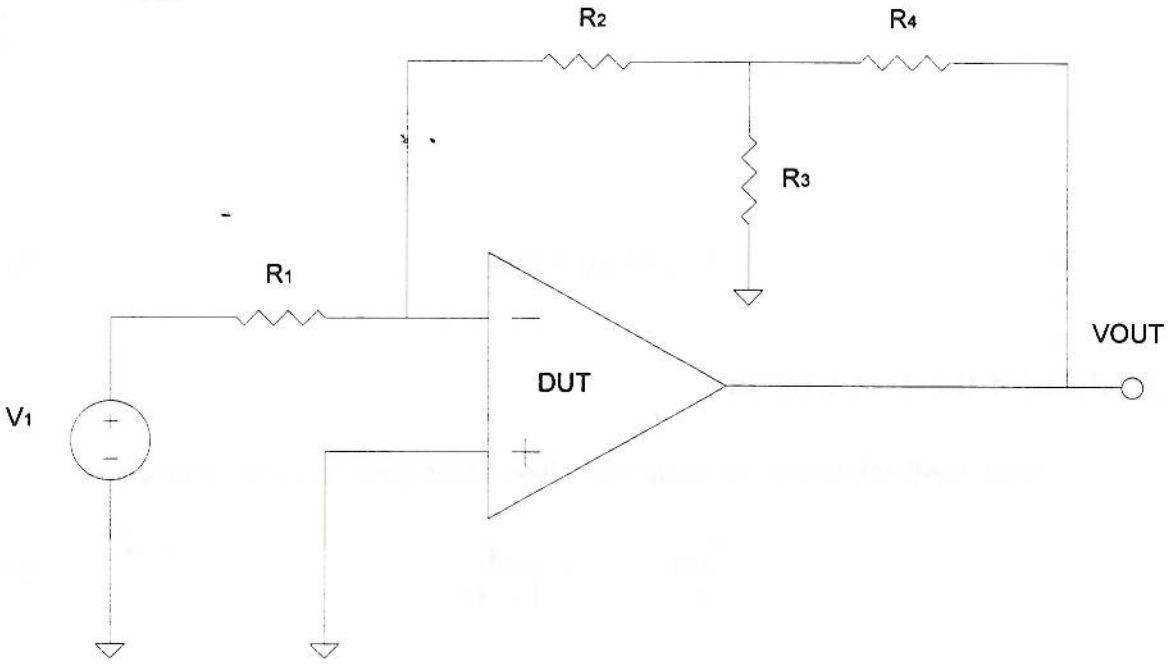
The capacitance that is being measured is comparable to typical parasitics found on bread boards or other test boards. Capacitance in parallel with R_T and C_{CM} will add with C_{CM} to establish the 3 dB frequency. Low capacitance boards should be used or else accounted for in the calculation. Similarly, the parasitic capacitance contributed by R_T should not be neglected. This parasitic introduces a zero at $f = \frac{1}{2\pi R_T C_{PARASITIC}}$.

Parameter: Differential Input Capacitance (C_{DIFF})

Definition: The equivalent capacitance between the input terminals of the operational amplifier. As shown in the circuit diagram below, differential input capacitance is one of several specified input impedances.



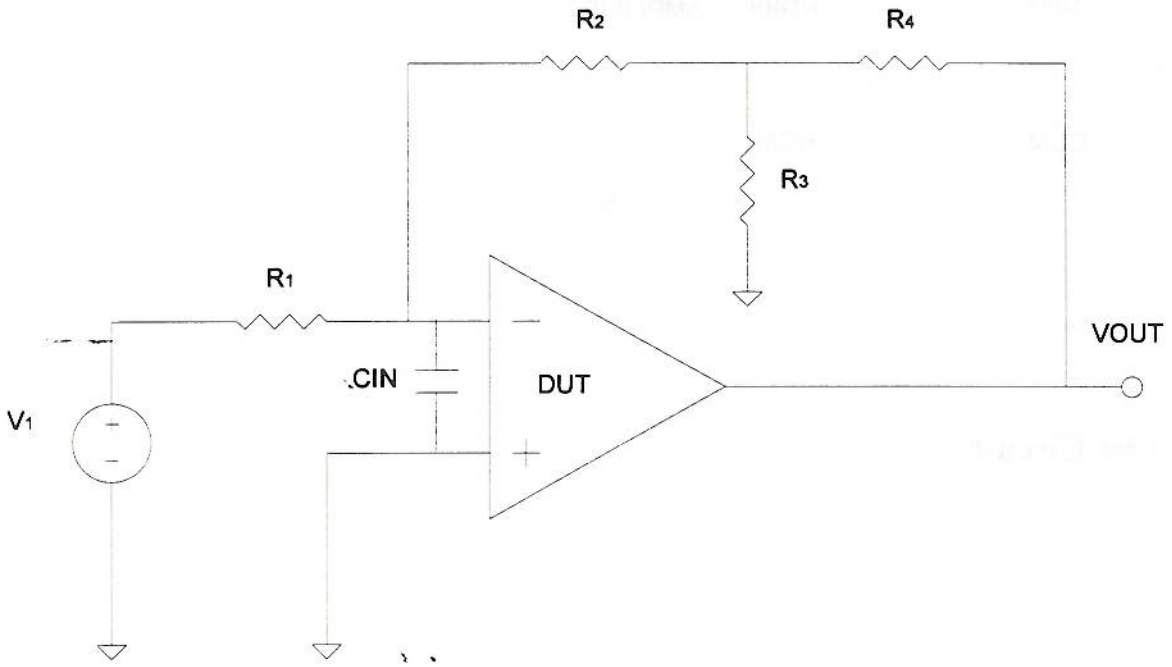
Test Circuit:



About the Test Circuit:

A high-gain, high-impedance op amp circuit configuration is required to observe the effect of the differential input capacitance on the transfer function, V_{OUT}/V_1. Resistor values can be chosen for the "T-Configuration" test circuit above to achieve both high gain and high impedances.

The test described here measures the sum of the differential input capacitance and the common-mode input capacitance. In order to determine the value of the differential input capacitance, the common-mode input capacitance must be measured and then subtracted from the result found using the following method. As shown below, C_{IN} represents one common-mode input capacitance plus the differential input capacitance.



$$C_{IN} = C_{CM} + C_{DIFF} \tag{1}$$

Analysis of the Test Circuit:

Classic feedback theory states that the closed-loop gain, V_{OUT}/V_1 is given by:

$$\frac{V_{OUT}}{V_1} = A_{CL} = \frac{A}{1 + A\beta} \tag{2}$$

where A_{CL} is the closed-loop gain, A is the open-loop gain and β is feedback factor. The closed-loop gain can be rewritten as

$$A_{CL} = \frac{1}{\beta} \cdot \frac{A\beta}{1 + A\beta}. \tag{3}$$

Aβ is termed the "loop gain" of the feedback configuration. The term, 1/β, is the gain of the circuit in the case that the open-loop gain is infinity. This is the value that is calculated when analyzing an ideal op amp circuit. One consequence of the ideal op amp assumptions is that any impedances between the terminals of the amplifier are ignored since it is assumed that both terminals are at the same potential and there is no current flow between them. As a result, the impedance that is to be measured in this case, C_{IN}, will only appear in the loop gain terms.

For this test circuit,

$$\frac{1}{\beta} = -\left(\frac{R_2 + R_4}{R_1}\right)\left(1 + \frac{R_2 || R_4}{R_3}\right). \tag{4}$$

For the typical case where R_3 is relatively small compared to R_2 and R_4,

$$\frac{R_2 || R_4}{R_3} >> 1 \tag{5}$$

and

$$\frac{1}{\beta} \cong \frac{R_2 R_4}{R_1 R_3}. \tag{6}$$

The loop gain, Aβ, is given by:

$$A\beta = \frac{R_3 || (R_2 + R_1)}{R_3 || (R_2 + R_1) + R_4} \cdot \frac{R_1}{R_1 + R_2} \cdot \frac{A_{OL}}{1 + s/2\pi f_b} \cdot \frac{1}{1 + s(R_1 || (R_2 + R_3 || R_4))C_{IN}} \tag{7}$$

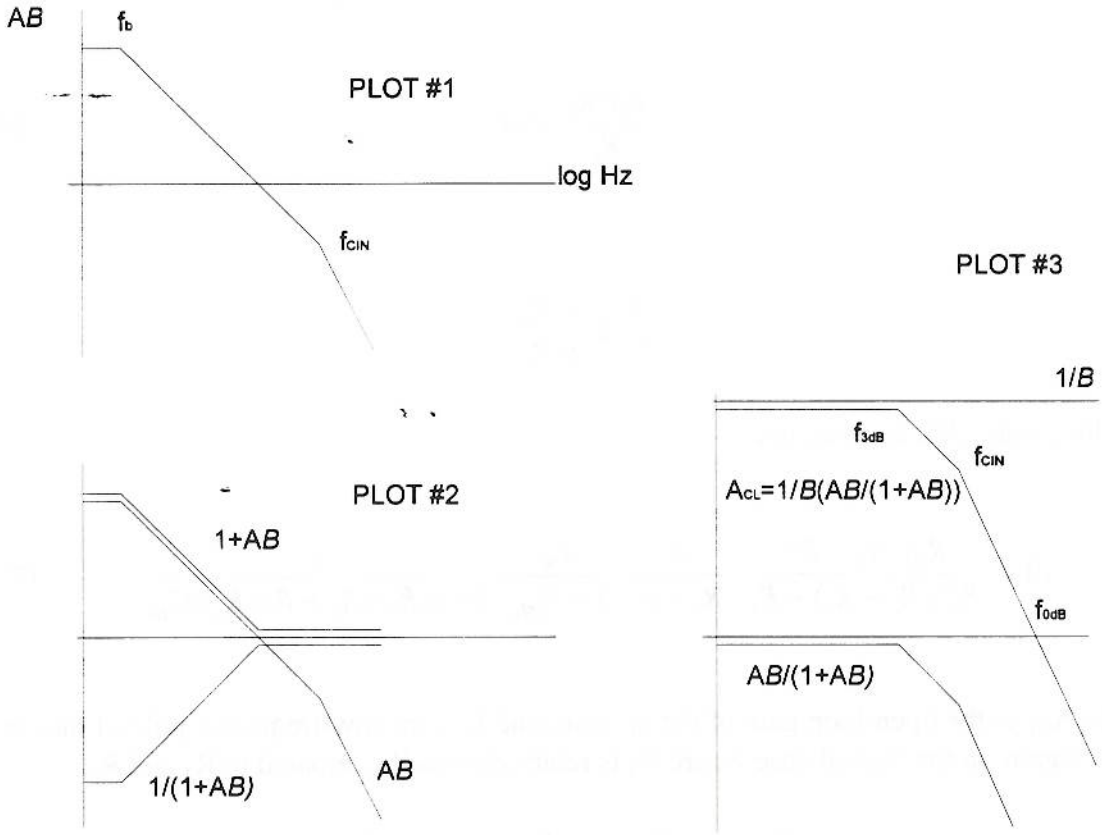
where A_{OL} is the open-loop gain of the op amp, and f_b is the low-frequency pole of the op amp. Again, in the typical case where R_3 is relatively small compared to R_2 and R_4,

$$A\beta \cong \frac{R_3}{R_3 + R_4} \cdot \frac{R_1}{R_1 + R_2} \cdot \frac{A_{OL}}{1 + s/2\pi f_b} \cdot \frac{1}{1 + s(R_1 || R_2)C_{IN}} \tag{8}$$

Two poles appear in the loop gain expression; one is contributed by the op amp and is located at f_b and the other is a result of C_{IN} and it is located at f_{CIN} where f_{CIN} is given by:

$$f_{CIN} = \frac{1}{2\pi(R_1||(R_2 + R_3||R_4))C_{IN}}. \tag{9}$$

A graphical technique can be used to determine Aβ/(1+Aβ). The loop gain is shown in plot #1. Frequency f_{CIN} must occur after the loop gain crosses 0 dB so that it appears in the complete closed-loop gain of the circuit. Plot #2 demonstrates the graphical technique of determining Aβ/(1+Aβ). First, Aβ is redrawn. Next, 1+Aβ is shown to follow Aβ until 0 dB where it levels off and remains at 0 dB for high frequencies. 1/(1+Aβ) is the same shape as 1+Aβ, only it is mirrored about 0 dB. Finally, since the plots are on the log scale, Aβ/(1+Aβ) is found graphically by subtracting the 1/(1+Aβ) function from the Aβ function. The result is shown in plot #3 as Aβ/(1+Aβ). To determine the overall closed-loop response of the test circuit, 1/β is multiplied with Aβ/(1+Aβ). This closed-loop gain function of the test circuit is indeed what can be observed on a gain-phase analyzer.



It remains to determine f_{CIN} from the closed-loop response function. An approximation using the ratios of gains and frequencies can be used to find f_{CIN}. In the case where the frequencies of interest are widely separated, the following approximation is sufficient for determining f_{CIN}:

$$f_{CIN} = \frac{(f_{odB})^2}{f_{3dB} A_{CL\_DC}} \tag{10}$$

where f_{0dB} is the frequency at which the closed-loop gain of the amplifier reaches 0 dB, f_{3dB} is the 3 dB frequency of the circuit configuration and A_{CL_DC} is the dc closed-loop gain of the circuit. Once f_{CIN} has been determined, a simple back calculation for C_{IN} can be performed since the resistor values of the circuit are known:

$$C_{IN} = \frac{1}{2\pi f_{CIN}\left(R_1 || \left(R_2 + R_3 || R_4\right)\right)}. \tag{11}$$

Test Conditions:

- Set the power supplies to the specified value.
- T = 25 °C

Test Method:

Key to implementing this test circuit for measuring input capacitance is a proper choice of resistor values: R_1, R_2, R_3 and R_4. These resistor values must be chosen such that f_{CIN} is significantly greater than f_{3dB} and significantly less than f_{0dB}. For this to be true, the dc gain of the circuit must be high, about 1000 V/V, and the impedance seen by C_{IN} must be significantly large, on the order of 50 kΩ to 500kΩ. A typical choice of resistor values might be:

$R_1 = 500\ k\Omega$
$R_2 = 1\ M\Omega$
$R_3 = 2\ k\Omega$
and $R_4 = 1M\Omega$.

The parasitic capacitance associated with R_1 introduces a zero at high frequencies. If this zero affects the placement of f_{0dB}, an erroneous C_{IN} measurement will be made. The value of R_1 should not be greater than 500 kΩ in order to avoid this situation.

With the resistor values shown above, $1/\beta$, which is approximately the dc gain of the circuit , is 1004 V/V. The resistance seen by C_{IN}, given in equation 11, is 334 kΩ. This would place f_{CIN} at 119 kHz for an op amp with $C_{DIFF} + C_{CM} = 4$ pF such as the OPA131.

Once resistor values have been chosen, the circuit transfer function can be determined by the use of a gain-phase analyzer. A small input voltage must be used to avoid slew limiting. An input voltage level of 500 μV to 1 mV is typical. Values from the transfer function are used directly in equations 10 and 11 to calculate C_{IN}.

Since equation 10 is an approximation that is valid for widely separated pole and zero frequencies, the resistor values R_1, R_2, R_3 and R_4 must be chosen in order to place f_{CIN} at a frequency where the approximation is satisfactory. The accuracy of the measurement can easily be verified by artificially placing a small known capacitance across the inputs of the op amp. A 1 pF capacitor works well. With the extra capacitance in place, the test procedure can be repeated to observe how well the extra 1 pF is resolved. If f_{CIN} is not significantly greater than f_{3dB}, an increase of less than 1 pF will be observed and it can be concluded that the original C_{IN} measurement was lower than the actual value of C_{IN}. In this case, an appropriate adjustment of R_1 and R_3 to increase f_{CIN} and maintain a gain of 1000 V/V should be made. On the other hand, if an increase of greater than 1 pF is observed, f_{CIN} should be decreased by choosing new values for R_1 and R_2 while maintaining a gain of 1000 V/V. The test procedure can be repeated until the added capacitance is resolved with an acceptable amount of error. Finally, once C_{IN} has been determined, equation 1 can be used to calculate the differential input capacitance of the amplifier.

COOKBOOK TEST PROCEDURE:

- Measure resistors R_1, R_2, R_3 and R_4.
- Measure the dc gain of the circuit: A_{CL_DC}.
- Measure f_{3dB}.
- Measure f_{0dB}.
- Calculate C_{IN} using equations 10 and 11.
- Measure a 1 pF capacitor.
- Add the 1 pF capacitor across the input terminals of the op amp.
- Measure the dc gain of the circuit: A_{CL_DC}.
- Measure f_{3dB}.
- Measure f_{0dB}.
- Calculate C_{IN} using equations 10 and 11.
- Make appropriate adjustments to R_1 and R_3 and repeat this procedure until the additional 1 pF capacitor is resolved with an acceptable error.
- Calculate C_{DIFF} using equation 1.

Special Considerations:

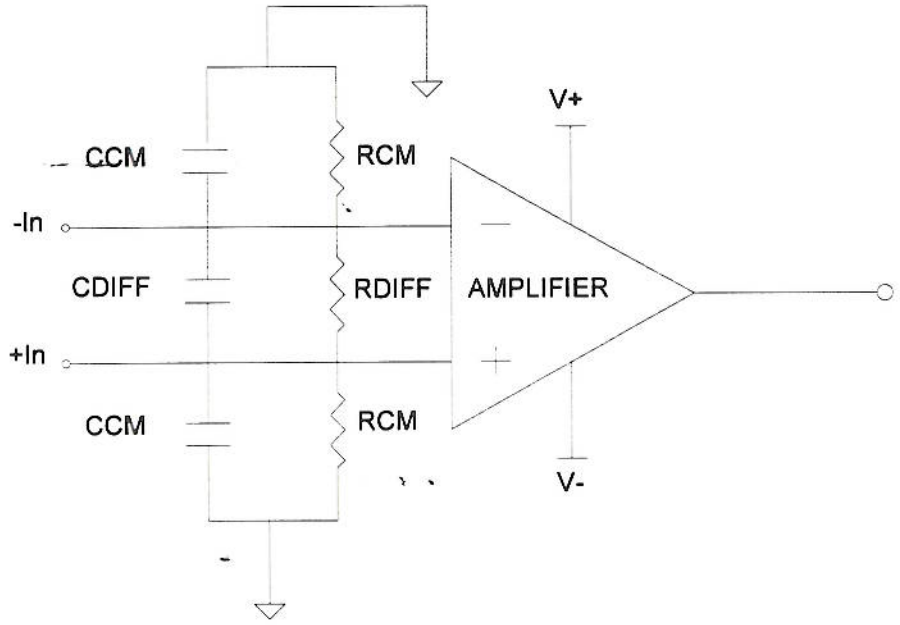
The capacitance that is being measured is comparable to typical parasitics found on bread boards or other test boards. Perf board without metal traces or possibly air-wiring should be used to build the test circuit.

Only those units that show a two-pole response in the closed-loop gain can be measured using the technique described above. For example, the OPA627 exhibits the two-pole response, however, the OPA27 does not.

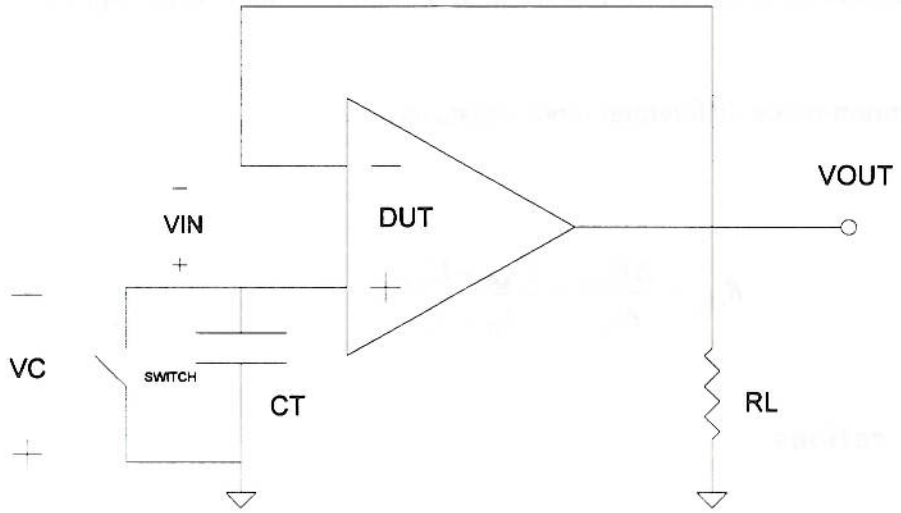
Parameter: Common-Mode Input Resistance (R_{CM})

Definition: The equivalent resistance from an input terminal to ground. As shown in the circuit diagram below, common-mode input resistance is one of several specified input impedances. Mathematically, R_{CM} is defined as the incremental change in common-mode voltage with an incremental change in bias current:

$$R_{CM} = \frac{\Delta V_{CM}}{\Delta I_B}.$$



Test Circuit:



Test Conditions:

- Set the power supplies to the specified value.
- T = 25 °C

Test Method:

The common-mode input resistance is measured by calculating $\Delta V_{CM}/\Delta I_B$. The test circuit used for finding I_B is a convenient way to measure both a change in common-mode voltage and a change in input bias current. The bias current can be calculated at two common-mode voltage levels. Using the integration method, however, a calculation of I_B must be made while allowing the common-mode voltage to vary a small amount.

- Measure I_B at a given common-mode voltage: V_{CM1},I_{B1}.

For example, measure I_{B1} at a common-mode voltage of -100 mV by measuring the integration time needed for the output to decrease from -50 mV to -100 mV. Use the equations given in the Test Method section of input bias current for calculating I_{B+}.

- Measure I_B at a second common-mode voltage: V_{CM2},I_{B2}.

Continuing with the example, measure I_{B2} at a common-mode voltage of -500 mV by measuring the integration time needed for the output to decrease from -450 mV to -500 mV. Use the equations given in the Test Method section of input bias current for calculating I_{B+}.

- Calculate the common-mode differential input resistance:

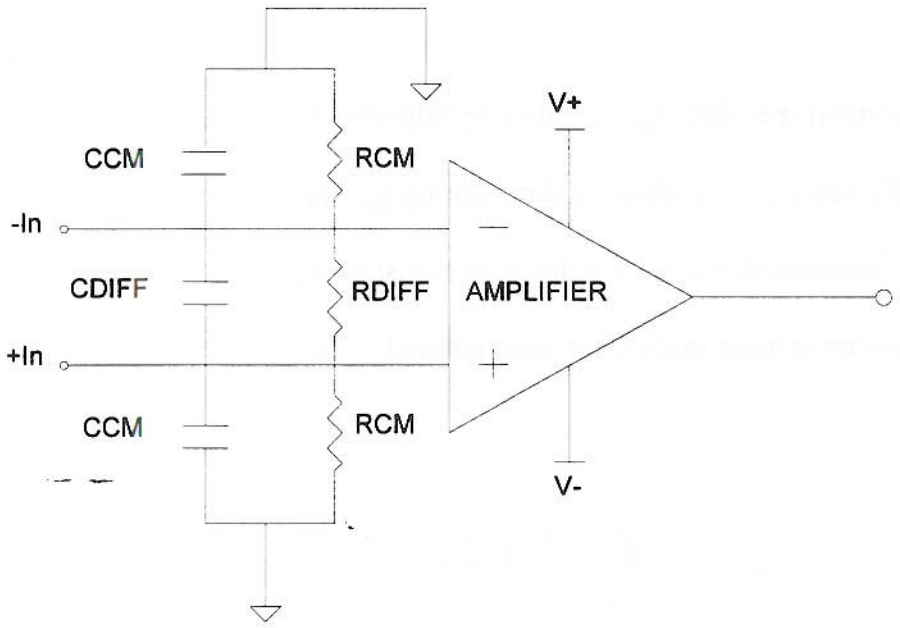
$$R_{CM} = \frac{\Delta V_{CM}}{\Delta I_B} = \frac{V_{CM1} - V_{CM2}}{I_{B1} - I_{B2}}.$$

Special Considerations:

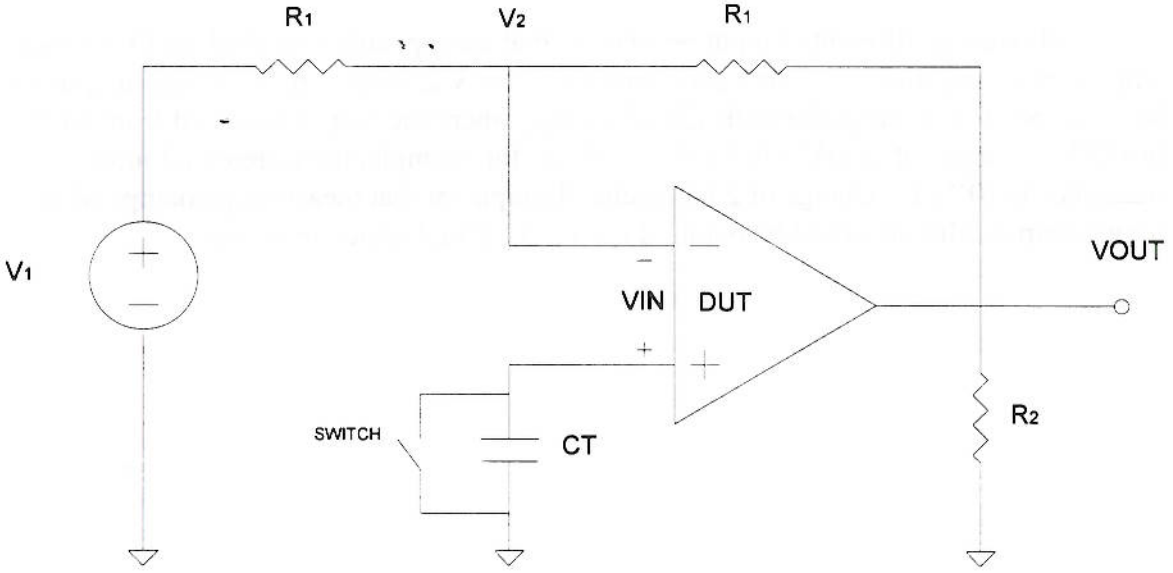
Parameter: Differential Input Resistance (R_{DIFF})

Definition: The equivalent resistance between the input terminals of the operational amplifier. As shown in the circuit diagram below, differential input resistance is one of several specified input impedances. Mathematically, R_{DIFF} is defined as the incremental change in differential input voltage with an incremental change in bias current:

$$R_{DIFF} = \frac{\Delta V_{IN}}{\Delta I_B}.$$



Test Circuit:



Test Conditions:

- Set the power supplies to the specified value.
- Choose R_2 to establish the specified load: $R_{LOAD} \cong R_2 \| R_1$.
- T = 25 °C

Test Method:

- Set V_{OUT} to the maximum specified A_{OL} condition by adjusting V_1.
- Measure V_{IN}: V_{IN1}.
- Measure I_{B+} using the integration method for determining I_{B+}: I_{B1}.

- Set V_{OUT} to the minimum specified A_{OL} condition by adjusting V_1.
- Measure V_{IN}: V_{IN2}.
- Measure I_{B+} using the integration method for determining I_{B+}: I_{B2}.

- Calculate R_{DIFF}:

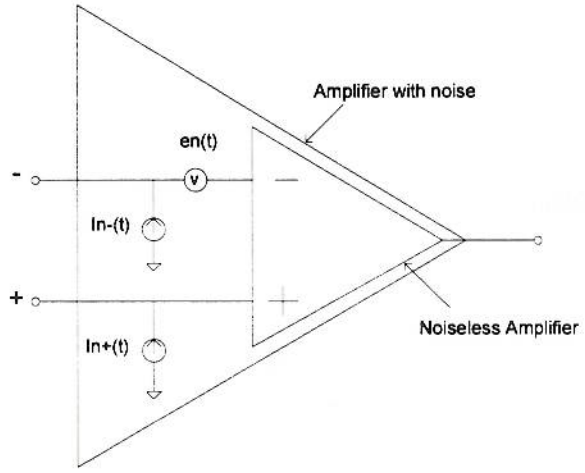
$$R_{DIFF} = \frac{\Delta V_{IN}}{\Delta I_B} = \frac{V_{IN1} - V_{IN2}}{I_{B1} - I_{B2}}.$$

Special Considerations:

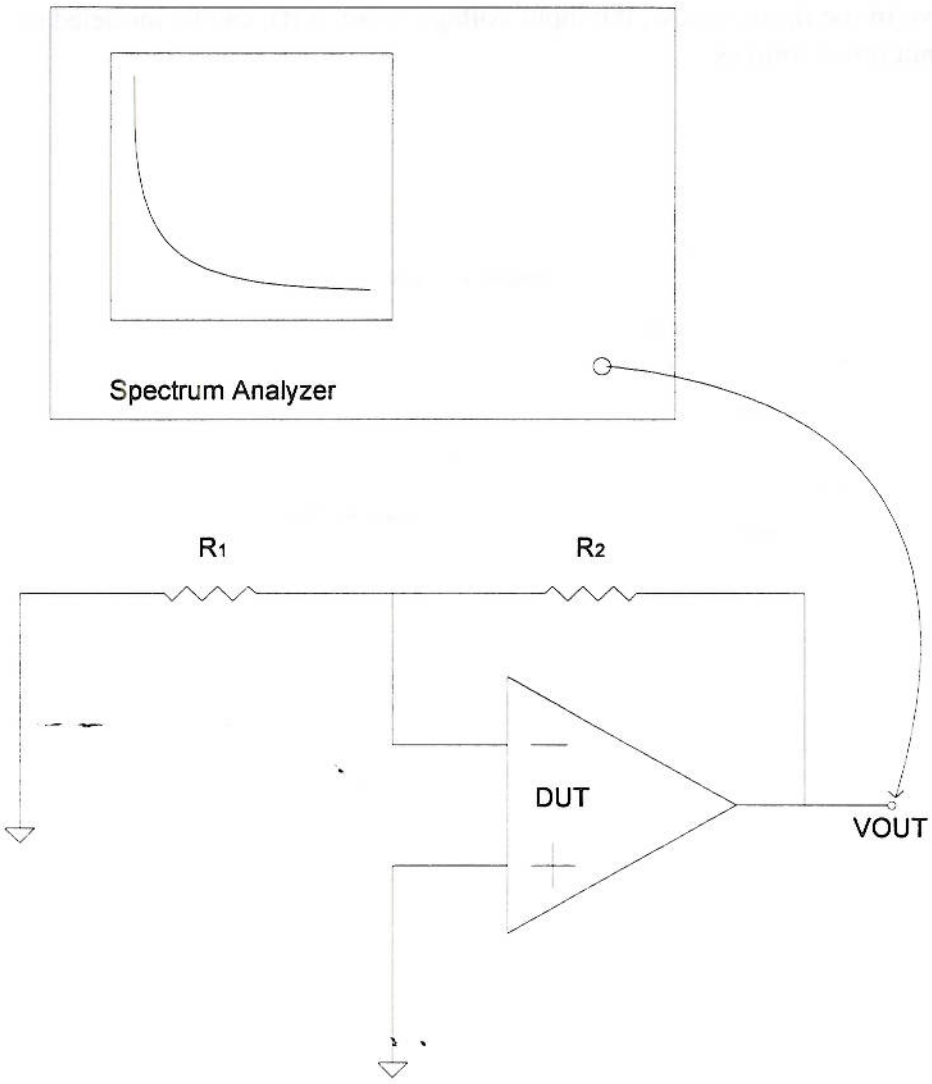
Measuring differential input resistances that are typically specified for FET-input amplifiers is very difficult. For a given change in the V_{IN}, a very small change in I_B must be resolved. For an amplifier with 120 dB of A_{OL} where the output is moved from 10 V to -10 V, a change of 20 μV will be observed. If, for example, the differential input resistance is 10^{10} Ω, a change of 2 fA results. Equipment that measures picoamps with femptoamp resolution would be required for a typical FET-input amplifier.

Parameter: Input Voltage Noise Density

Definition: The input voltage noise is the time varying component of the input offset voltage. As shown in the figure below, the input voltage noise, $e_n(t)$, can be modeled as one of several input noise sources.

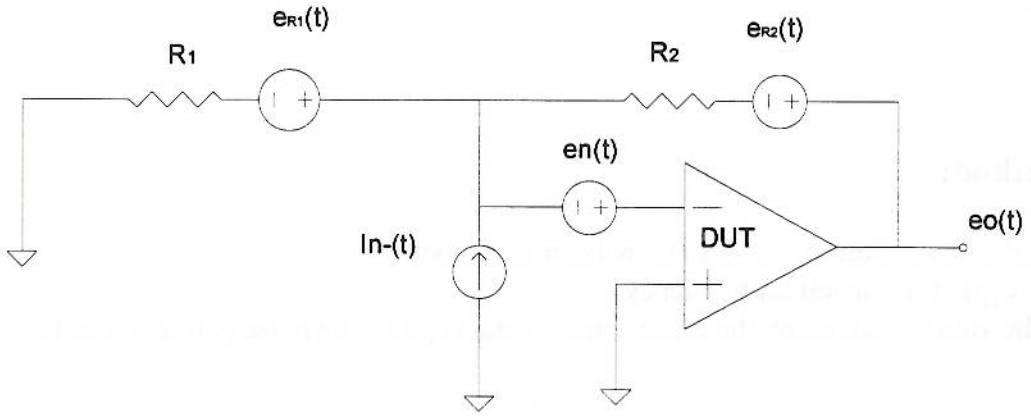


Test Circuit:



About the Test Circuit:

The test circuit including relevant noise sources is shown below.



$$e_0(t) = e_n(t)\left(1 + \frac{R_2}{R_1}\right) + I_{n-}(t)(R_2) + e_{R1}(t)\left(\frac{R_2}{R_1}\right) + e_{R2}(t)$$

The objective in selecting resistors R_1 and R_2 is to minimize the relative input-referred contribution of the noise sources that are not being measured. In this case, they are $I_{n-}(t)$, $e_{R1}(t)$ and $e_{R2}(t)$. The contribution of $I_{n-}(t)$ can be minimized by selecting a small value of R_1. The contribution of $e_{R2}(t)$ can be reduced by placing the amplifier in a high gain. Since $e_n(t)$ and $e_{R1}(t)$ are gained up by approximately the same amount for high gains, resistor R_1 must be selected such that the noise contribution from R_1 is at least four times less than the predicted value of $e_n(t)$, the value to be measured. $e_{R1}(t)$ is given by:

$$e_{R1}(t) = \sqrt{4kTR_1}\ .$$

For

$$e_n(t) \geq 4e_{R1}(t),$$

resistor R_1 is given by:

$$R_1 \leq \frac{(e_n(t))^2}{64kT}$$

Test Conditions:

- Set the power supplies to the specified value.
- Select R_1 and R_2 per the discussion given above.
- T = 25 °C

Test Method:

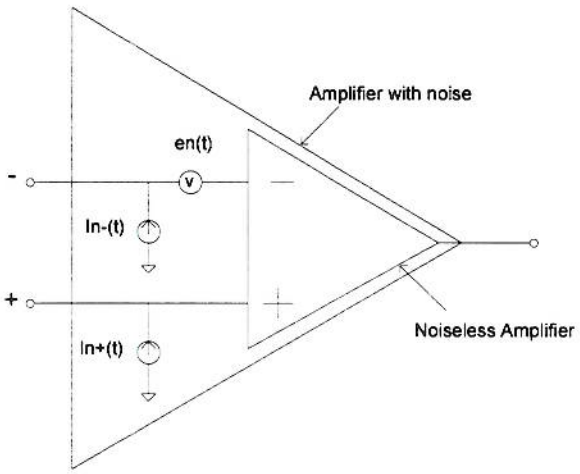
- Connect the test circuit to a spectrum analyzer as shown.
- Measure $e_o(t)$ at the specified frequency.
- Divide the value obtained by the noise gain to obtain $e_n(t)$. The noise gain is given by:

$$Noise\_gain = \left(1 + \frac{R_2}{R_1}\right).$$

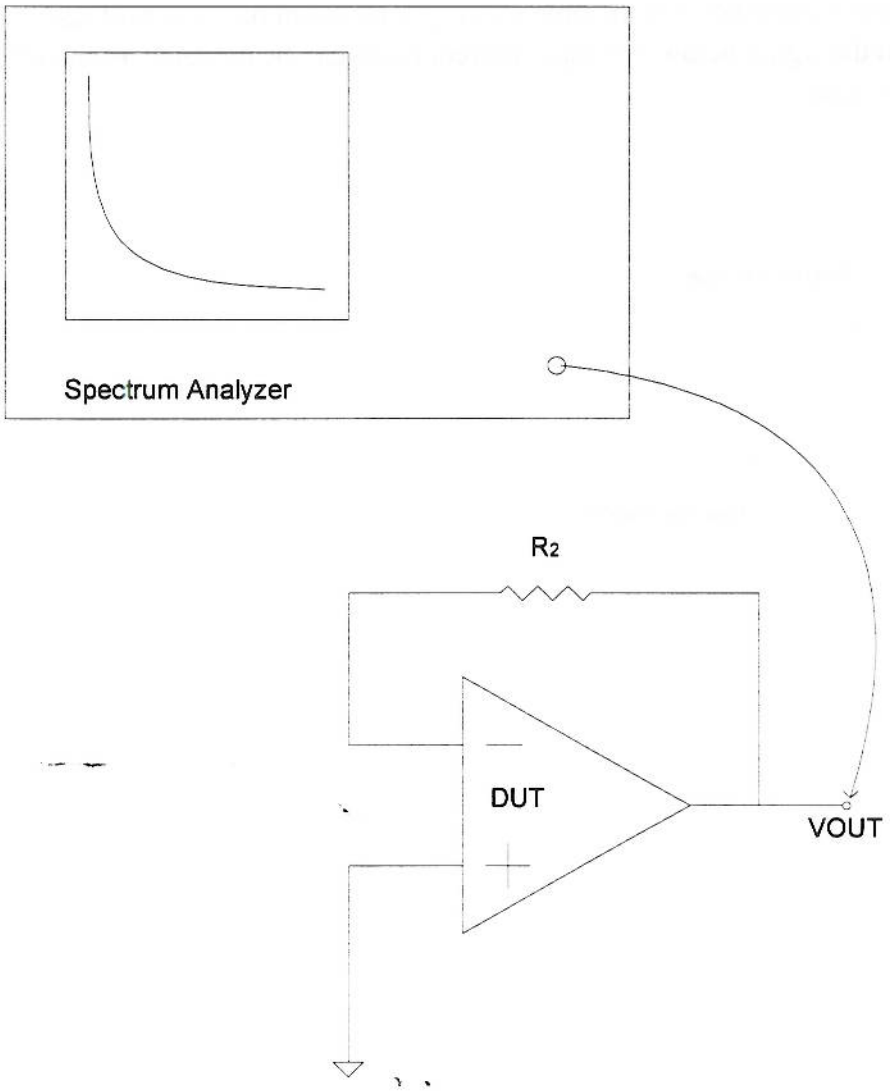
Special Considerations:

Parameter: Input Current Noise Density

Definition: The input current noise is the time varying component of the input bias current. As shown in the figure below, the input current noise can be modeled as one of several input noise sources.

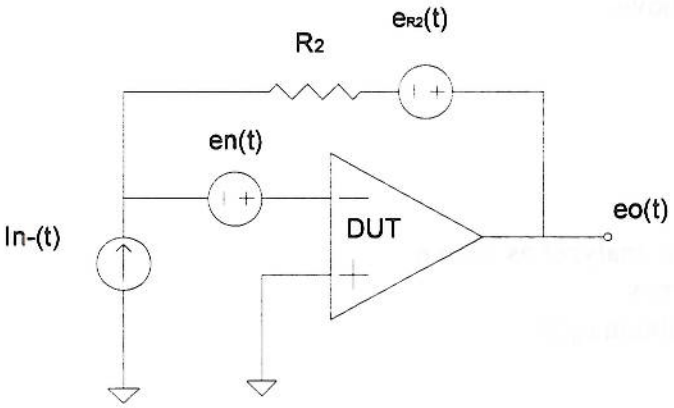


Test Circuit:



About the Test Circuit:

The test circuit including relevant noise sources is shown below.



$$e_0(t) = e_n(t) + I_{n-}(t)(R_2) + e_{R2}(t)$$

The objective in selecting resistor R_2 is to minimize the relative input-referred contribution of the noise sources that are not being measured. In this case, they are $e_n(t)$ and $e_{R2}(t)$. The contribution of $I_{n-}(t)$ can be made much larger than that of $e_n(t)$ by selecting a large value of R_2. R_2 should be selected so that the contribution of $e_{R2}(t)$ to the output voltage is at least four times less than $I_{n-}(t)(R_2)$. This $I_{n-}(t)(R_2)$ contribution is given by:

$$I_{n-}(t)(R_2) \approx \sqrt{2qI_{B-}}(R_2).$$

For

$$I_{n-}(t)(R_2) \geq 4e_{R2}(t),$$

R_2 must be given by:

$$R_2 \geq \frac{4kT}{qI_{B-}}.$$

Test Conditions:

- Set the power supplies to the specified value.
- Select R_2 per the discussion given above.
- T = 25 °C

Test Method:

- Connect the test circuit to a spectrum analyzer as shown.
- Measure $e_o(t)$ at the specified frequency.
- Divide the value obtained by R_2 to obtain $e_n(t)$.

Special Considerations:

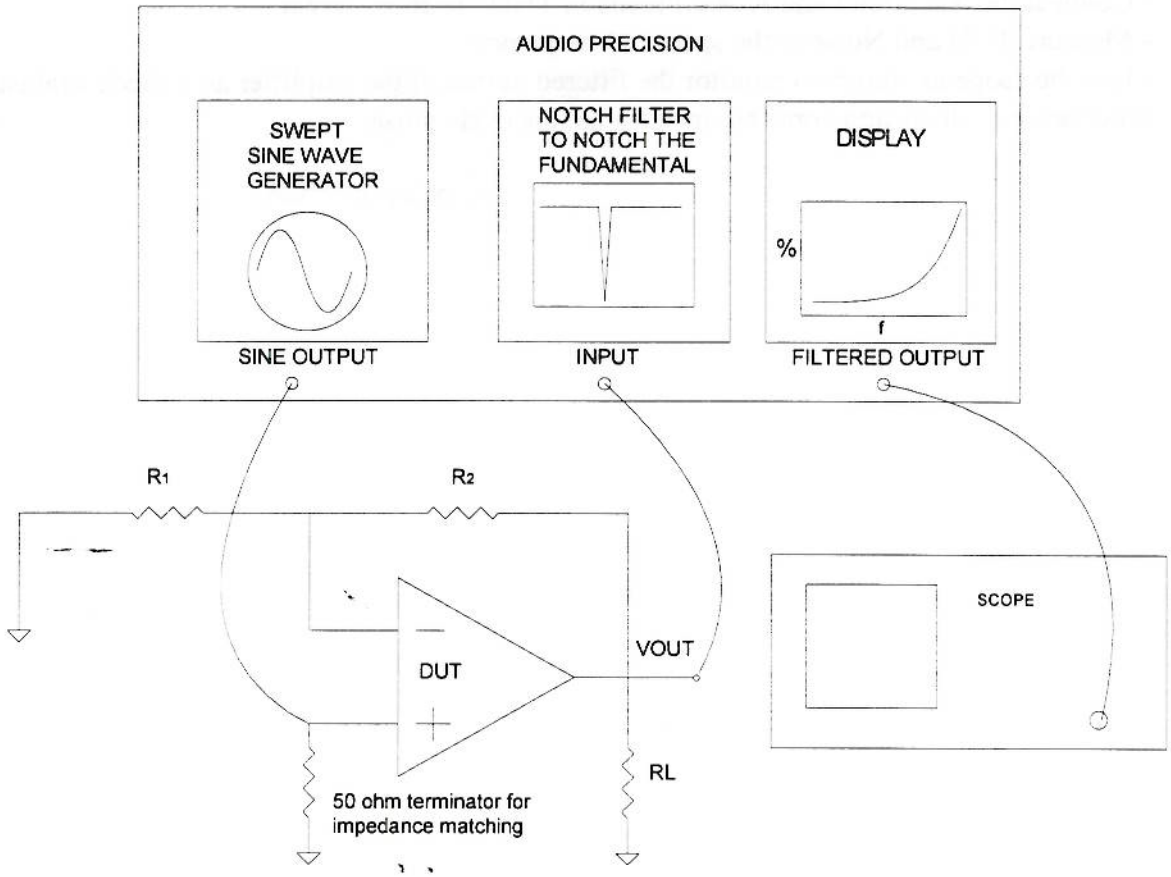
A typical bipolar-input amplifier with 5 nA of input bias current would require R_2 to be greater or equal to 20 MΩ. On the other hand, a typical FET-input amplifier with 5 pA of input bias current would require R_2 to be greater than or equal to 20×10^9 Ω.

add high noise gain test method

Parameter: Total Harmonic Distortion Plus Noise (THD + Noise)

Definition: The ratio of the rms value of the harmonic components of the output and the rms value of the noise at the output to the rms value of the fundamental component of the output.

Test Circuit:



Test Conditions:

- Set the power supplies to the specified value.
- Choose R_L to establish the specified load: $R_{LOAD}=R_L||(R_2+R_1)$
- T = 25 °C

Test Method:

- Choose R_1 and R_2 to establish the specified gain.

$$GAIN = 1 + \frac{R_2}{R_1}$$

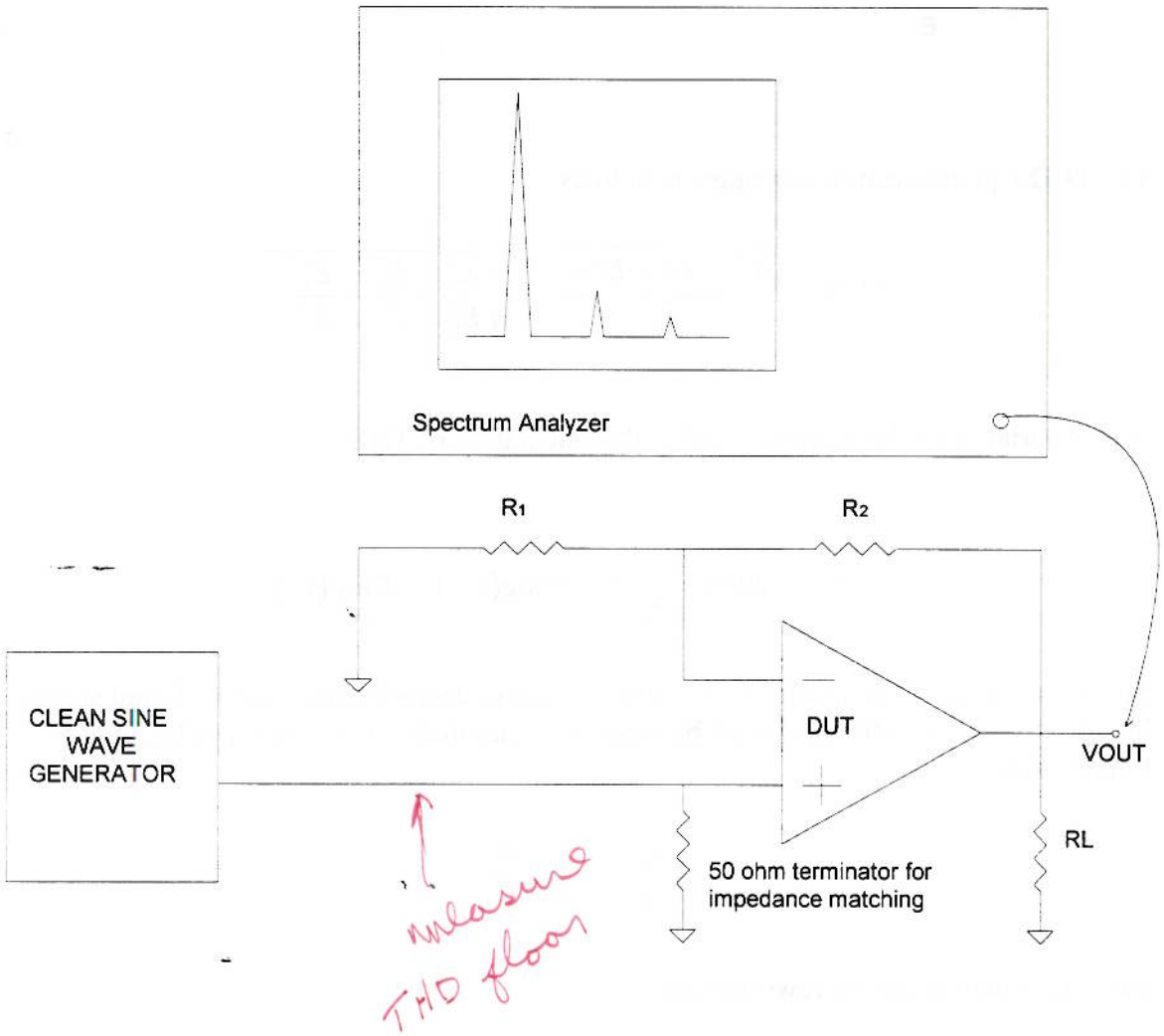
- Connect the test circuit and Audio Precision THD meter as shown.
- Measure THD and Noise at the specified frequency.
- Use the scope as shown to monitor the filtered output of the amplifier as a check against other noise or distortion contributors such as line cycle noise.

crossover

Higher Frequency Measurements

To make THD measurements at frequencies beyond the range of the Audio Precision THD meter, the following method can be used to measure THD with a spectrum analyzer.

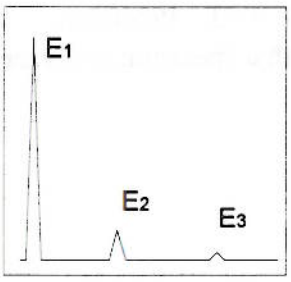
Test Circuit:



Test Method:

- Connect the test circuit and spectrum analyzer as shown.
- Set the function generator to output a sine wave at the specified frequency.

- The output of the spectrum analyzer will show a peak at the fundamental frequency and smaller peaks at the harmonic frequencies:



The THD equation can be rewritten as follows:

$$THD = \frac{\sqrt{E_2^2 + E_3^2 + E_4^2 + \ldots}}{E_1} = \sqrt{\frac{E_2^2}{E_1^2} + \frac{E_3^2}{E_1^2} + \frac{E_4^2}{E_1^2} \ldots}$$

A new variable can be defined to aid in the calculation of THD:

$$dBc_X = 20\log\left(\frac{E_X}{E_1}\right) = 20\log(E_X) - 20\log(E_1)$$

Since the output of the spectrum analyzer is given in decibels, dBc_X can be found simply by calculating the difference in dB between the magnitudes of the peaks of E_X and E_1. Finally, since

$$\left(\frac{E_X}{E_1}\right)^2 = 10^{\frac{dBc_X}{10}},$$

the THD equation can be rewritten as:

$$THD = \left(\sqrt{10^{\frac{dBc_2}{10}} + 10^{\frac{dBc_3}{10}} + 10^{\frac{dBc_4}{10}} + \ldots}\right)(100)\%$$

Once all of the dBc_X values have been found using the spectrum analyzer, THD can be calculated.

Special Considerations:

APPENDIX A: Differential input voltage.

V_{OS} is one of several components that comprise the differential input voltage of an op amp. V_{IN} can be written as the sum of the contributions due to the initial V_{OS}, the temperature-dependent drift component of V_{OS}, input voltage required due to finite open loop gain (A_{OL}), errors due to finite common-mode rejection (CMR) and power supply rejection (PSR):

$$V_{IN} = V_{OS} + \frac{\partial V_{OS}}{\partial T}(\Delta T) + \frac{V_{OUT}}{A_{OL}} + CMRR \times V_{CM} + PSRR^{+} \times \Delta(V+) + PSRR^{-} \times \Delta(V-).$$

V_{OUT} - the output voltage of the amplifier.
A_{OL} - the open-loop gain of the amplifier.
T - the temperature of the amplifier.
ΔT - the difference between the temperature of the amplifier and 25 °C: (T - 25 °C).
CMRR - the common-mode rejection ratio which in this case has units of V/V.
V_{CM} - the voltage common to both inputs of the amplifier.
$PSRR^{+}$ - the positive power supply rejection ratio which in this case has units of V/V.
$\Delta(V+)$ - the difference between the positive power supply voltage and the specified power supply voltage: $((V+) - (V+)_{SPECIFIED})$.
$PSRR^{-}$ - the negative power supply rejection ratio which in this case has units of V/V.
$\Delta(V-)$ - the difference between the negative power supply voltage and the specified power supply voltage: $((V-) - (V-)_{SPECIFIED})$.

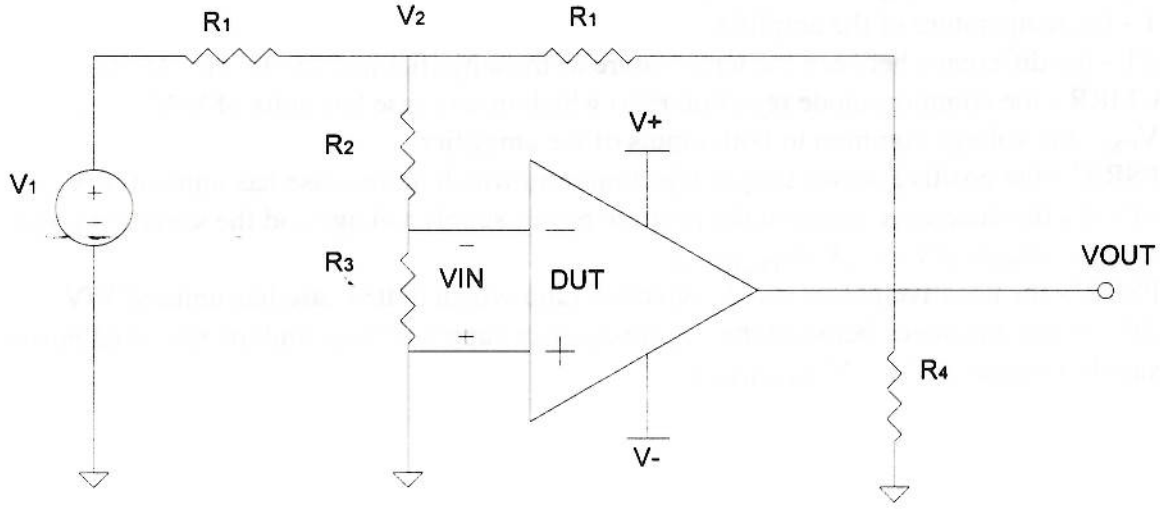
Appendix B: False Summing Junction Test Circuit

The test circuit shown below is essentially a unity gain, inverting op amp configuration. Resistors R_2 and R_3 simply gain up the input voltage V_{IN} such that the voltage V_2 is given by:

$$V_2 = -V_{IN}\left(1 + \frac{R_2}{R_3}\right)$$

The node labeled "V_2" is the summing junction of the circuit configuration. As in standard op amp configurations this node is approximated to be at ground for purposes of calculating the load:

$$R_{LOAD} \cong R_1 || R_4$$



The amount of error introduced into the circuit by R_2 and R_3 is proportional to the amount by which V_{IN} is gained up.

Suggested resistor values:
$R_1 = 10k\Omega$
$R_2 = 10k\Omega$
$R_3 = 100\ \Omega$
$R_4 = 2.5\ k\Omega$ for $R_{LOAD} \cong 2\ k\Omega$.

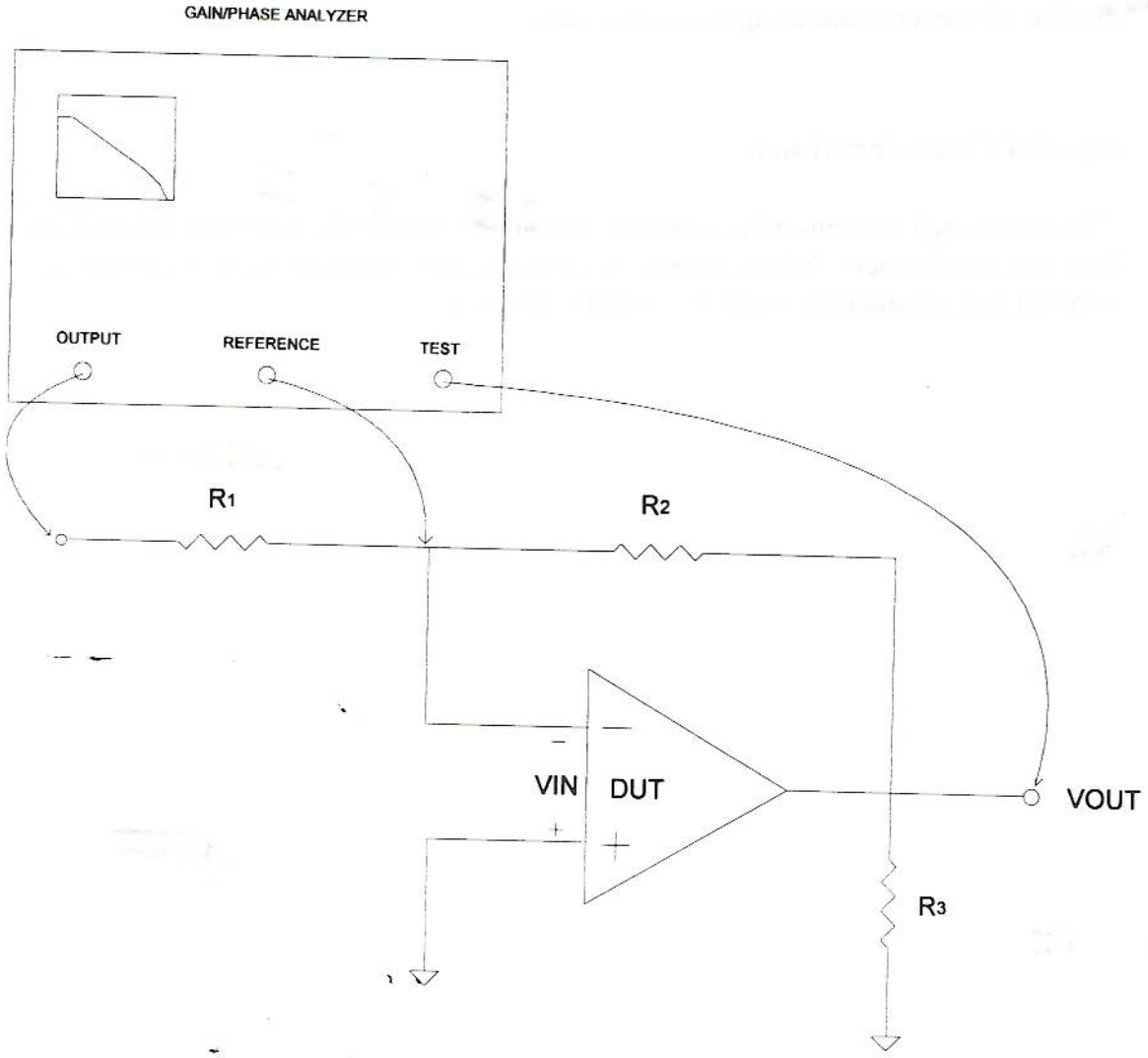
- A note about the power supplies: 3.3 μF tantalum capacitors are typically used to bypass both of the supplies to ground.

Op Amp Glossary of Terms
Part II: Performance Curves
Thatcher Klumpp, Aug. 22, 1995

Table of Contents

Performance Curve: Open-Loop Gain/Phase versus Frequency

Test Circuit:



Test Conditions:

- Set the power supplies to the specified value.
- Choose R_1 and R_2 to establish an arbitrary gain.
- Choose R_3 to establish the specified load: $R_{LOAD} \cong R_2 || R_3$.
- T = 25 °C

Test Method:

- Connect the Gain/Phase analyzer to the test circuit as shown and plot the test channel divided by the reference channel on a log scale.

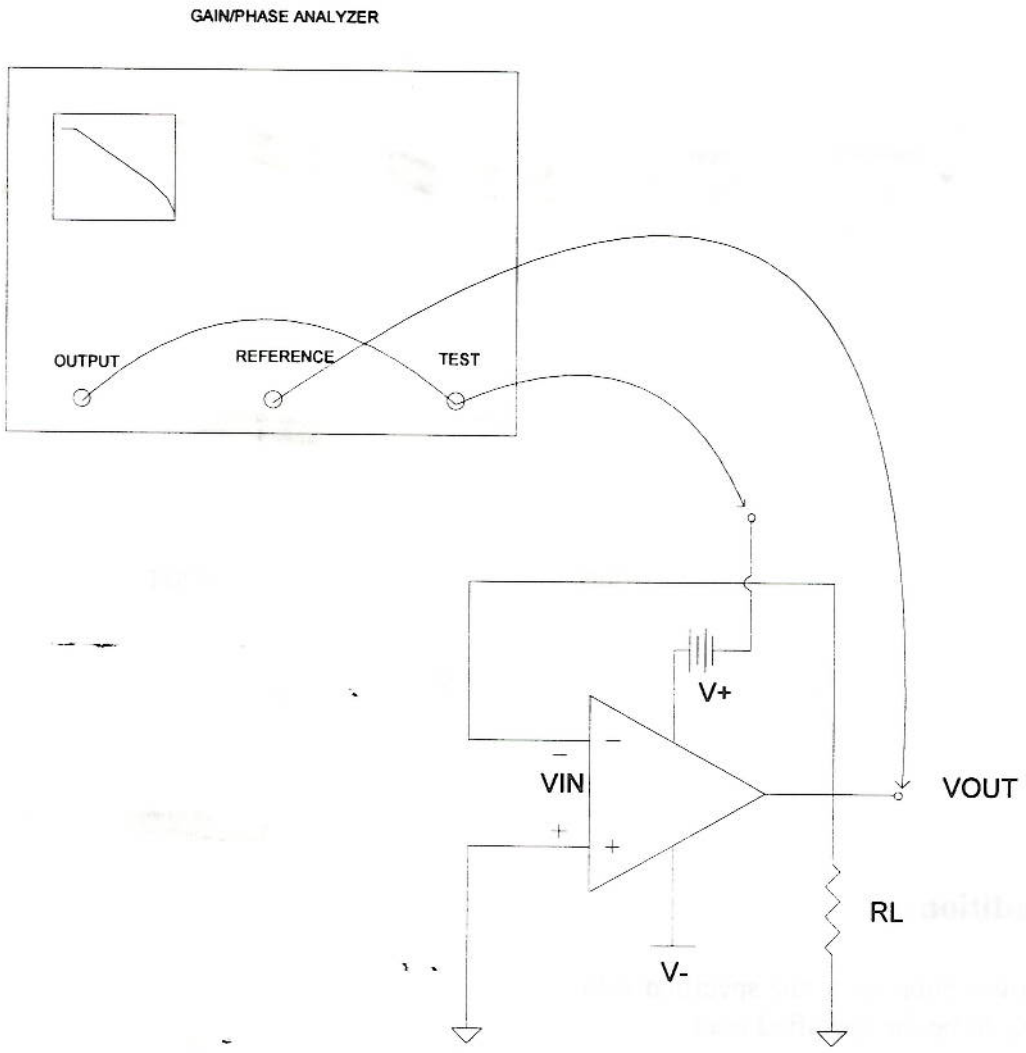
Special Considerations:

- The cable used to connect the summing junction voltage to the reference channel must have low capacitance. A large amount of parasitic capacitance between the inverting terminal and ground may cause the amplifier to oscillate.

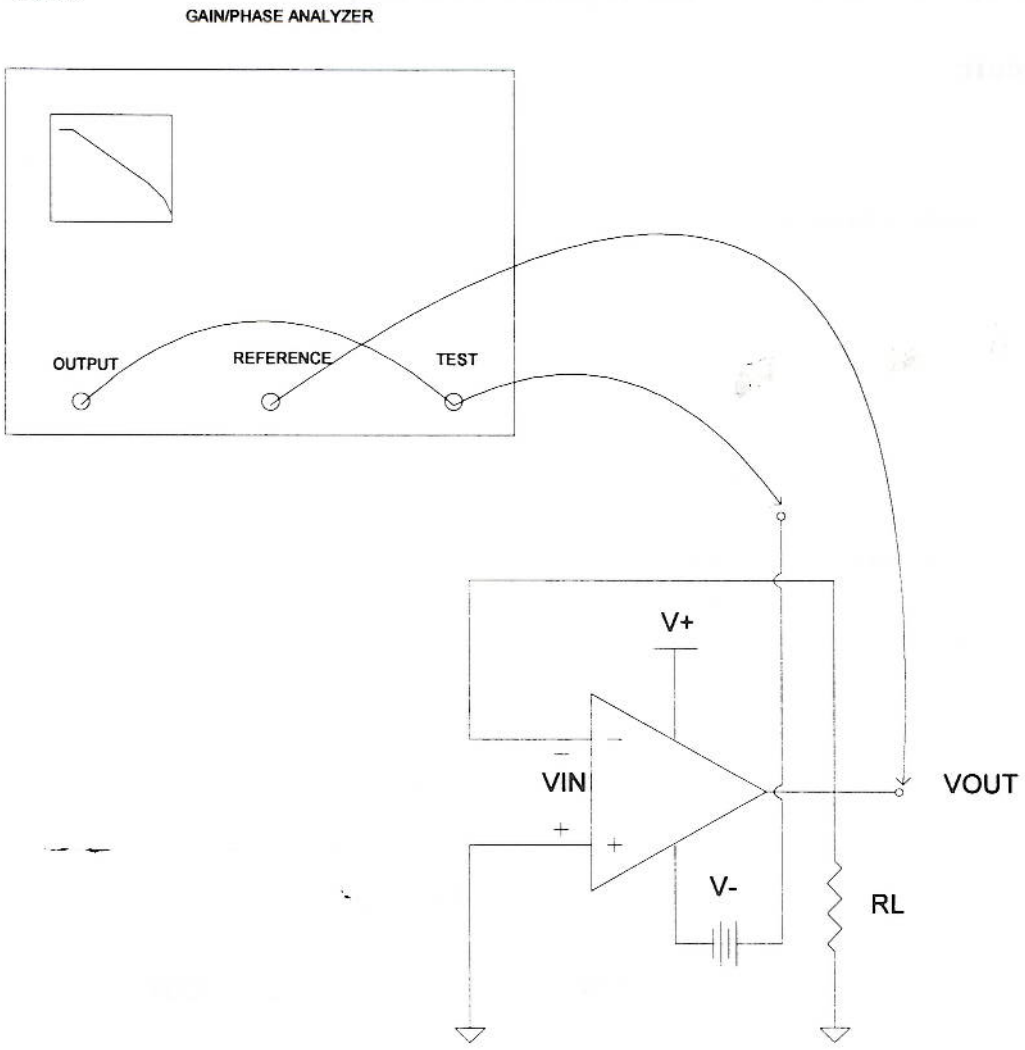
Performance Curve: Power Supply Rejection versus Frequency

Test Circuit:

+PSR:



-PSR:



Test Conditions:

- Set the power supplies to the specified value.
- Choose R_L to be the specified load.
- T = 25 °C

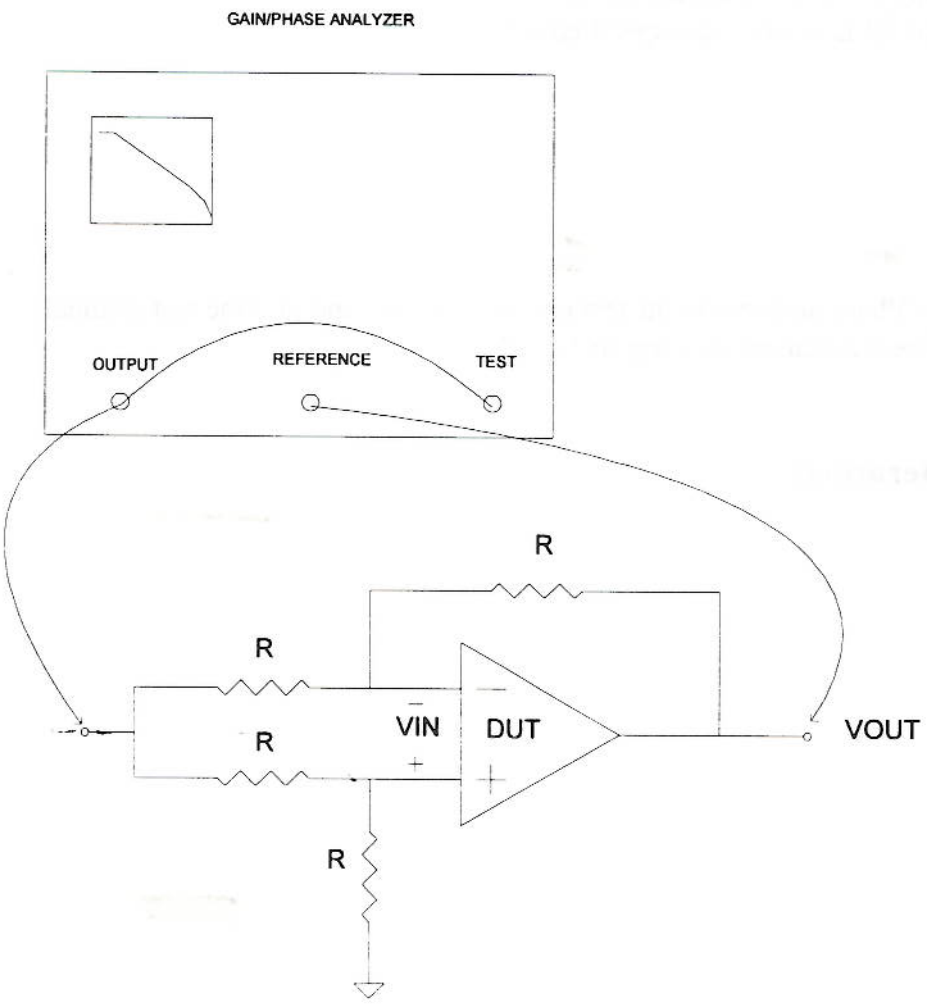
Test Method:

- Connect the Gain/Phase analyzer to the test circuits as shown and plot the test channel divided by the reference channel on a log scale for both +PSR and -PSR.

Special Considerations:

Performance Curve: Common-Mode Rejection versus Frequency

Test Circuit:



About the Test Circuit:

The op amp is connected in the difference amplifier configuration. Since all of the resistors are equal, the output is twice the differential input voltage. The input signal voltage is two times the common-mode voltage. Plotting the test channel voltage divided by the reference channel voltage accomplishes the CMR plot of V_{CM}/V_{IN} versus frequency.

Test Conditions:

- Set the power supplies to the specified value.
- Select R such that 2R is equal to the specified load.
- T = 25 °C

Test Method:

- Connect the Gain/Phase analyzer to the test circuit as shown and plot the test channel divided by the reference channel on a log scale.

Special Considerations:

Performance Curve: Input Bias and Input Offset Current versus Temperature

Test Circuit:

- Use either the integration technique or the large resistor method described for measuring input bias current.

Test Method:

- Measure the input bias current at various temperatures within the absolute maximum rated operating temperatures.
- Calculate the offset current at each data point.
- Plot both input bias and input offset current as a function of temperature.

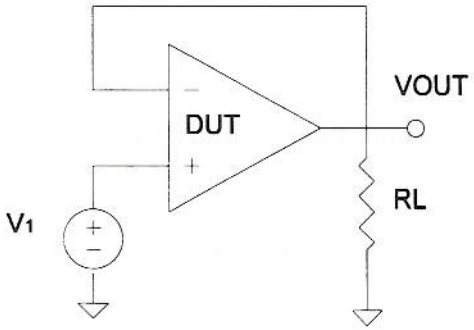
Special Considerations:

- Parasitic capacitances contributed by the test fixture and the input capacitances of the amplifier make this test difficult to carry out. Perf board or air-wiring may be required to obtain an acceptable plot on the Gain/Phase analyzer.

Performance Curve: Input Bias Current versus Input Common-Mode Voltage

Semiconductor Parameter Analyzer Method

Test Circuit:



Test Conditions:

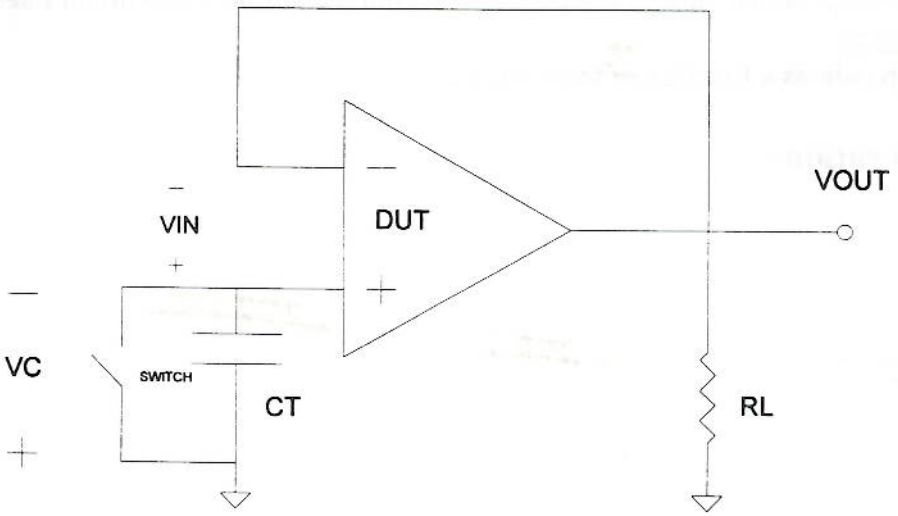
- Set the power supplies to the specified value.
- Choose R_L to be the specified load.
- T = 25 °C

Test Method:

- Use a semiconductor parameter analyzer to source the voltage V_1 and monitor the bias current.
- Sweep V_1 over the entire common-mode input voltage range.
- Plot the input bias current versus the common-mode voltage.

Integration Technique
Test Circuit:

- Use the integration technique described for measuring the input bias current flowing into the noninverting terminal of the amplifier:



Test Method:

Changing the common-mode voltage of this circuit configuration can be accomplished by changing the supply voltages while maintaining the specified voltage difference between V+ and V-. For instance, if V+ and V- were +15V and -15V, the common-mode voltage would be 0V. To make the common-mode voltage +10V, V+ would be 5V and V- would be -25V. To make the common-mode voltage -10V, V+ would be 25V and V- would be -5V.

- Measure the input bias current at various points over the common-mode input voltage range.

Note: The integration capacitor, C_T, should be chosen such that change in common-mode voltage is not significant during the integration time. 0-50mV should be sufficient.

- Plot I_B versus V_{CM} over the common-mode input voltage range.

Performance Curve: Open-Loop Gain versus Temperature

Test Circuit:

- Use the circuit described for measuring dc open loop gain.

Test Method:

- Measure the open-loop gain at various temperatures within the absolute maximum rated operating temperatures.
- Plot the open-loop gain as a function of temperature.

Special Considerations:

Performance Curve: Quiescent Current and Short Circuit Current versus Temperature

Test Circuit:

- Use the circuits described for measuring quiescent current and short-circuit current.

Test Method:

- Measure the quiescent current and short-circuit current at various temperatures within the absolute maximum rated operating temperatures.
- Plot the quiescent current and the short-circuit current as a function of temperature.

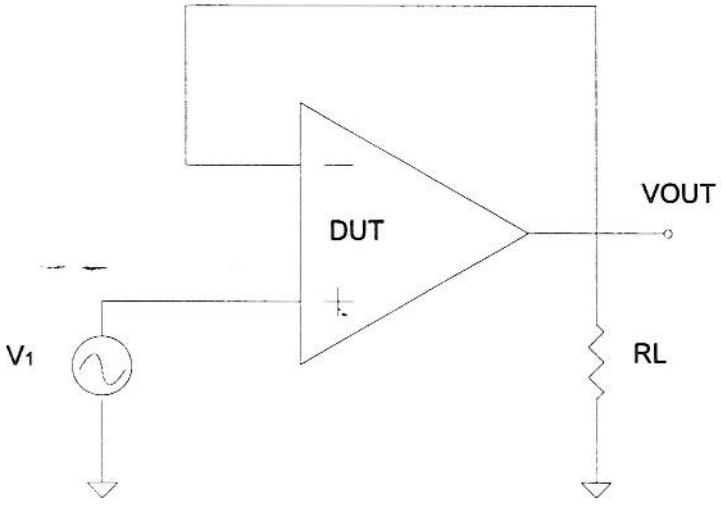
Special Considerations:

Performance Curve: Maximum Output Voltage versus Frequency

Definition: The maximum output voltage without slew-rate induced distortion. The maximum voltage is defined by the dc A_{OL} test conditions. For a given slew rate, the maximum frequency and maximum output voltage are related by:

$$f_{MAX} = \frac{SLEW\_RATE}{2\pi V_{OUT\_MAX}}.$$

Test Circuit:



Test Conditions:

- Set the power supplies to the specified value.
- Choose R_L to be the specified load.
- T = 25 °C

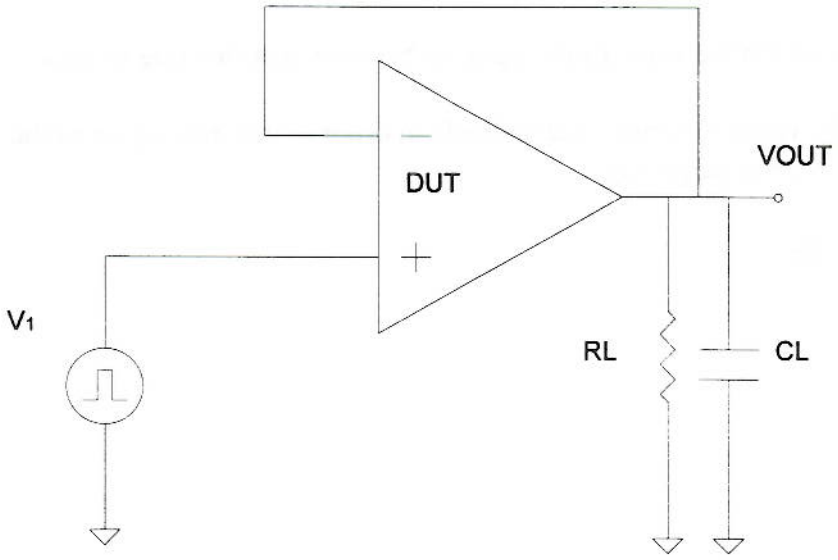
Test Method:

- Set the amplitude of the sinusoidal input voltage, V_1, to the A_{OL} output voltage condition.
- Adjust the frequency of V_1 and observe the output voltage of the amplifier on an oscilloscope.
- Record the frequency at which the wave form begins to become distorted due to slew limiting.
- Repeat this procedure for various output voltage levels in order to generate a plot of the maximum output voltage versus frequency.

Special Considerations:

Performance Curve: Small-Signal and Large-Signal Step Response

Test Circuit:



Test Conditions:

- Set the power supplies to the specified value.
- Choose R_L to be the specified resistive load.
- Choose C_L to be the specified load capacitance.
- T = 25 °C

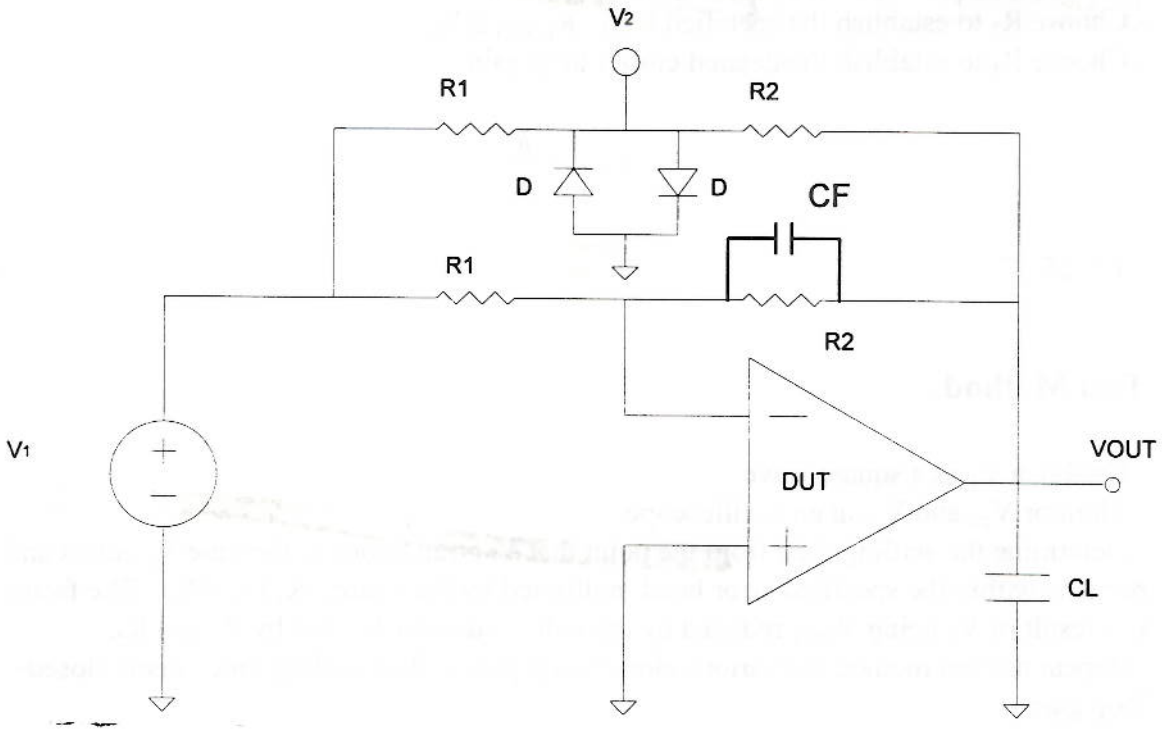
Test Method:

- Establish V_1 to be a square wave with the specified amplitude and frequency. For the small-signal case, the amplitude is typically ±100 mV with a frequency of 500 kHz. For the large-signal case, the amplitude is typically ±10 V with a frequency of 100 kHz.
- Monitor V_{OUT} on an oscilloscope.

Special Considerations:

Performance Curve: Settling Time versus Closed-Loop Gain

Test Circuit:



About the Test Circuit:

- The voltage gain V_{OUT}/V_{IN} equals $-R_2/R_1$.
- The voltage V_2 is given by a weighted subtraction of the input and output:

$$V_2 = \frac{R_1}{R_1 + R_2} V_{OUT} + \frac{R_2}{R_1 + R_2} V_1.$$

- The two diodes clamp the voltage V_2 in order to avoid overloading the oscilloscope when measuring very small voltages. The diodes should be fast reverse recovery diodes such as the HP-5082-2835.

Test Conditions:

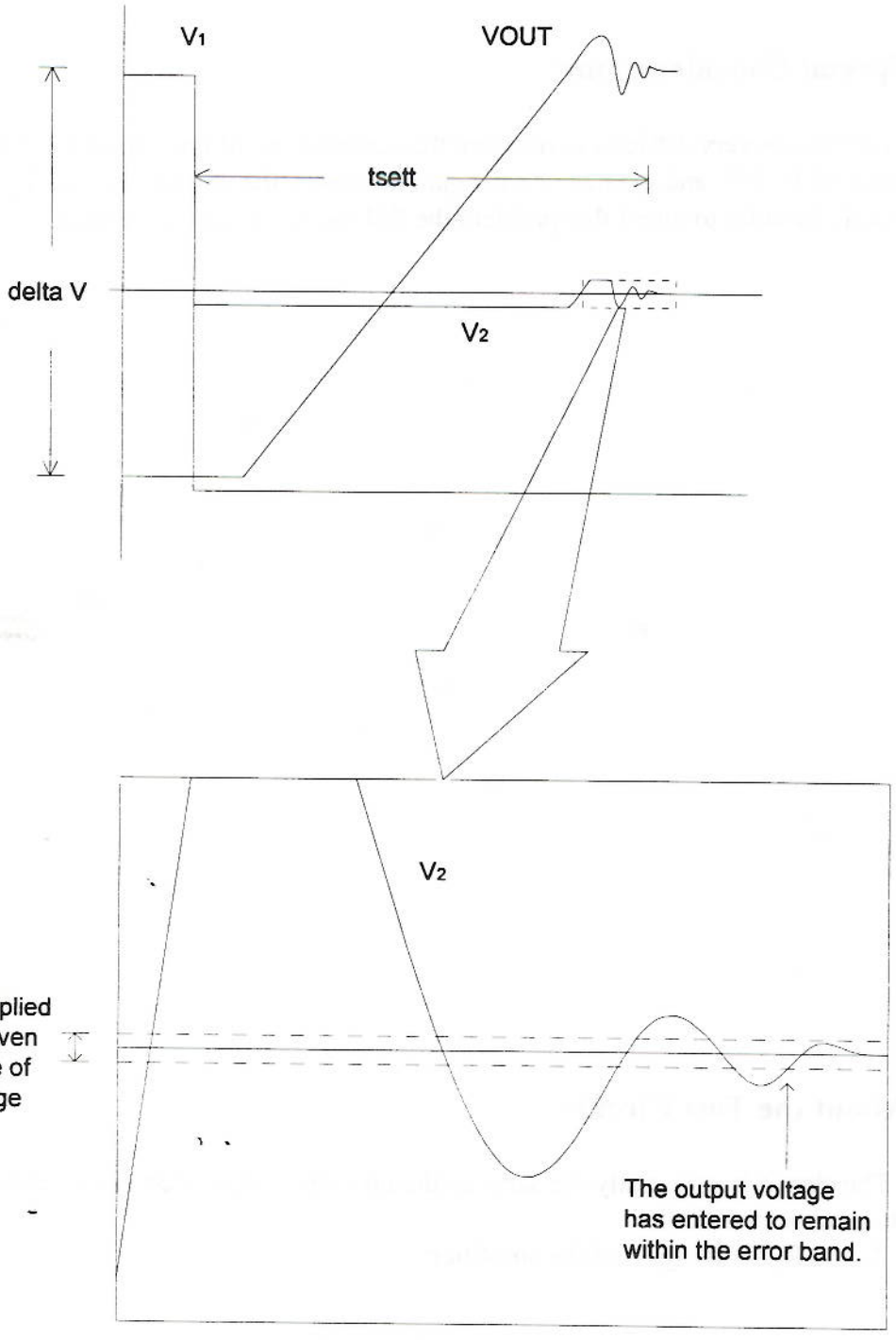
- Set the power supplies to the specified value.
- Choose C_L as the specified load capacitance.
- Choose R_2 to establish the specified load: $R_{LOAD} \cong R_2/2$.
- Choose R_1 to establish the desired closed-loop gain:

$$A_{CL} = -\frac{R_2}{R_1}.$$

- T = 25 °C

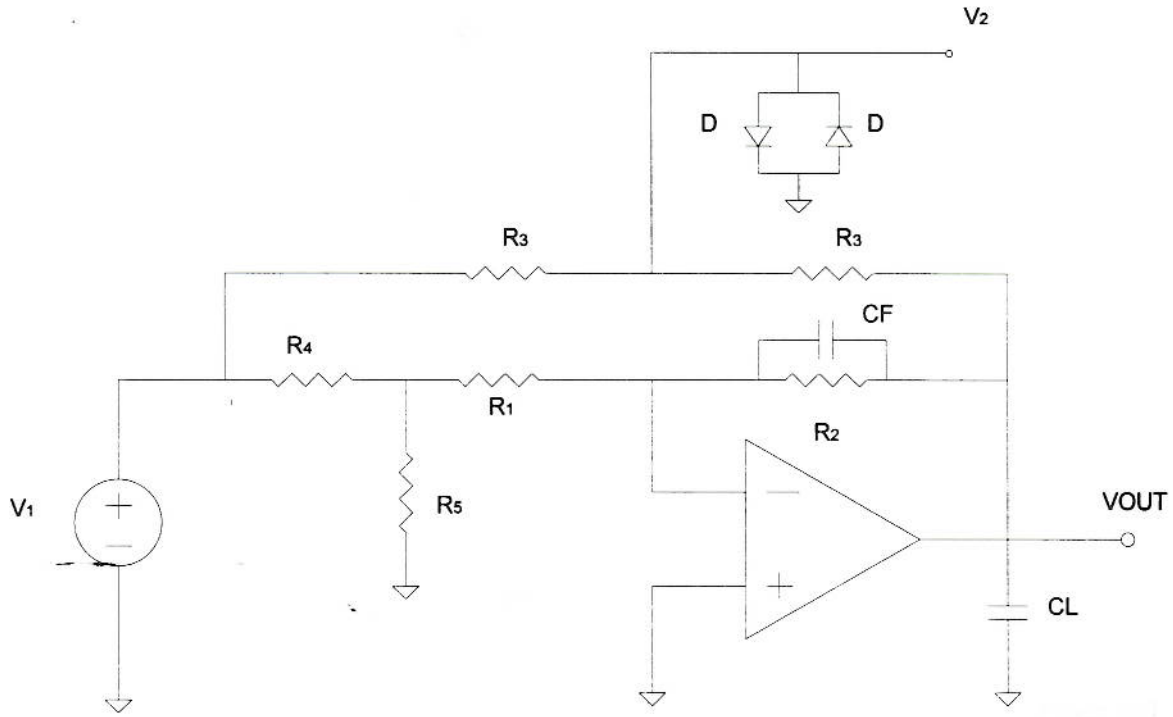
Test Method:

- Establish V_1 as a square wave.
- Monitor V_{IN} and V_2 on an oscilloscope.
- Determine the settling time from the point that V_{IN} transitions to the time V_2 enters and remains within the specified error band multiplied by the factor, $R_1/(R_1+R_2)$. The factor is a result of V_2 being V_{OUT} reduced by the voltage divider formed by R_1 and R_2.
- Repeat the test method for various closed-loop gains. Plot settling time versus closed-loop gain.


V1
VOUT
tsett
delta V
V2
V2
The specified error band multiplied by R1/(R1+R2)given as a percentage of the output voltage step
The output voltage has entered to remain within the error band.

Special Considerations:

- It becomes very difficult to measure the settling time of the circuit described above for gains of 10 V/V and greater. As the gain increases, the voltage level at V_2 becomes very small. In order to avoid this problem the following circuit can be used:



About the Test Circuit:

- The circuit is essentially the same as the previously described circuit except that R_4 and R_5 have been added.
- R_1 and R_2 set the gain of the amplifier:

$$A_{CL} = -\frac{R_2}{R_1}.$$

- The gain of the complete circuit should be chosen to be -1 V/V.

- Resistors R_4 and R_5 must be chosen to divide V_1 by the amount that resistors R_1 and R_2 gain up the signal. An example choice of resistor values would be:

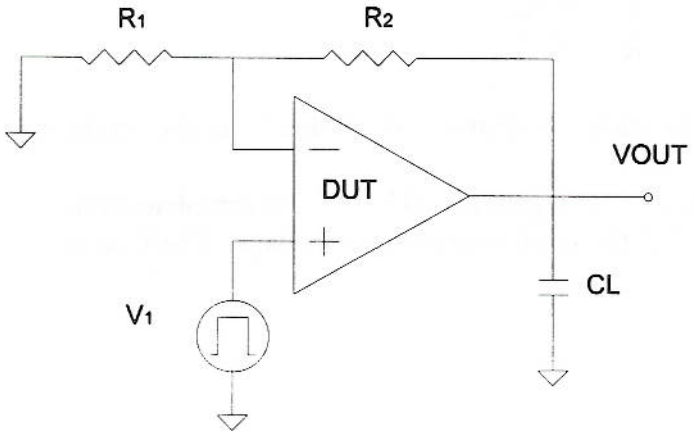
$$R_1 = 1\ k\Omega$$
$$R_2 = 10\ k\Omega$$
$$R_3 = 2.5\ k\Omega$$
$$R_4 = 90\ \Omega$$
$$R_5 = 10\ \Omega.$$

- Resistors R_4 and R_5 are chosen to be small compared to R_1 so that V_1 is divided by the resistor divider: $R_5/(R_5+R_4)$.
- These choices of resistors place the DUT in a gain of -10 V/V. The complete circuit is in a gain of -1 V/V and V_2 is one half of the small signal output voltage. The load is approximately $R_3||R_2 = 2\ k\Omega$.

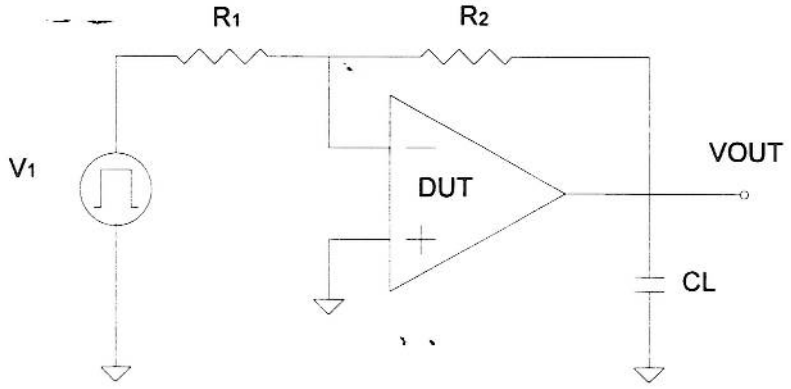
Performance Curve: Small-Signal Overshot versus Load Capacitance

Test Circuit:

Use the standard noninverting configuration for positive gains:



Use the standard inverting configuration for negative gains.



Test Conditions:

- Set the power supplies to the specified value.
- Choose R_2 to be the specified resistive load.
- Choose C_L to be the load capacitance.
- T = 25 °C

Test Method:

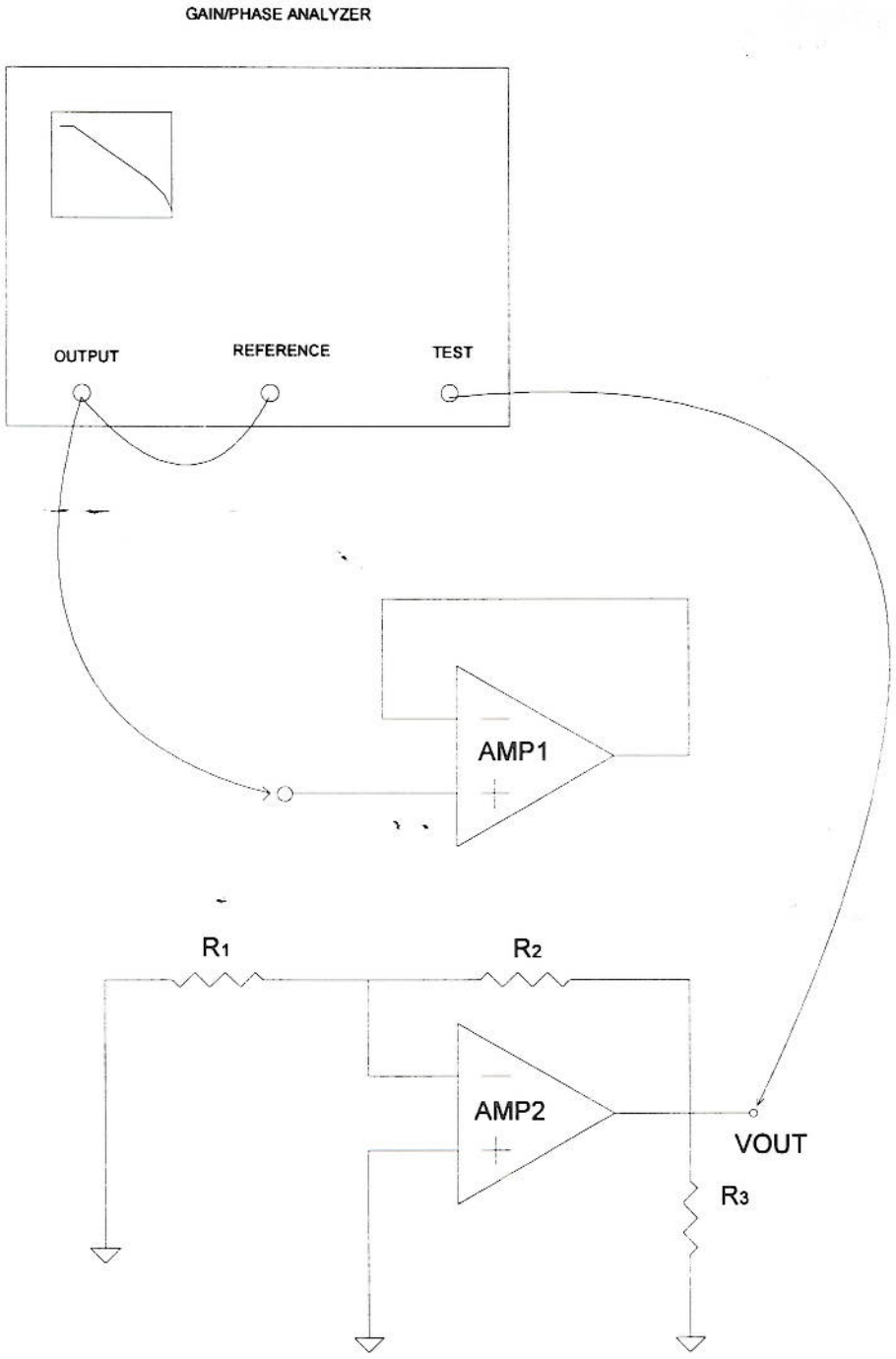
- Establish V_I to be a small-signal square wave. The amplitude of V_{OUT} is typically ±100 mV with a frequency of 500 kHz.
- Observe V_{OUT} on an oscilloscope. Measure the amount that V_{OUT} overshoots the target output voltage.
- Repeat the test method for various closed-loop gains and load capacitances.
- Plot the percentage overshot as a function of load capacitance for various gains.

Special Considerations:

Performance Curve: Channel Separation versus Frequency. This performance test is for characterizing dual and quad-packaged amplifiers.

Definition: The gain measured from the input of one amplifier to the output of a second amplifier in the same package.

Test Circuit:



Test Conditions:

- Set the power supplies to the specified value.
- Choose R_1 and R_2 to establish a gain of 100 V/V.
- Choose R_3 to establish the specified load: $R_{LOAD} \cong R_2 || R_3$.
- T = 25 °C

Test Method:

- Connect the Gain/Phase analyzer to the test circuit as shown and plot the test channel divided by the reference channel on a log scale.

- Normalize the plot to a gain of one.

Special Considerations:

- The choice of gain for this test is only to make the output easier to measure. Care must be taken when selecting the gain of AMP #2 so that the channel separation versus frequency plot is not dominated by the bandwidth limit of the gain configuration of AMP #2.

Performance Curve: Input Voltage and Current Noise Spectral Density versus Frequency

Test Circuit:

Use the circuits described to measure input current and noise density.

Test Method:

- Determine the voltage and current noise density over the specified frequency and plot them on the same graph.

Special Considerations:

Performance Curve: Total Harmonic Distortion and Noise versus Frequency

Test Circuit:

- Use the circuit described to measure total harmonic distortion.

Test Method:

- Measure THD over the specified frequency range.
- Repeat the test method for various closed-loop gains.
- Plot THD for each closed-loop gain configuration versus frequency.

Special Considerations: