



DSP原理与应用

The Technology & Applications of DSP

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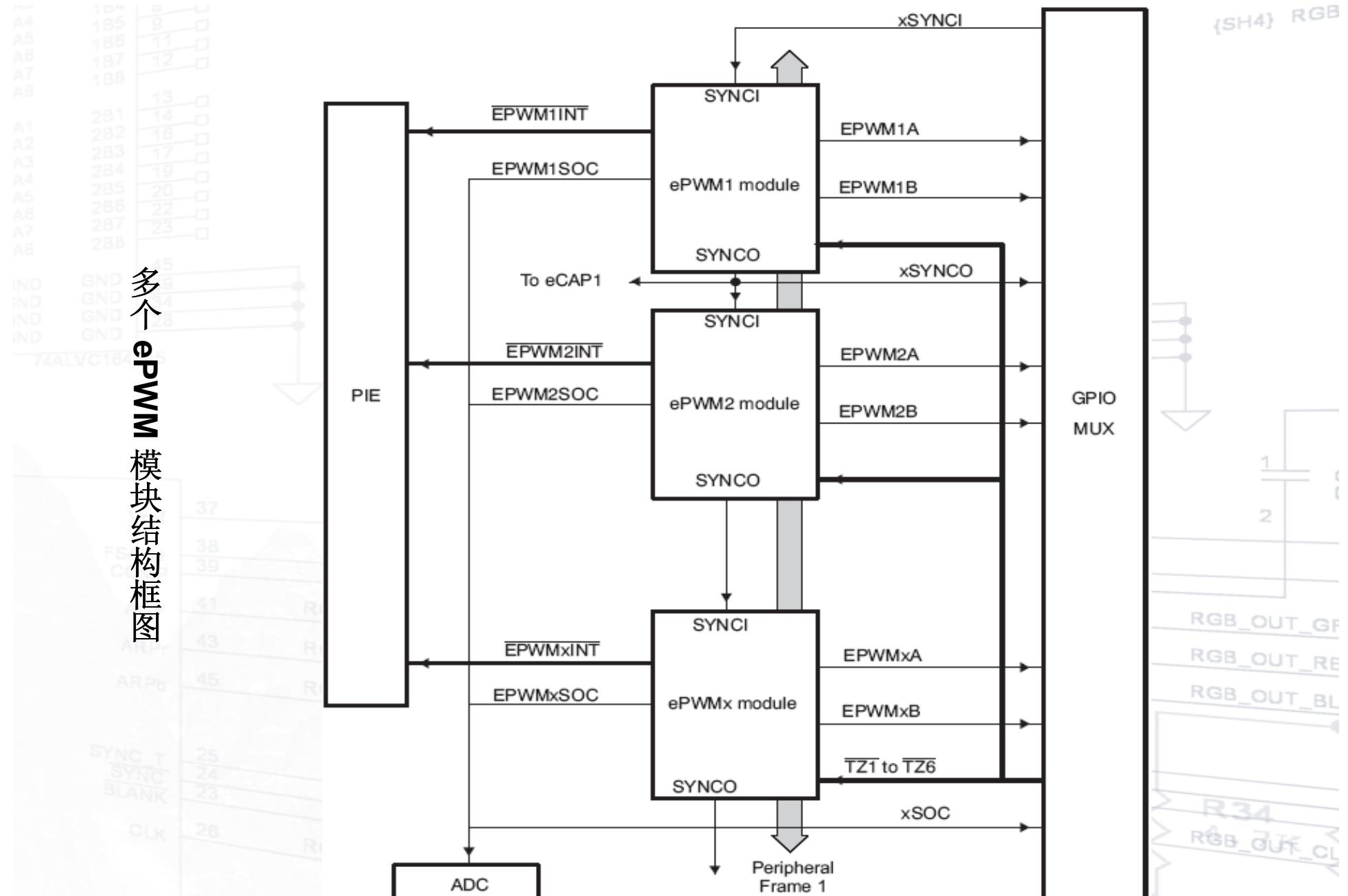
TEXAS
INSTRUMENTS



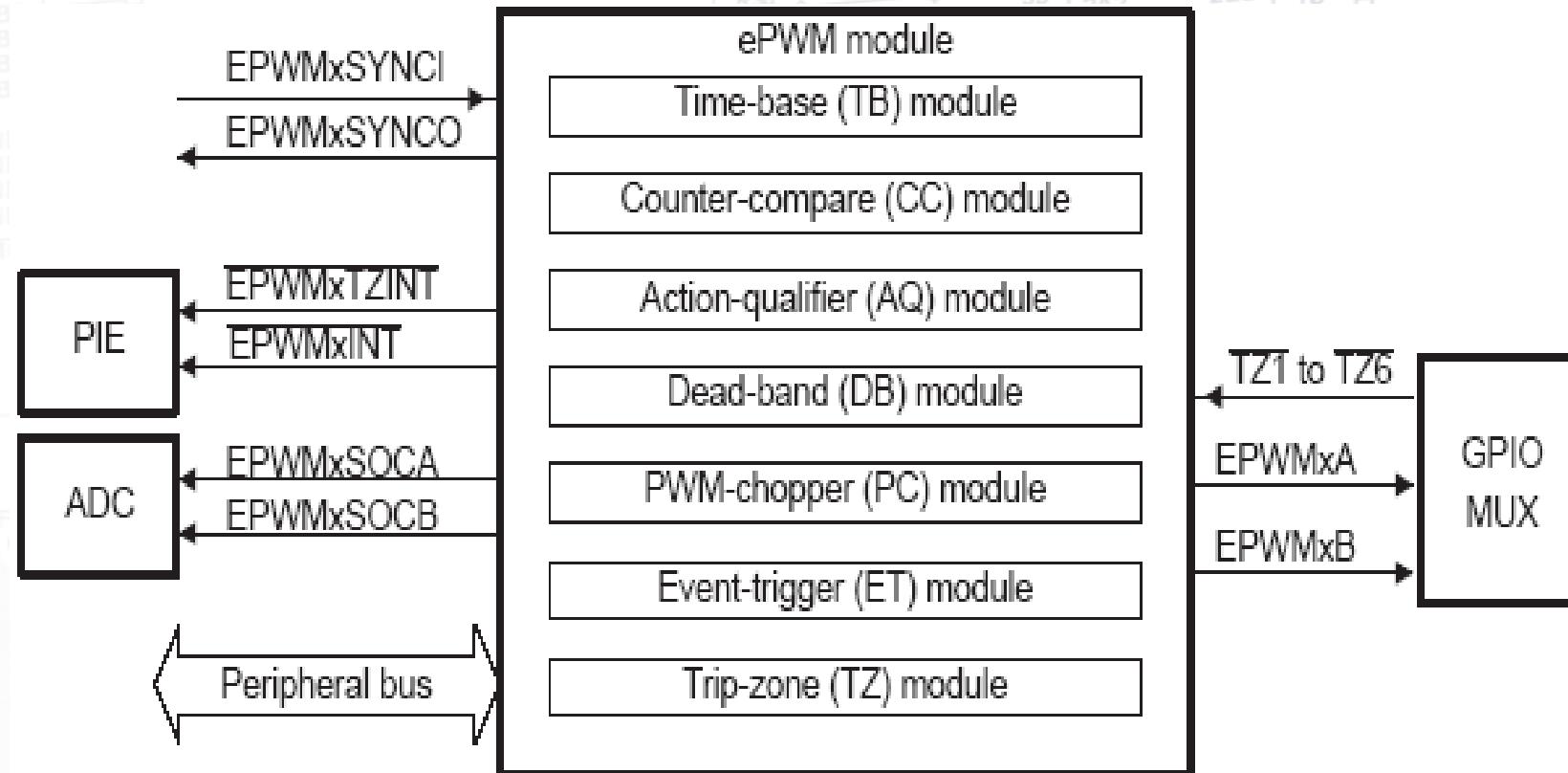
§ 7.1 F28335的PWM控制

- 每个ePWM模块都支持下列特性:
 - 精确的16位时间定时器，可以进行周期和频率控制。
 - 两个PWM输出(**EPWMxA and EPWMxB**) 可以用于下面的控制
 - 两个独立的**PWM**输出进行单边控制
 - 两个独立的**PWM**输出进行双边对称控制
 - 一个独立的**PWM**输出进行双边非对称控制
 - 与其它ePWM模块有关的可编程超前和滞后相控。
 - 在一个循环基础上的硬件锁定(同步)相位关系。
 - 独立的上升沿和下降沿死区延时控制
 - 可编程控制故障区(**trip zone**) 用于故障时的周期循环控制(**trip**)和单次(**one-shot**)控制。
 - 一个控制条件可以使**PWM**输出强制为高, 低, 或高阻逻辑电平.
 - 所有事件都可以触发**CPU**中断, 启动**ADC**开始转换。
 - 可编程事件有效降低了在中断时**CPU**的负担。
 - PWM**高频载波信号对于脉冲变压器门极驱动非常有用。





ePWM模块的子模块和信号连接



模块相关信号说明如下：



- **PWM 输出信号 (EPWMx A and EPWMx B) (x=1...6)**
- 通过**IO**引脚输出**PWM**信号.
- **Trip-zone 信号 (TZ1 to TZ6).**

这些输入信号警告ePWM模块有外部故障发生。设备的每个模块都可以配置成使用或者忽略任何故障区信号（**Trip-zone**）。这些信号可以设置为通用IO外设的异步输入。

- 基于时间的同步输入信号 (**EPWMxSYNCl**) 和输出 (**EPWMxSYNCO**) 信号.

同步信号雏菊花形将ePWM模块连接在一起。每个模块可以配置成使用或忽略其同步输入信号。产生到引脚的时钟同步输入和输出信号只能是ePWM1 (ePWM module #1)。ePWM1的同步输出信号 EPWM1SYNCO也连接到第一个增强捕获单元eCAP1模块的SYNCl。

● ADC start-of-conversion signals (EPWMxSOCA and EPWMxSOCB).

每个ePWM模块有两个ADC开始转换信号（每个ADC转换序列一个）任何ePWM模块都可触发任何一个序列。哪个事件触发ADC开始转换，可以在事件触发子模块中可以设计。

- 外设总线 (Peripheral Bus)
- 外设总线是 32-bits 宽, 允许16-bit和32-bit方式写入 ePWM 寄存器文件。

ePWM模块相关寄存器

{SH4} RGB

Table 1-1. ePWM Module Control and Status Register Set Grouped by Submodule

Name	Offset ⁽¹⁾	Size (x16)	Shadow	Description
Time-Base Submodule Registers				
TBCTL	0x0000	1	No	Time-Base Control Register
TBSTS	0x0001	1	No	Time-Base Status Register
TBPHSHR	0x0002	1	No	Extension for HRPWM Phase Register ⁽²⁾
TBPHS	0x0003	1	No	Time-Base Phase Register
TBCTR	0x0004	1	No	Time-Base Counter Register
TBPRD	0x0005	1	Yes	Time-Base Period Register
Counter-Compare Submodule Registers				
CMPCTL	0x0007	1	No	Counter-Compare Control Register
CMPAHR	0x0008	1	No	Extension for HRPWM Counter-Compare A Register ⁽²⁾
CMPA	0x0009	1	Yes	Counter-Compare A Register
CMPB	0x000A	1	Yes	Counter-Compare B Register
Action-Qualifier Submodule Registers				
AQCTLA	0x000B	1	No	Action-Qualifier Control Register for Output A (EPWMx _A)
AQCTLB	0x000C	1	No	Action-Qualifier Control Register for Output B (EPWMx _B)
AQSFRC	0x000D	1	No	Action-Qualifier Software Force Register
AQCSFRC	0x000E	1	Yes	Action-Qualifier Continuous S/W Force Register Set





{SH4} RGB

Dead-Band Generator Submodule Registers

DBCTL	0x000F	1	No	Dead-Band Generator Control Register
DBRED	0x0010	1	No	Dead-Band Generator Rising Edge Delay Count Register
DBFED	0x0011	1	No	Dead-Band Generator Falling Edge Delay Count Register

Trip-Zone Submodule Registers

TZSEL	0x0012	1	No	Trip-Zone Select Register
TZCTL	0x0014	1	No	Trip-Zone Control Register ⁽³⁾
TZEINT	0x0015	1	No	Trip-Zone Enable Interrupt Register ⁽³⁾
TZFLG	0x0016	1	No	Trip-Zone Flag Register ⁽³⁾
TZCLR	0x0017	1	No	Trip-Zone Clear Register ⁽³⁾
TZFRC	0x0018	1	No	Trip-Zone Force Register ⁽³⁾

Event-Trigger Submodule Registers

ETSEL	0x0019	1	No	Event-Trigger Selection Register
ETPS	0x001A	1	No	Event-Trigger Pre-Scale Register
ETFLG	0x001B	1	No	Event-Trigger Flag Register
ETCLR	0x001C	1	No	Event-Trigger Clear Register
ETFRC	0x001D	1	No	Event-Trigger Force Register

PWM-Chopper Submodule Registers

PCCTL	0x001E	1	No	PWM-Chopper Control Register
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High-Resolution Pulse Width Modulator (HRPWM) Extension Registers

HRCNFG	0x0020	1	No	HRPWM Configuration Register ⁽²⁾⁽³⁾
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§ 7.1.1 ePWM主要子模块配置参数说明

一、时基Time-base (TB)

标定与系统时钟 (SYSCLKOUT) 有关的时基时钟, 配置PWM时基计数器 (TBCTR) 的频率或周期.

设置时基计数器的下列参数:

- 计数增模式: 用于非对称PWM
- 计数器减模式: 用于非对称PWM
- 计数增-减模式: 用于对称PWM

配置与另一个ePWM模块的时基相位关系.

通过硬件或软件同步不同模块之间的时基定时器

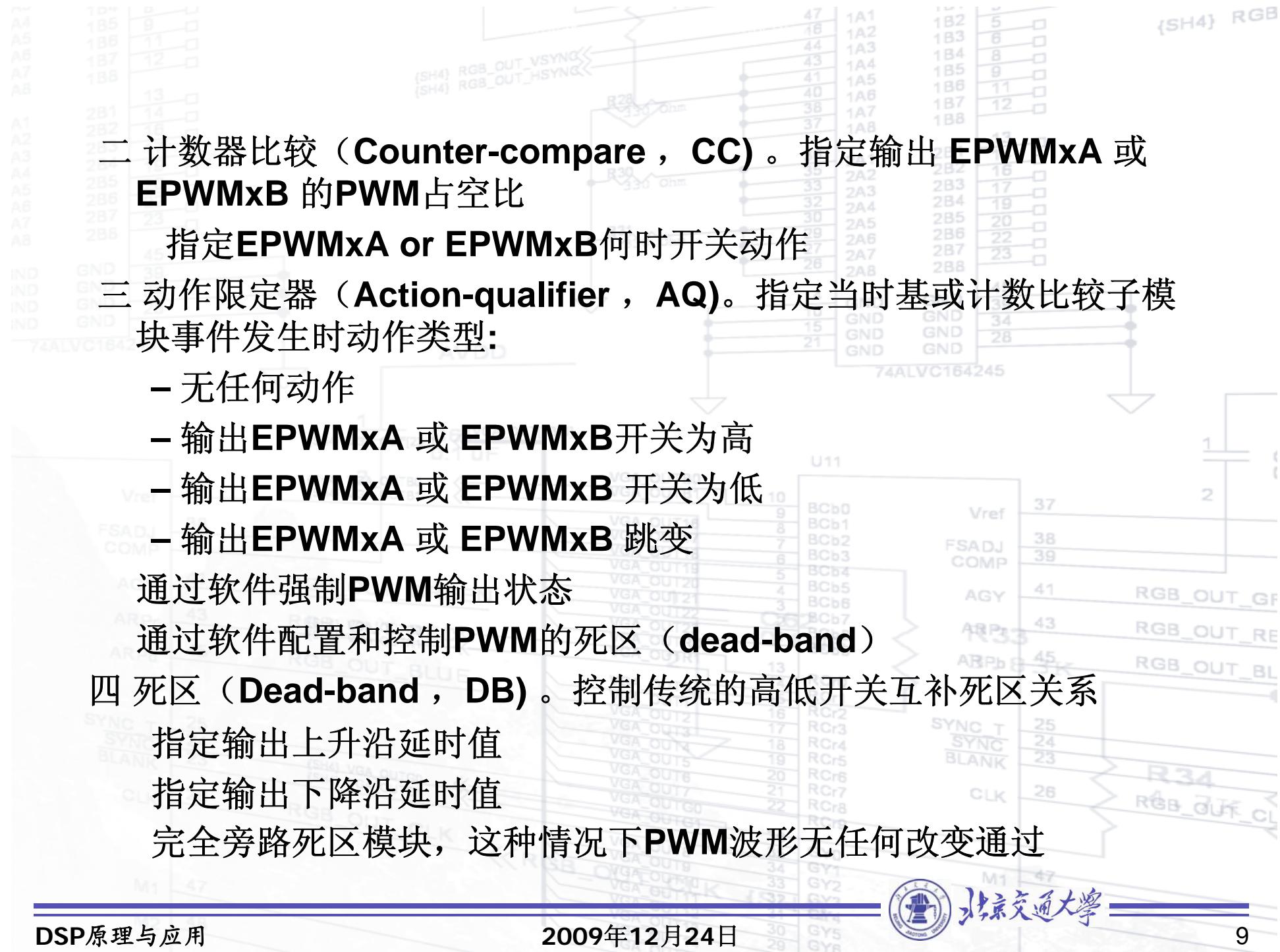
在同步事件之后配置时基计数器的方向 (增或减)

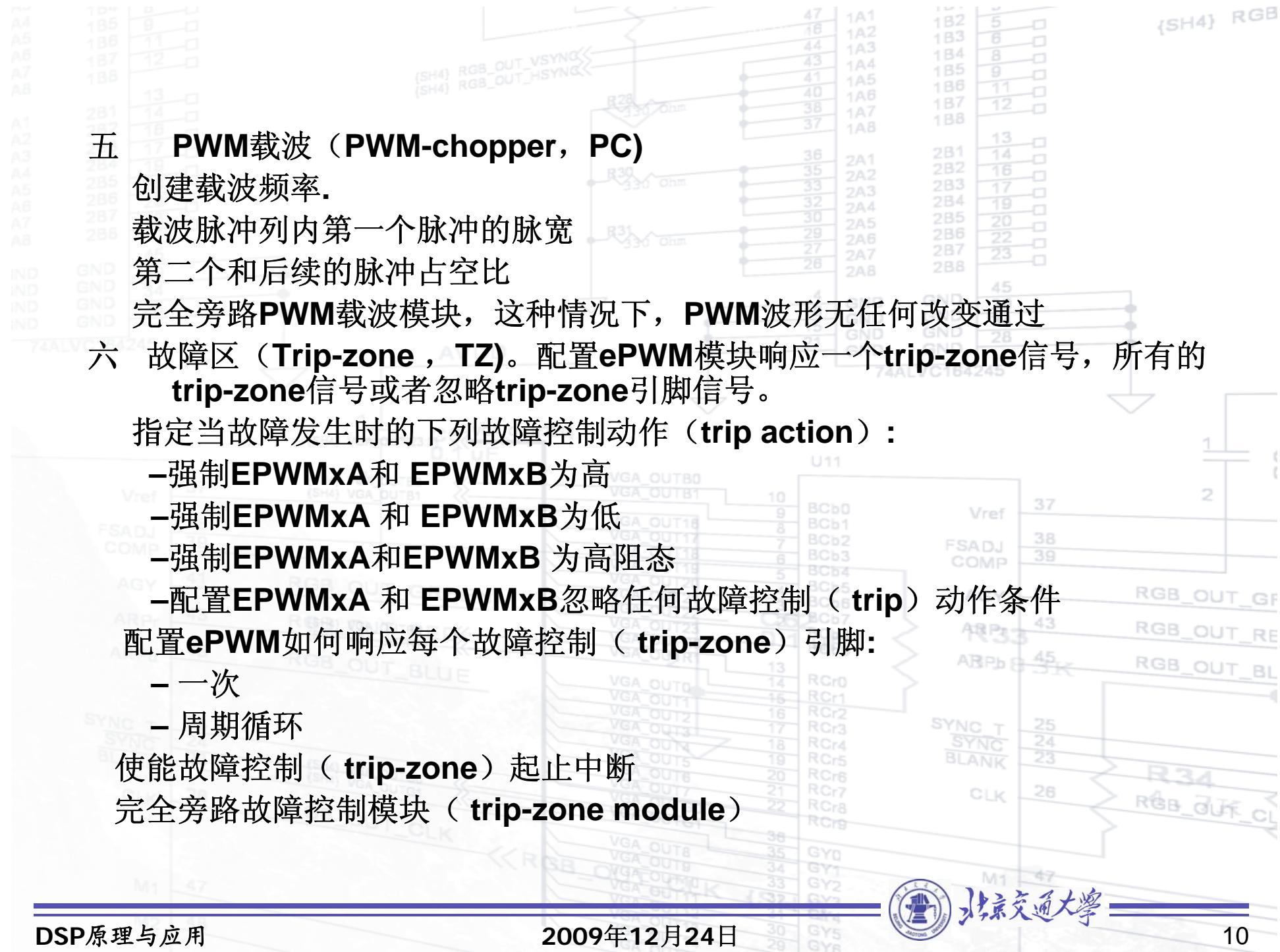
配置仿真器 (emulator) 终止DSP时时基计数器的行为.

指定ePWM模块同步输出源:

- 同步输入信号
- 时基计数器等于零
- 时基计数器等于计数器比较器 B (CMPB)
- 无输出同步信号产生







五 PWM载波 (PWM-chopper, PC)

创建载波频率.

载波脉冲列内第一个脉冲的脉宽

第二个和后续的脉冲占空比

完全旁路**PWM**载波模块，这种情况下，**PWM**波形无任何改变通过

六 故障区 (Trip-zone , TZ)。配置ePWM模块响应一个trip-zone信号，所有的 trip-zone信号或者忽略trip-zone引脚信号。

指定当故障发生时的下列故障控制动作 (trip action) :

- 强制EPWMxA和EPWMxB为高
- 强制EPWMxA和EPWMxB为低
- 强制EPWMxA和EPWMxB为高阻态
- 配置EPWMxA和EPWMxB忽略任何故障控制(trip)动作条件

配置ePWM如何响应每个故障控制（trip-zone）引脚

- 一次
- 周期循环

使能故障控制 (trip-zone) 起止中断

完全旁路故障控制模块 (trip-zone module)

§ 7.1.2 计算PWM周期和频率

PWM事件频率由时基周期寄存器**TBPRD** 和时基计数器模式决定。下图给出在时基计数器增模式，减模式和增减模式下**PWM**周期**T_{pwm}**和频率**F_{pwm}**关系。周期设置为4 (**TBPRD = 4**)。每一步增加时间由时基时钟**TBCLK**决定，时基时钟由系统时钟**SYSCLKOUT**标定。

(1) Up-Down-Count Mode:

在增减模式下，时基计数器从零开始，增加直到达到周期值(**TBPRD**)，然后开始减小直到达到零。这样计数器重复模式，开始增加。

(2) Up-Count Mode:

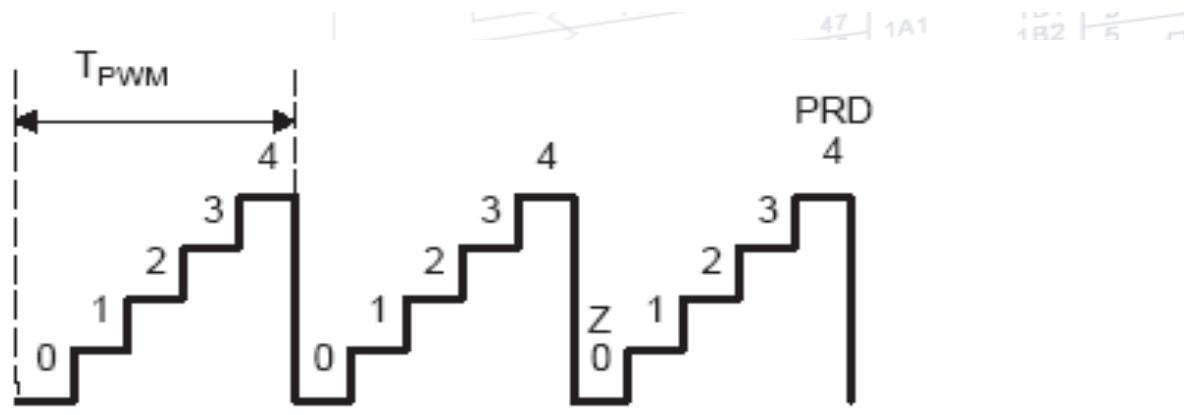
在增计数模式，时基计数器从零开始增加，直到达到周期寄存器值(**TBPRD**)。然后时基计数器复位到零，再次开始增加。

(3) Down-Count Mode:

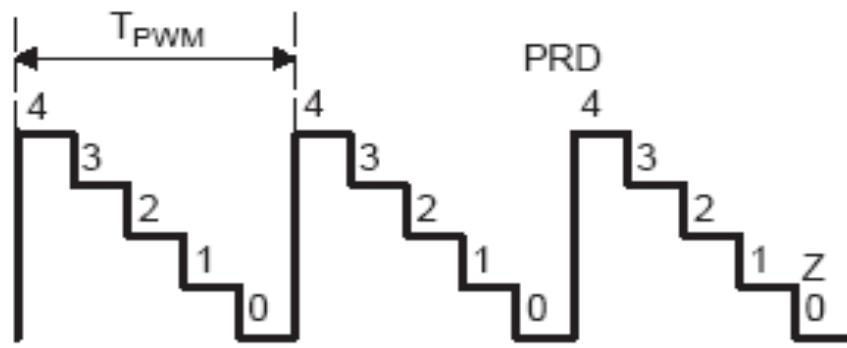
在减模式，时基计数器开始从周期值(**TBPRD**)开始减小，直到达到零。当达到零时，时基计数器复位到周期值，再次开始增计数。



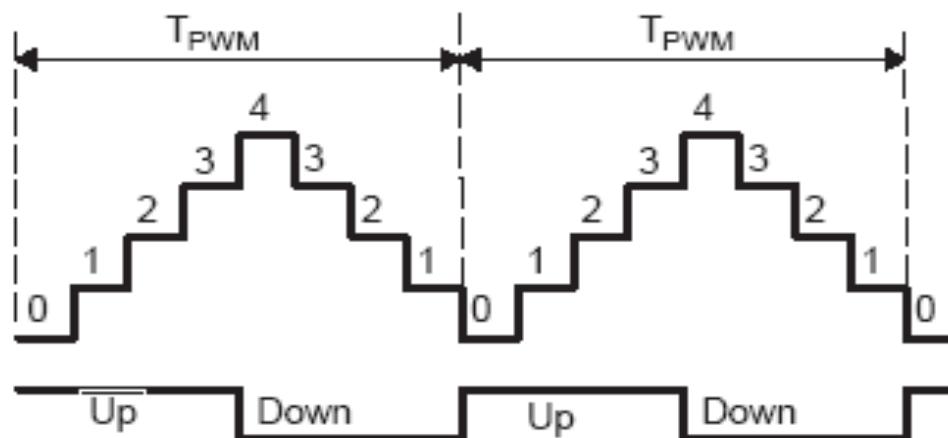
时基频率和周期



For Up Count and Down Count
 $T_{PWM} = (TBPRD + 1) \times T_{TBCLK}$
 $F_{PWM} = 1 / (T_{PWM})$



For Up and Down Count
 $T_{PWM} = 2 \times TBPRD \times T_{TBCLK}$
 $F_{PWM} = 1 / (T_{PWM})$



§ 7.1.3 时基周期影像寄存器

激活寄存器 (Active Register)

激活寄存器控制硬件，负责硬件动作发生 (cause) 或唤醒 (invoke) 影像寄存器 (Shadow Register)

影像寄存器为激活寄存器缓冲或提供临时保存位置。对硬件没有直接的控制。在特定时刻影像寄存器内容转移到激活寄存器。这样阻止由于寄存器被软件移步修改造成冲突或错误。

时基周期寄存器影像模式：

当 **TBCTL[PRDLD] = 0** 时，**TBPRD** 影像寄存器使能。当读和写 **TBPRD** 寄存器，在时基寄计数器为零时 (**TBCTR = 0x0000**)，影像寄存器内容转移到激活寄存器 (**TBPRD (Active) ← TBPRD (shadow)**)。默认 **TBPRD** 影像寄存器处于使能状态。

时基周期立即装入模式：

如果 (**TBCTL[PRDLD] = 1**) 则立即装入模式选择，则读写 **TBPRD** 寄存器直接改变激活寄存器。



§ 7.1.4 时基计数器同步

每个ePWM模块都有一个同步输入(**EPWMxSYNCI**)和一个同步输出(**EPWMxSYNCO**). 第一个ePWM1的同步输入来自外部引脚。每个ePWM模块可以设置成使用或忽略同步脉冲输入。如果**TBCTL** [**PHSEN**] 位置位，则当具备下列条件之一时，ePWM模块的时基计数器将自动装入相位寄存器(**TBPHS**)的内容。

同步输入脉冲**EPWMxSYNCI**:

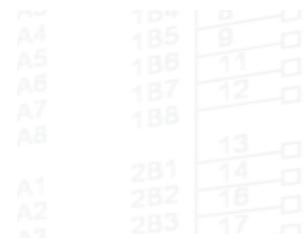
当检测到输入同步脉冲时,相位寄存器值装入计数寄存器(**TBPHS**—>**TBCNT**). 这种操作发生在下一个有效时基时钟沿

软件强制同步脉冲:

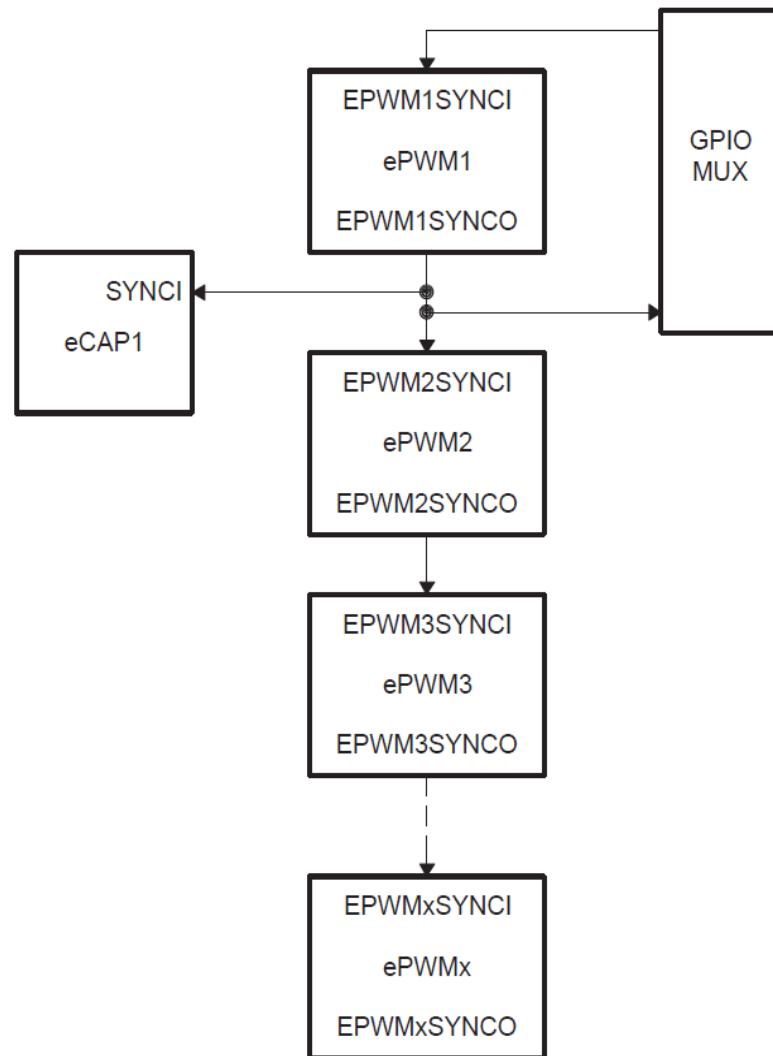
向**TBCTL[SWFSYNC]** 控制位写1产生一个软件强制同步。该脉冲与同步输入信号是或关系，因此与在**EPWMxSYNCI**上的脉冲具有同样的效果。

下图给出了ePWM模块的可能的同步连接。

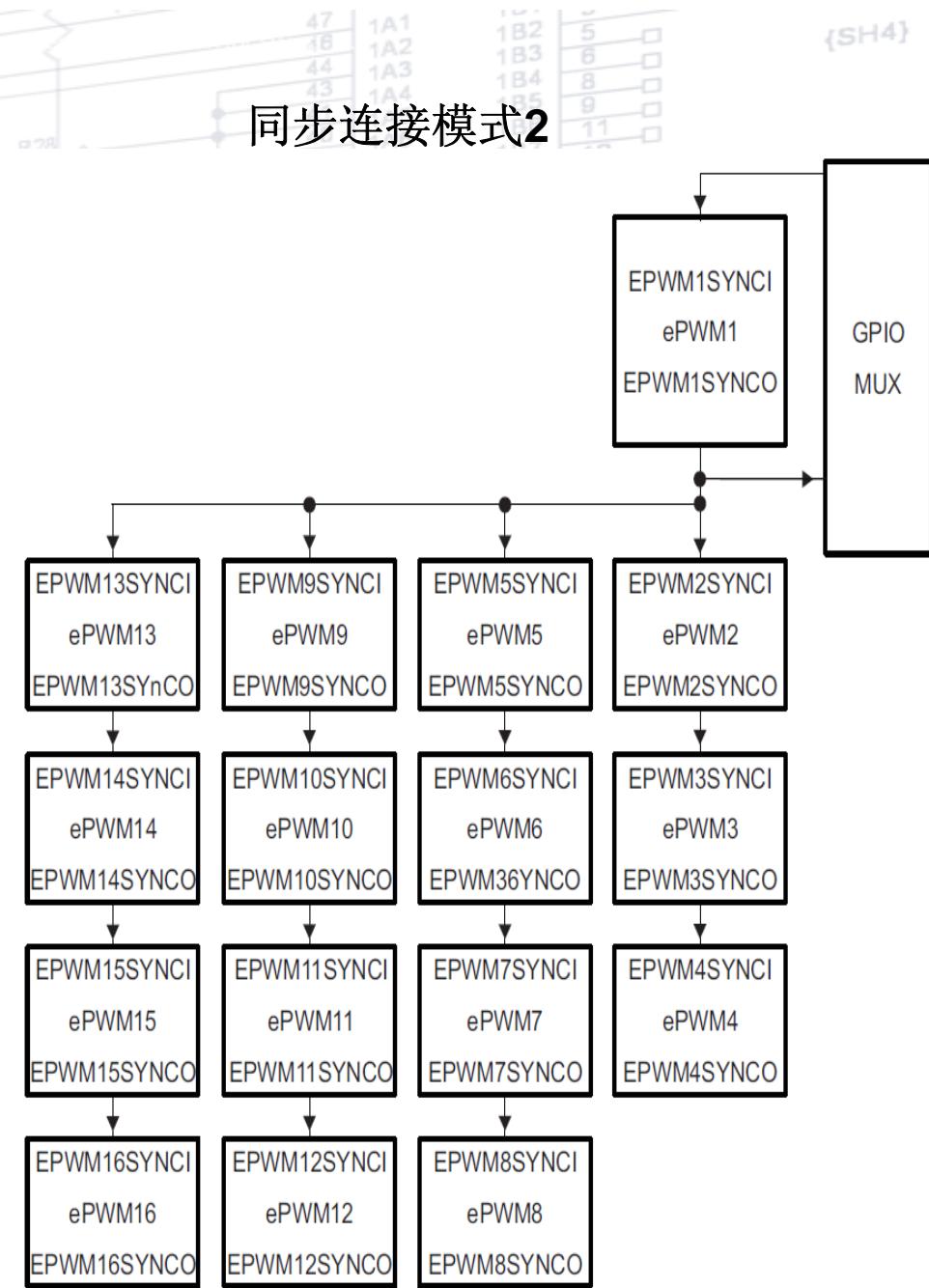




同步连接模式1



同步连接模式2



§ 7.1.5 多个ePWM模块时基时钟锁相

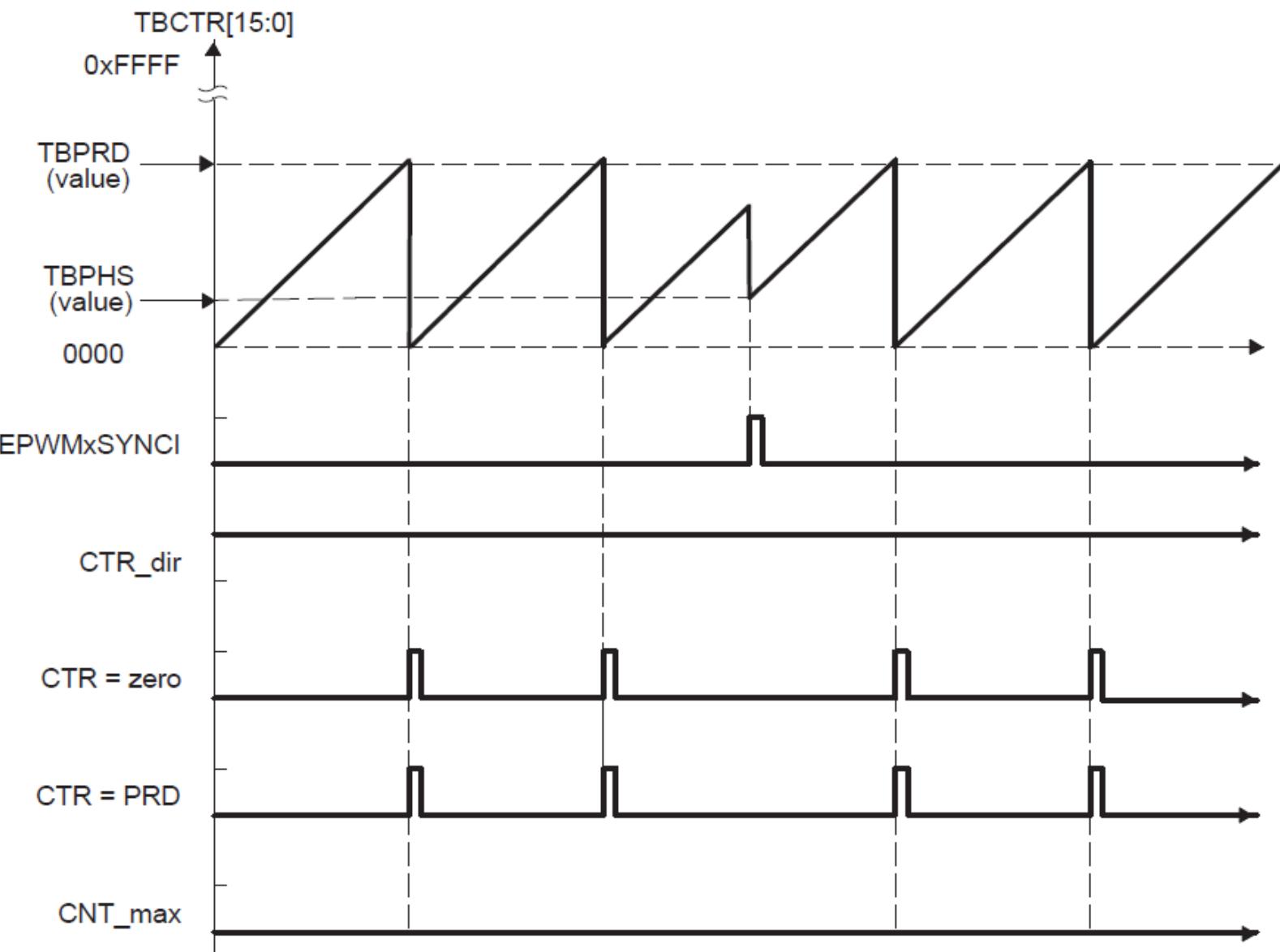
TBCLKSYNC位可以用于全局同步所有ePWM模块的时基时钟。当**TBCLKSYNC = 0**时,所有的ePWM模块时基时钟停止(默认状态)。当**TBCLKSYNC = 1**时,在**TBCLK**信号的上升沿所有的ePWM时基时钟模块开始。

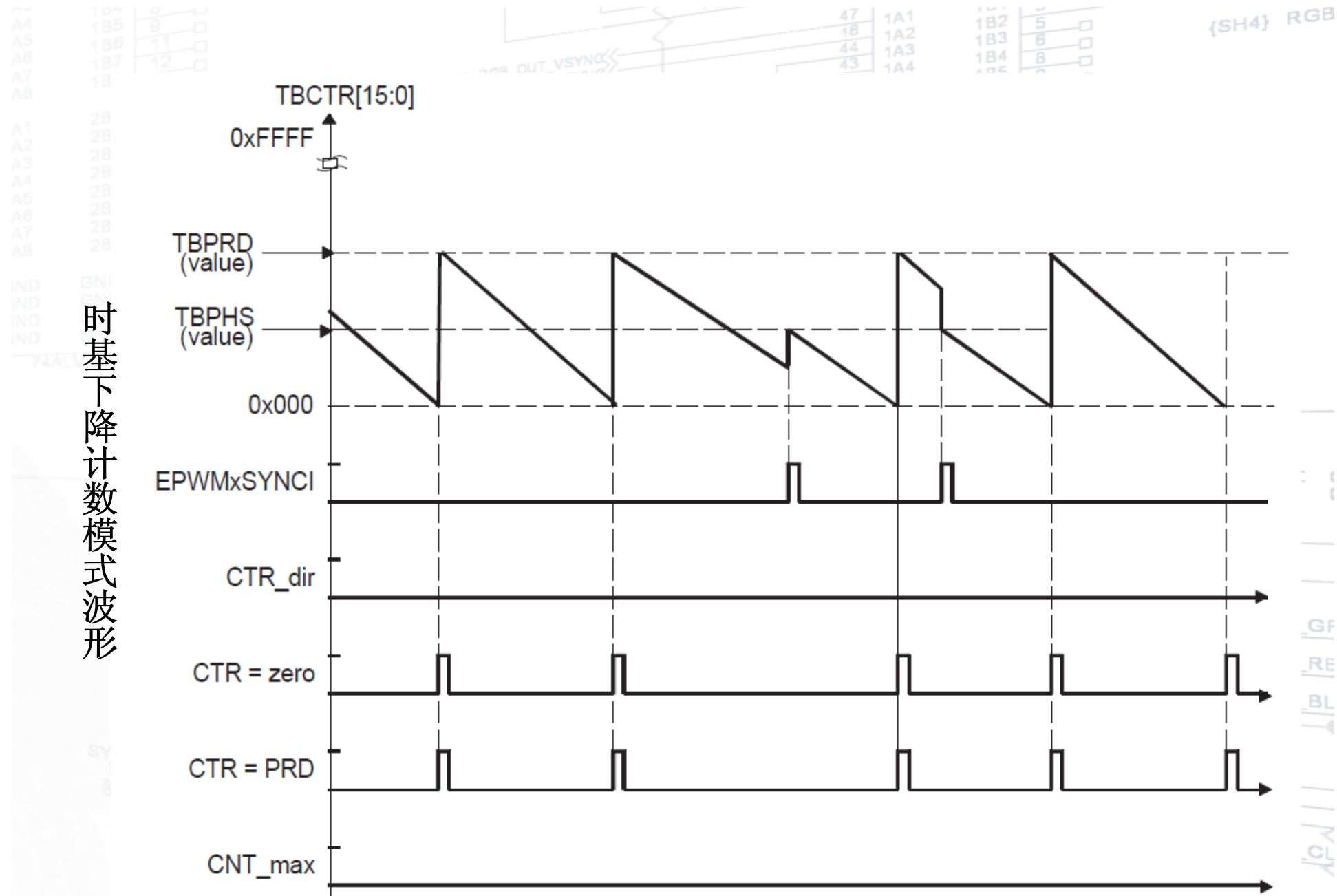
为了精确同步**TBCLK**, **TBCTL**的比例因子位必须设置相同。正确的ePWM时钟使能过程如下:

1. 分别使能各个ePWM模块时钟。
2. 设置**TBCLKSYNC = 0**。停止所有的ePWM模块的时基。
3. 配置比例因子值(**prescaler**)和期望的ePWM模块。
4. 设置**TBCLKSYNC = 1**。

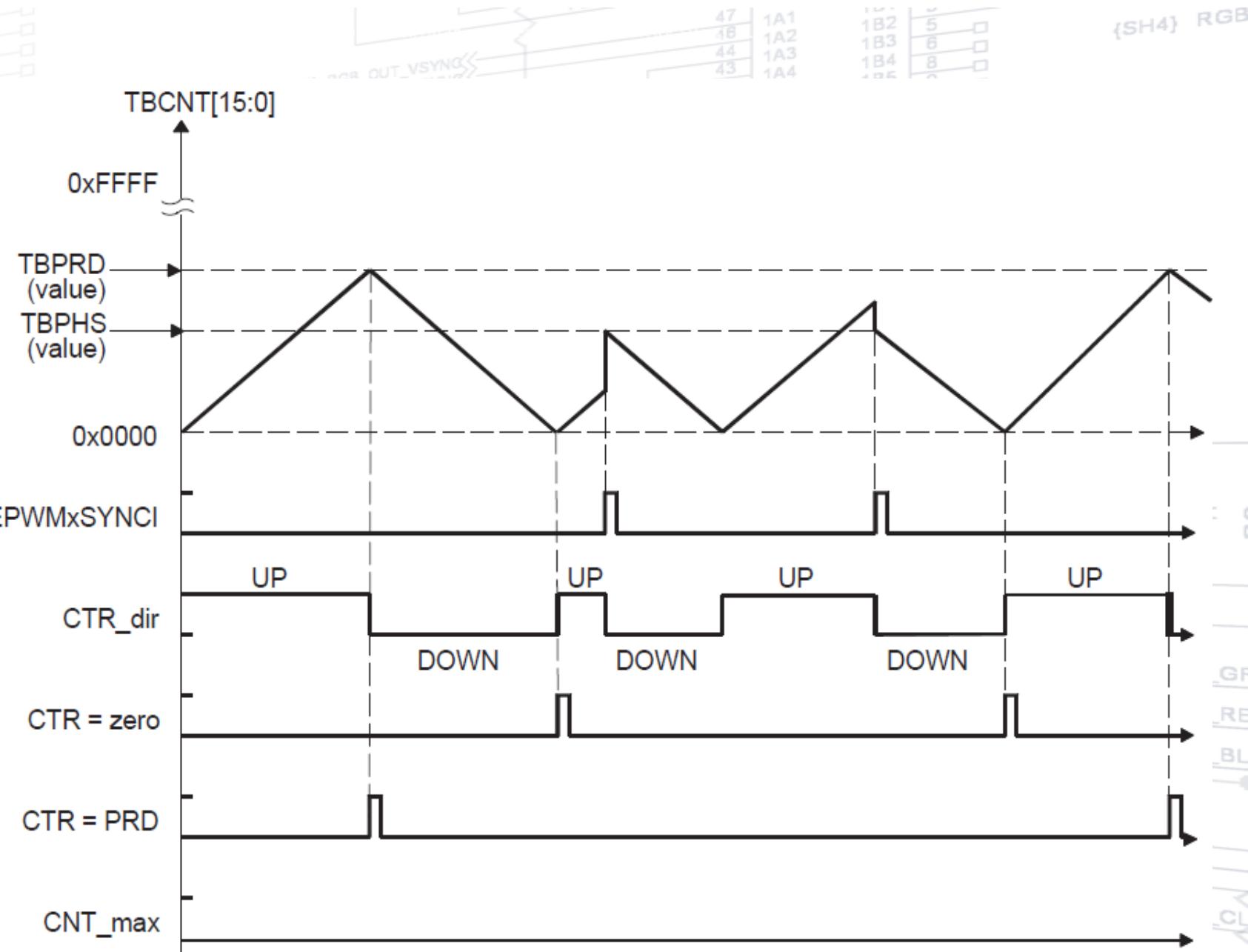


时基上升计数模式波形

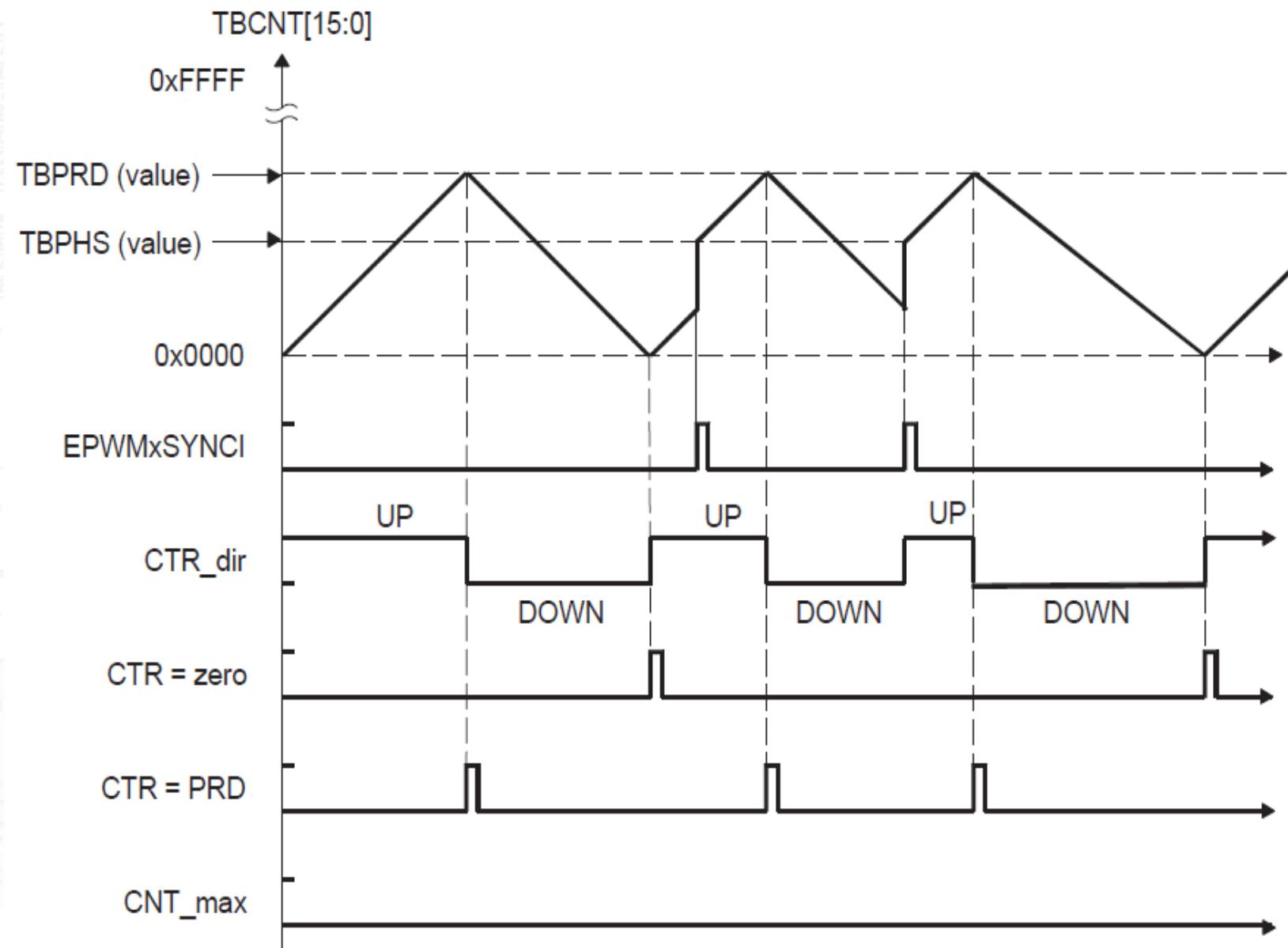




时基增减计数模式, TBCTL[PHSDIR = 0] 减计数同步事件



时基增减计数, TBCTL[PHSDIR = 1] 在同步事件到达时增计数



§ 7.1.6 计数器比较子模块

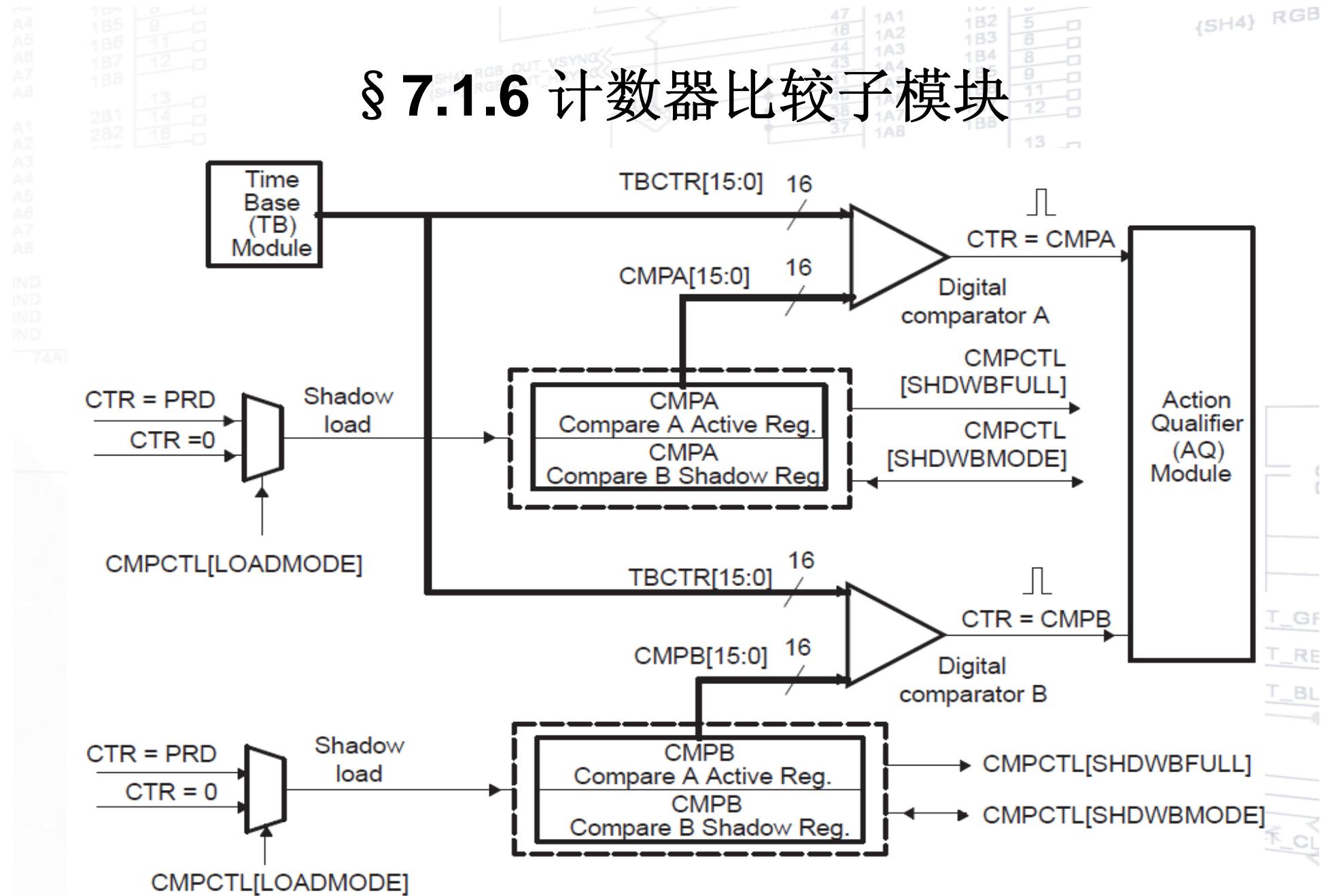


Table 2-5. Counter-Compare Submodule Key Signals

Signal	Description of Event	Registers Compared
CTR = CMPA	Time-base counter equal to the active counter-compare A value	TBCTR = CMPA
CTR = CMPB	Time-base counter equal to the active counter-compare B value	TBCTR = CMPB
CTR = PRD	Time-base counter equal to the active period. Used to load active counter-compare A and B registers from the shadow register	TBCTR = TBPRD
CTR = ZERO	Time-base counter equal to zero. Used to load active counter-compare A and B registers from the shadow register	TBCTR = 0x0000

计数器比较操作说明：

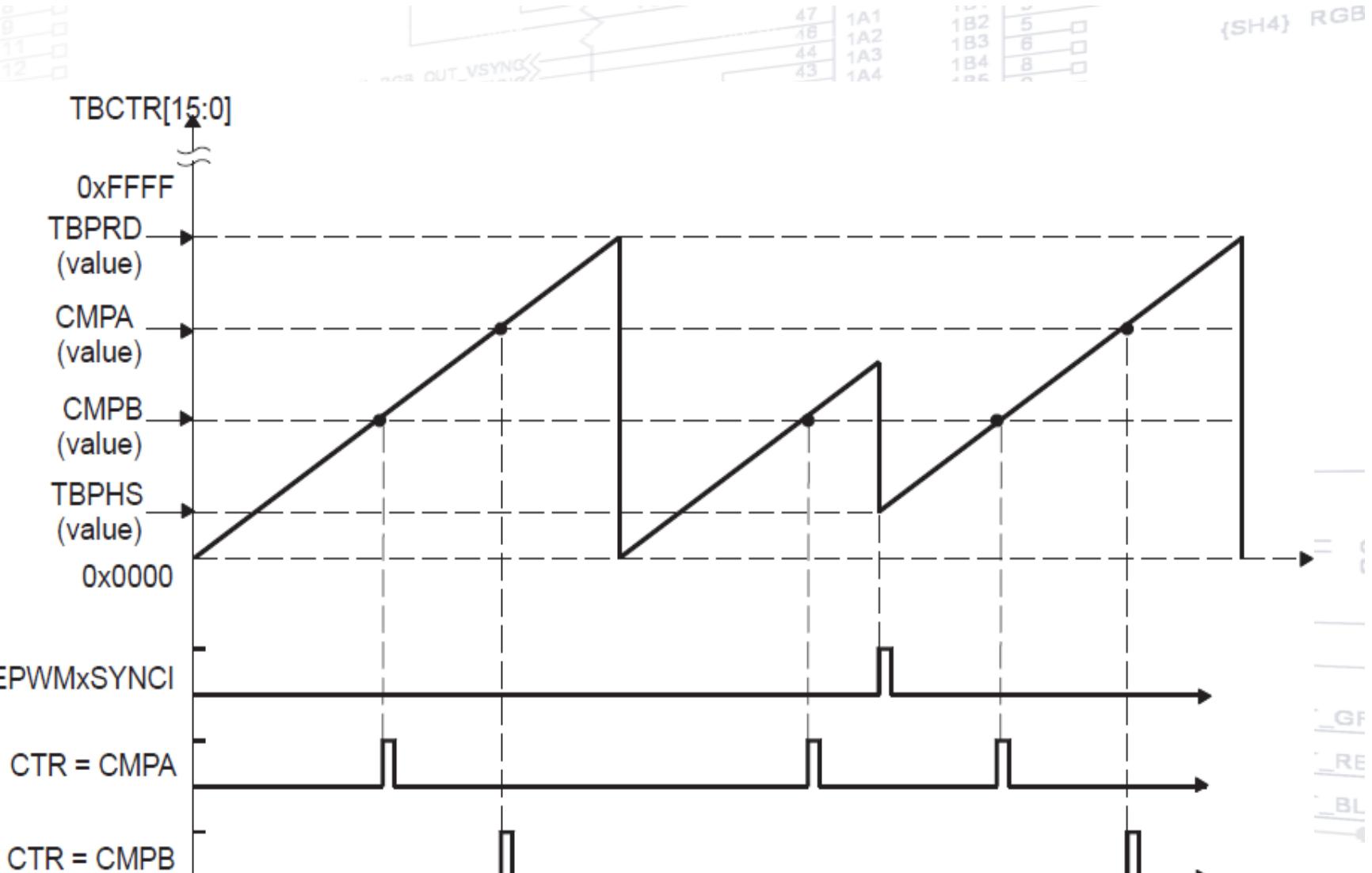
计数比较子模块用于产生两个独立的比较事件基或两个比较寄存器

1. **CTR=CMPA:** 时基计数器等于计数比较A寄存器 (**TBCTR=CMPA**)
2. **CTR=CMPB:** 时基计数器等于计数比较B寄存器 (**TBCTR=CMPB**)

对于增计数或减计数模式，每个周期每个事件仅发生一次。对于增减模式，如果比较值位于**0—TBPRD**之间，每个周期每个事件发生两次。



增计数模式下的事件比较波形



NOTE: An EPWMxSYNCl external synchronization event can cause a discontinuity in the TBCTR count sequence. This can lead to a compare event being skipped. This skipping is considered normal operation and must be taken into account.



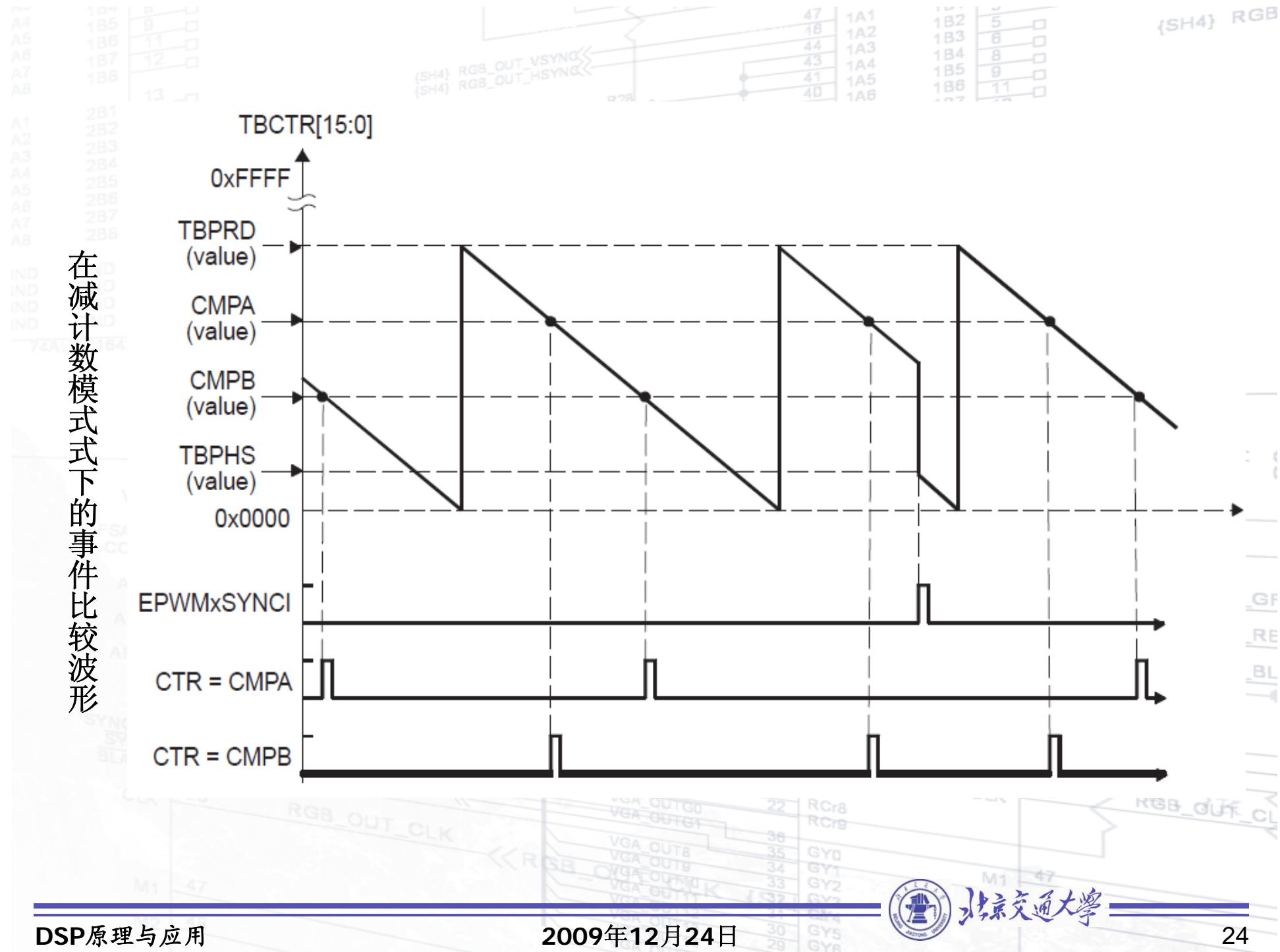


Figure 2-14. Counter-Compare Events In Up-Down-Count Mode, TBCTL[PHSDIR = 0] Count Down On Synchronization Event

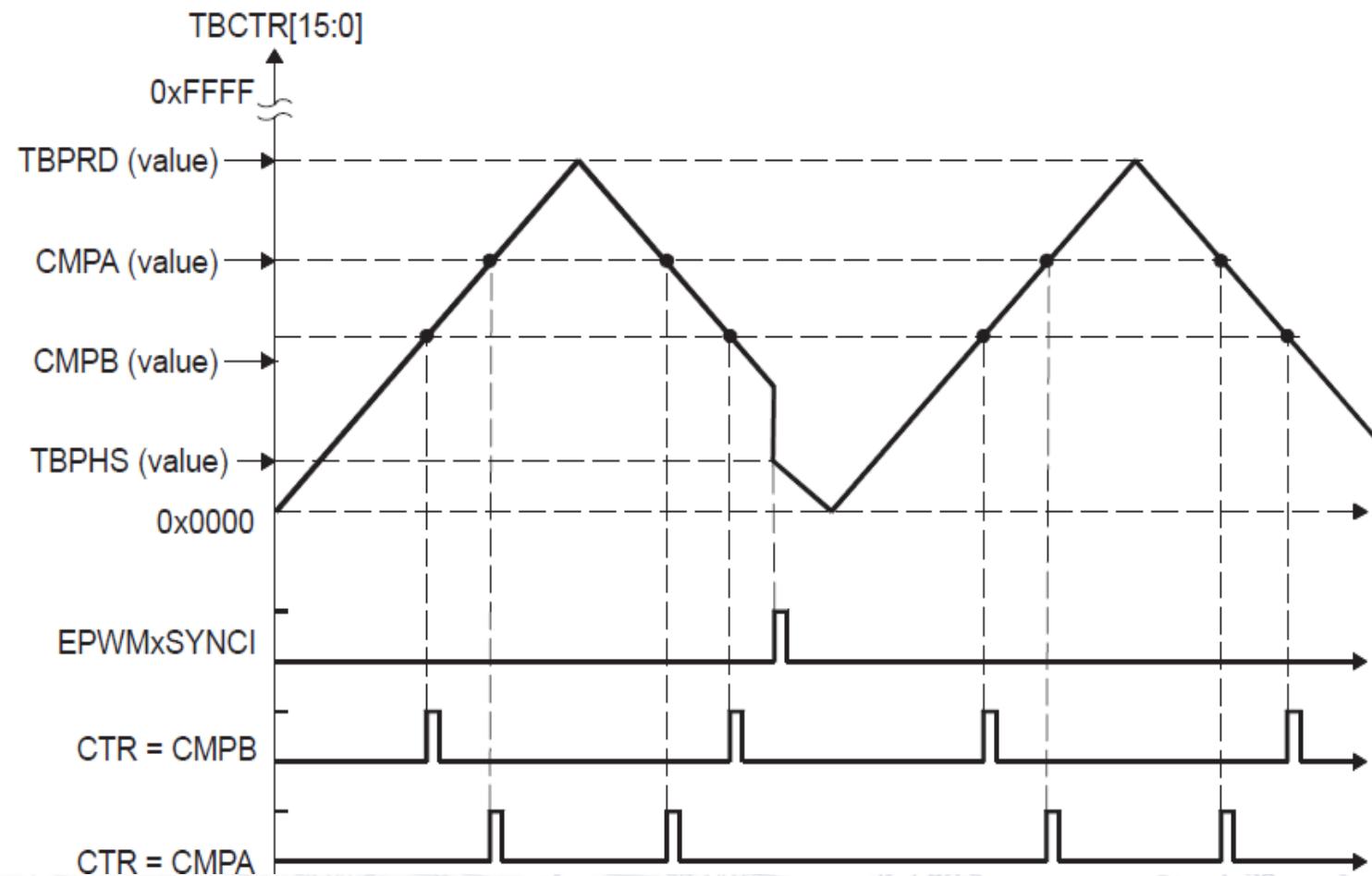
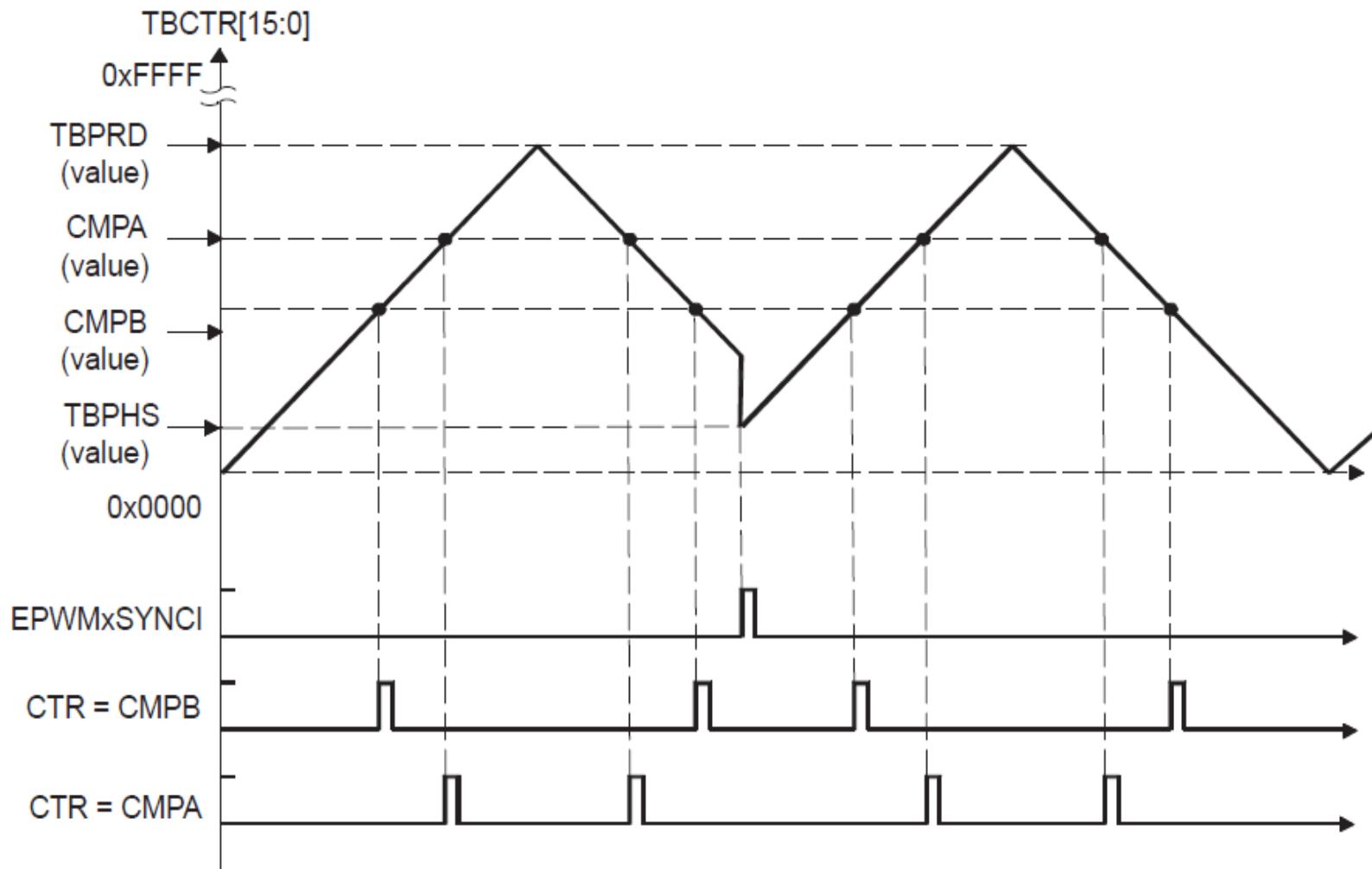


Figure 2-15. Counter-Compare Events In Up-Down-Count Mode, TBCTL[PHSDIR = 1] Count Up On Synchronization Event



§ 7.1.7 动作限定子模块

动作限定子模块在波形构造过程中和PWM产生中具有重要作用。

它决定哪个事件转换成各种动作类型，从而在EPWMxA 和 EPWMxB输出要求的波形。

动作限定子模块具有以下作用：

(1) 限定和产生动作（置位、清除、反转）：

- **CTR = PRD**: 时基计数器等于周期 ($TBCTR = TBPRD$).
- **CTR = Zero**: 时基计数器等于零 ($TBCTR = 0x0000$)
- **CTR = CMPA**: 时基计数器等于比较计数器A ($TBCTR = CMPA$)
- **CTR = CMPB**: 时基计数器等于比较计数器B ($TBCTR = CMPB$)

(2) 当这些事件同时发生时，管理优先级。

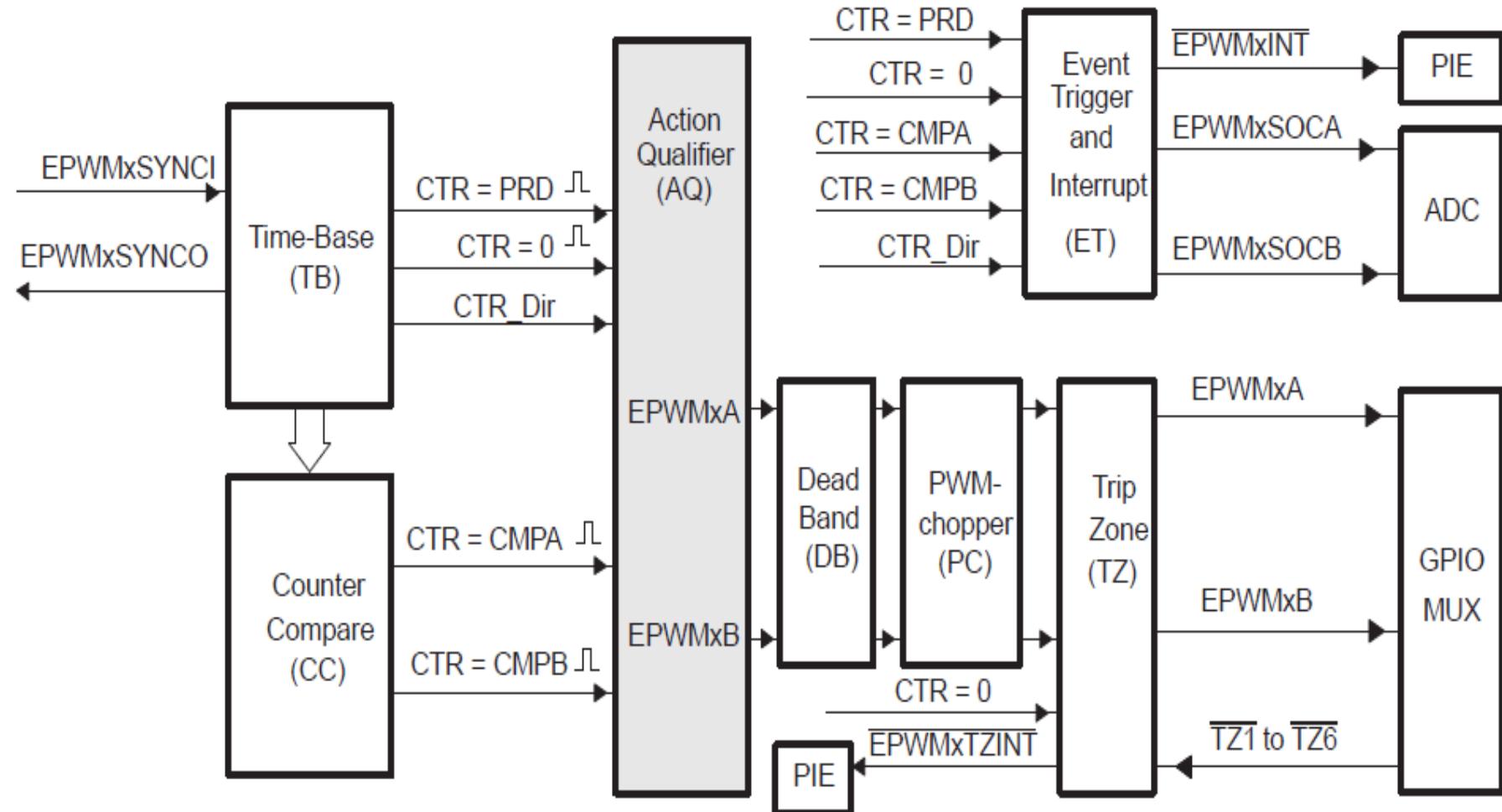
(3) 当时基计数器增计数和减计数时提供独立的事件控制。





动作控制子模块框图

Figure 2-16. Action-Qualifier Submodule



EPWM的几种可能输出模式

Figure 2-18. Possible Action-Qualifier Actions for EPWMxA and EPWMxB Outputs

S/W force	TB Counter equals:				Actions
	Zero	Comp A	Comp B	Period	
					Do Nothing
					Clear Low
					Set High
					Toggle



1P7
A4
A5
A6
A7
A8

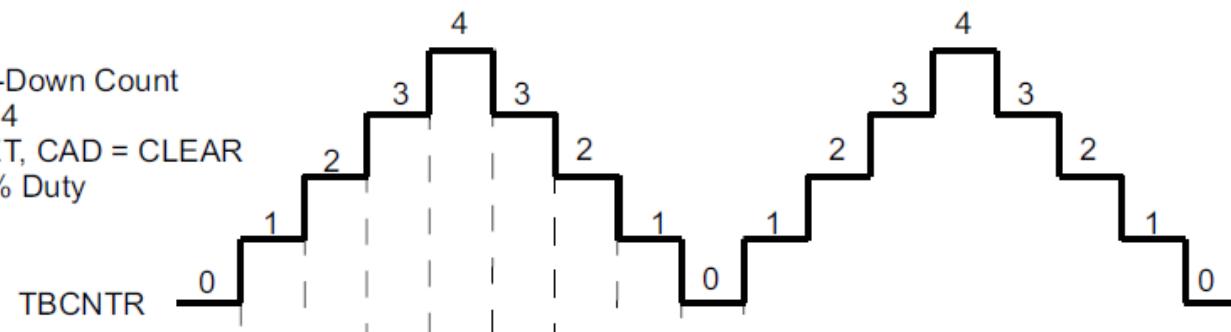
47
1A1
1B2
5

{SH4} RGB

Figure 2-19. Up-Down-Count Mode Symmetrical Waveform

A1
A2
A3
A4
A5
A6
A7
A8

Mode: Up-Down Count
TBPRD = 4
CAU = SET, CAD = CLEAR
0% - 100% Duty



TBCNTR Direction

Case 1:
CMPA = 4, 0% Duty

Case 2:
CMPA = 3, 25% Duty

Case 3:
CMPA = 2, 50% Duty

Case 3:
CMPA = 1, 75% Duty

Case 4:
CMPA = 0, 100% Duty

EPWMxA/EPWMxB

EPWMxA/EPWMxB

EPWMxA/EPWMxB

EPWMxA/EPWMxB

EPWMxA/EPWMxB

Figure 2-20. Up, Single Edge Asymmetric Waveform, With Independent Modulation on EPWMxA and EPWMxB—Active High

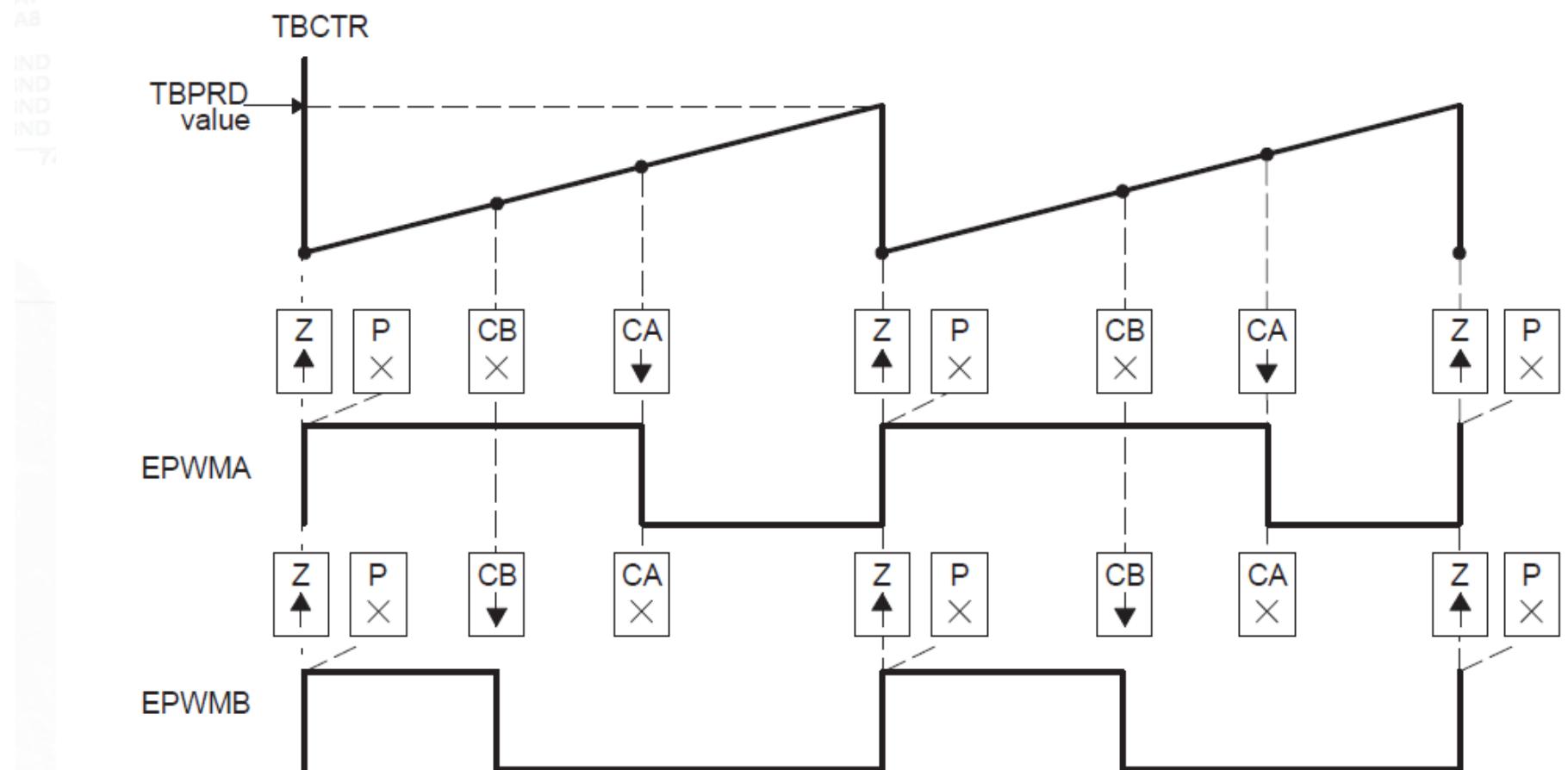


Figure 2-21. Up, Single Edge Asymmetric Waveform With Independent Modulation on EPWMxA and EPWMxB—Active Low

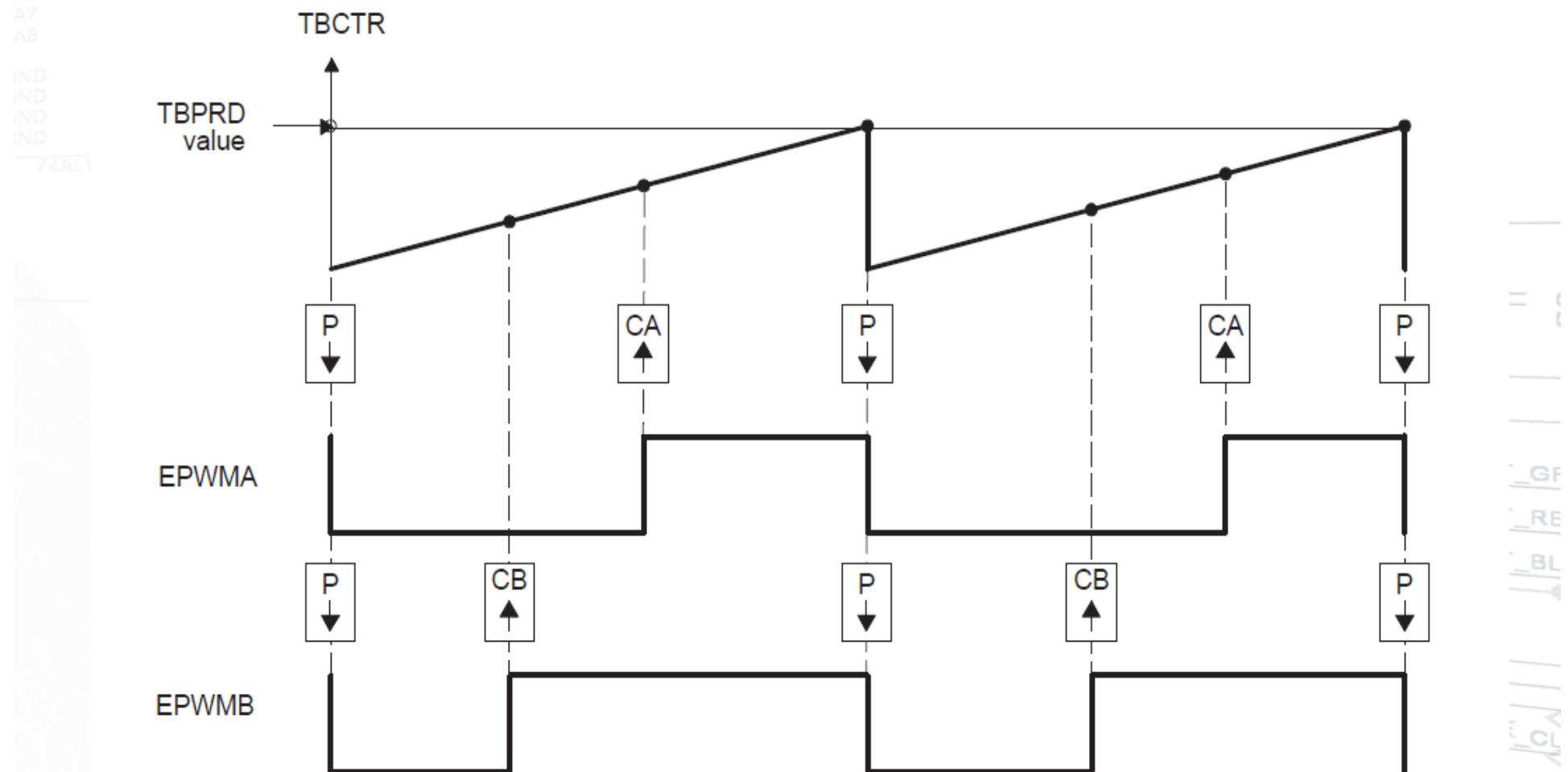
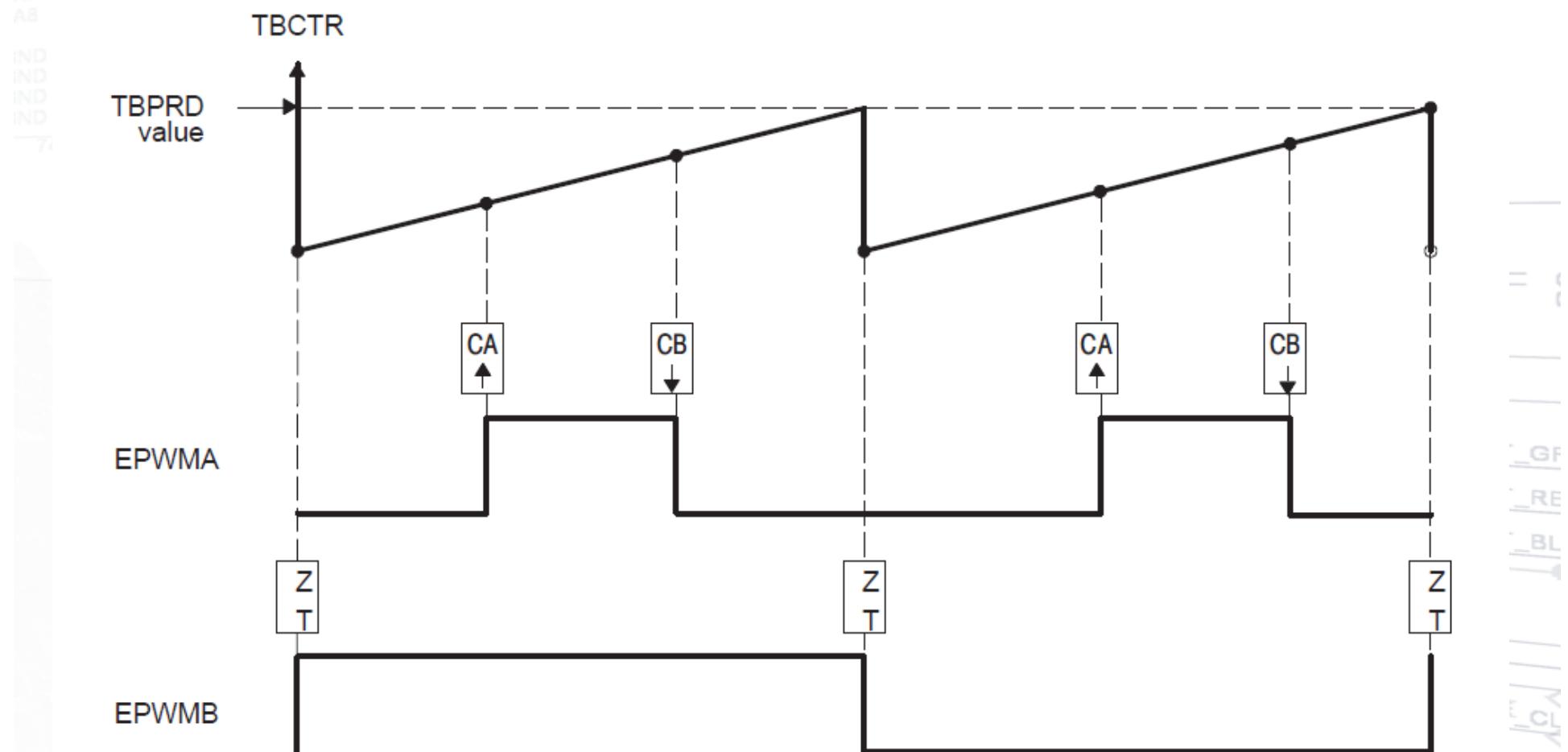


Figure 2-22. Up-Count, Pulse Placement Asymmetric Waveform With Independent Modulation on EPWMxA



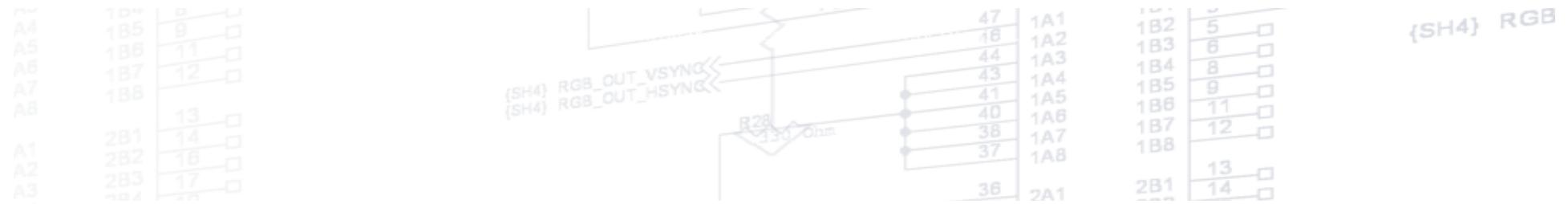
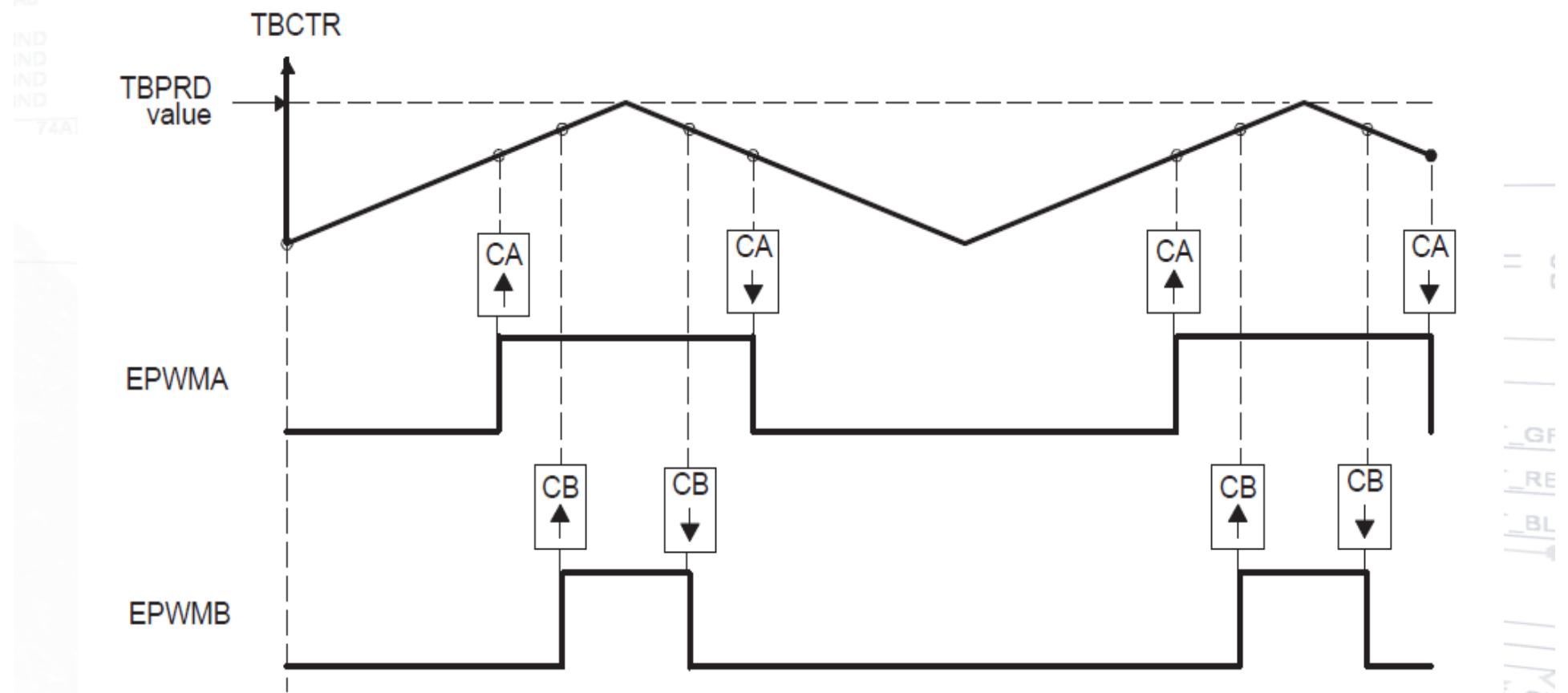


Figure 2-23. Up-Down-Count, Dual Edge Symmetric Waveform, With Independent Modulation on EPWMxA and EPWMxB—Active Low



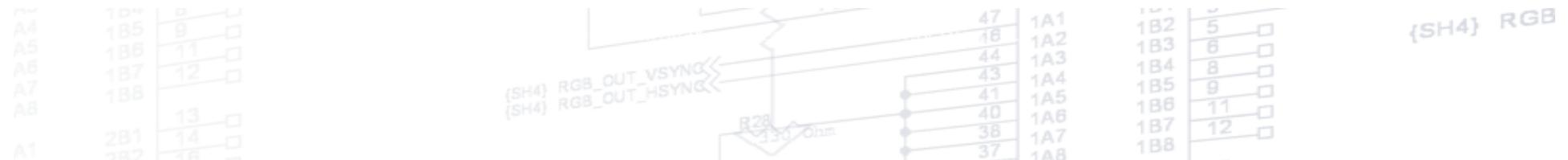
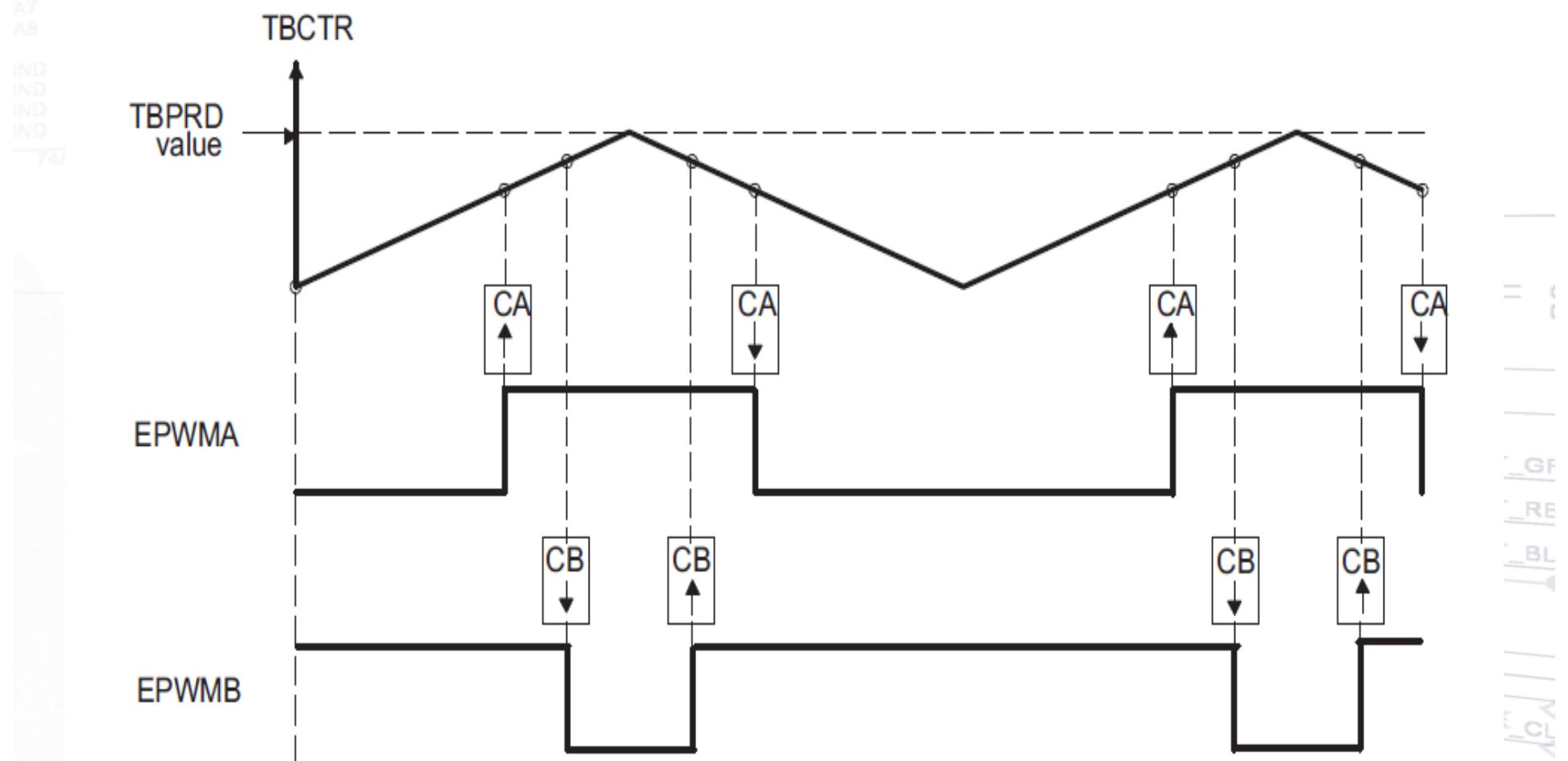


Figure 2-24. Up-Down-Count, Dual Edge Symmetric Waveform, With Independent Modulation on EPWMxA and EPWMxB—Complementary



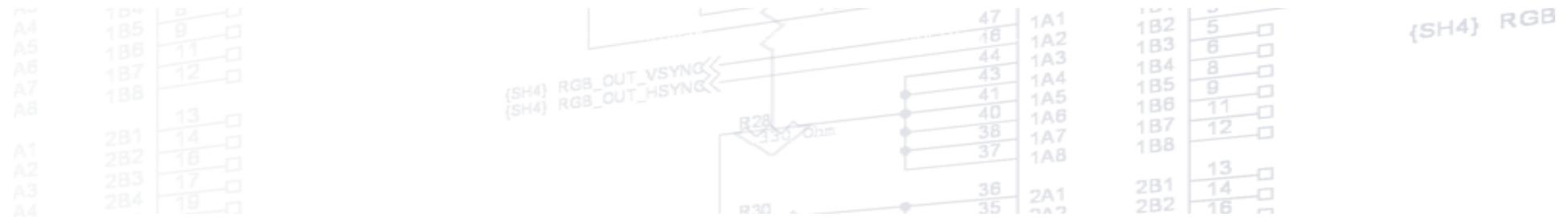
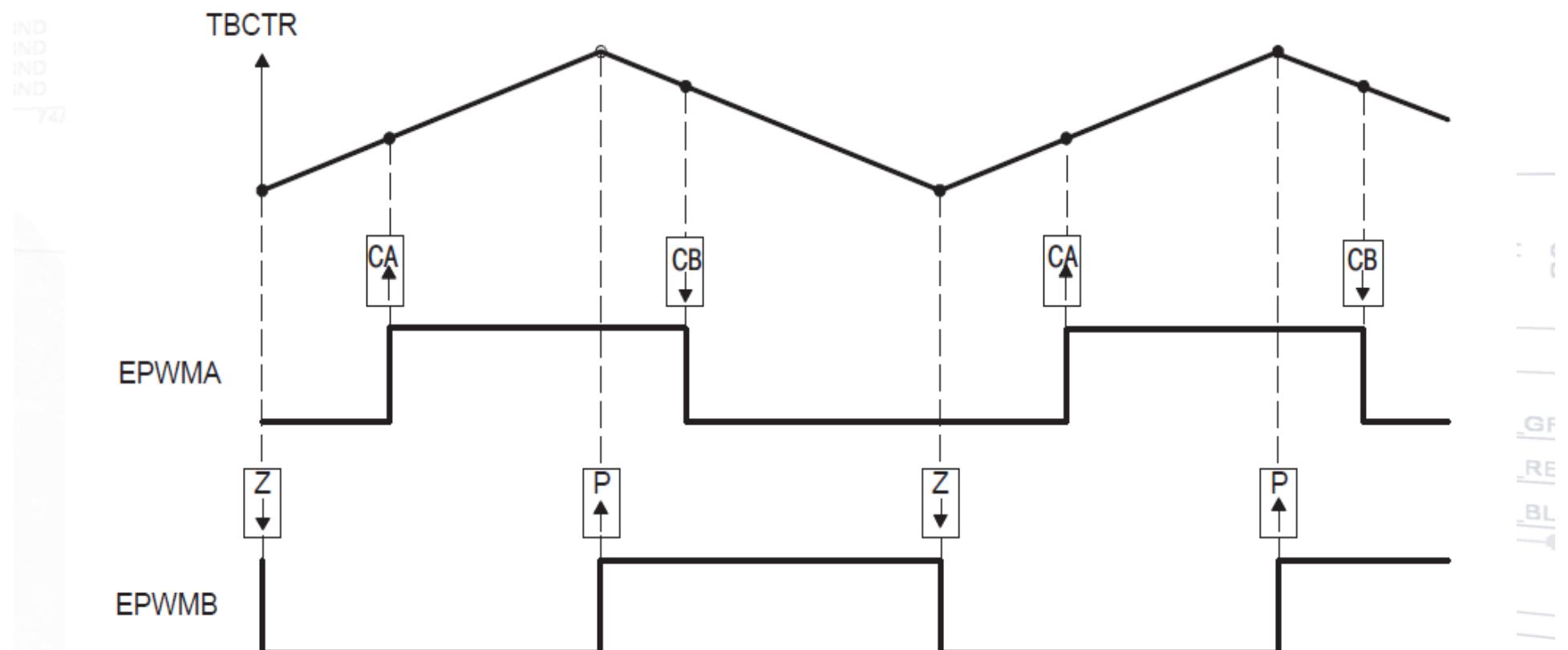


Figure 2-25. Up-Down-Count, Dual Edge Asymmetric Waveform, With Independent Modulation on EPWMxA—Active Low



§ 7.1.8 死区产生子模块

死区子模块有两组独立的选项设置

输入源选择 (Input Source Selection) :

死区模块的输入信号是来自动作控制的输出信号EPWMxA和EPWMxB。使用DBCTL[IN_MODE]控制位可以选择每个延时的信号源，上升沿或下降沿：

- EPWMxA 该信号源上升沿和下降沿延时，这种模式是默认模式。
- EPWMxA 该信号源下降沿延时，EPWMxB 在上升沿延时
- EPWMxA 在上升沿延时，EPWMxB 在下降沿延时
- EPWMxB 上升沿和下降沿延时

输出模式控制 (Output Mode Control) :

输出模式由DBCTL[OUT_MODE]位决定.这些位决定是下降沿延时，上升沿延时，都不延时或者都延时。

极性控制 (Polarity Control) :

极性控制(DBCTL[POLSEL])允许我们指定是上升沿延时信号或和下降沿延时信号在送出死区子模块之前是否取反。



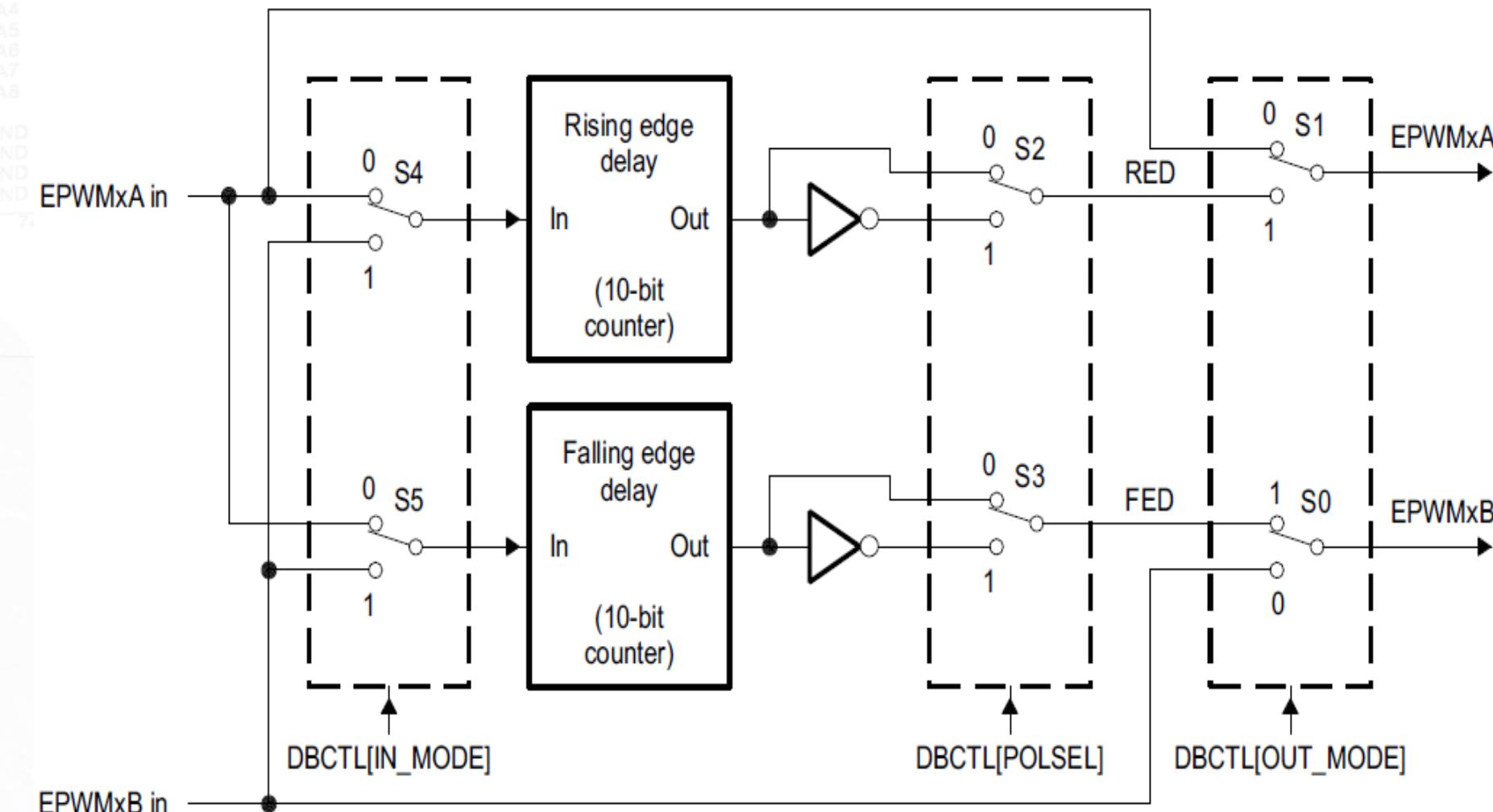
	107	U
A4	185	0
A5	186	11
A6	187	12
A7	188	
A8	13	
2B1	14	



{SH4} RGB

死区子模块的配置

Figure 2-27. Configuration Options for the Dead-Band Submodule





{SH4} RGB

Table 2-13. Classical Dead-Band Operating Modes

Mode	Mode Description ⁽¹⁾	DBCTL[POLSEL]		DBCTL[OUT_MODE]	
		S3	S2	S1	S0
1	EPWMxA and EPWMxB Passed Through (No Delay)	X	X	0	0
2	Active High Complementary (AHC)	1	0	1	1
3	Active Low Complementary (ALC)	0	1	1	1
4	Active High (AH)	0	0	1	1
5	Active Low (AL)	1	1	1	1
6	EPWMxA Out = EPWMxA In (No Delay)	0 or 1	0 or 1	0	1
	EPWMxB Out = EPWMxA In with Falling Edge Delay				
7	EPWMxA Out = EPWMxA In with Rising Edge Delay	0 or 1	0 or 1	1	0
	EPWMxB Out = EPWMxB In with No Delay				

(1) These are classical dead-band modes and assume that DBCTL[IN_MODE] = 0,0. That is, EPWMxA in is the source for both the falling-edge and rising-edge delays. Enhanced, non-traditional modes can be achieved by changing the IN_MODE configuration.

Mode 1: 旁路上下降沿和上升沿
不使用死区功能

Mode 2-5: 经典死区极性设置 **Dead-Band Polarity Settings:**

Mode 6: 旁路上升沿延时 **Bypass rising-edge-delay**

Mode 7: 旁路下降沿延时 **Bypass falling-edge-delay**



	107	
A4	185	
A5	9	
A6	186	11
A7	187	12
A8	188	
	13	
A1	281	14
A2	282	16
A3	283	17
A4	284	19
A5	285	20
A6	286	22
A7	287	23
A8	288	
IND	45	
IND	GND	39
IND	GND	34
IND	GND	28
	74ALVC164245	

Figure 2-28. Dead-Band Waveforms for Typical Cases ($0\% < \text{Duty} < 100\%$)

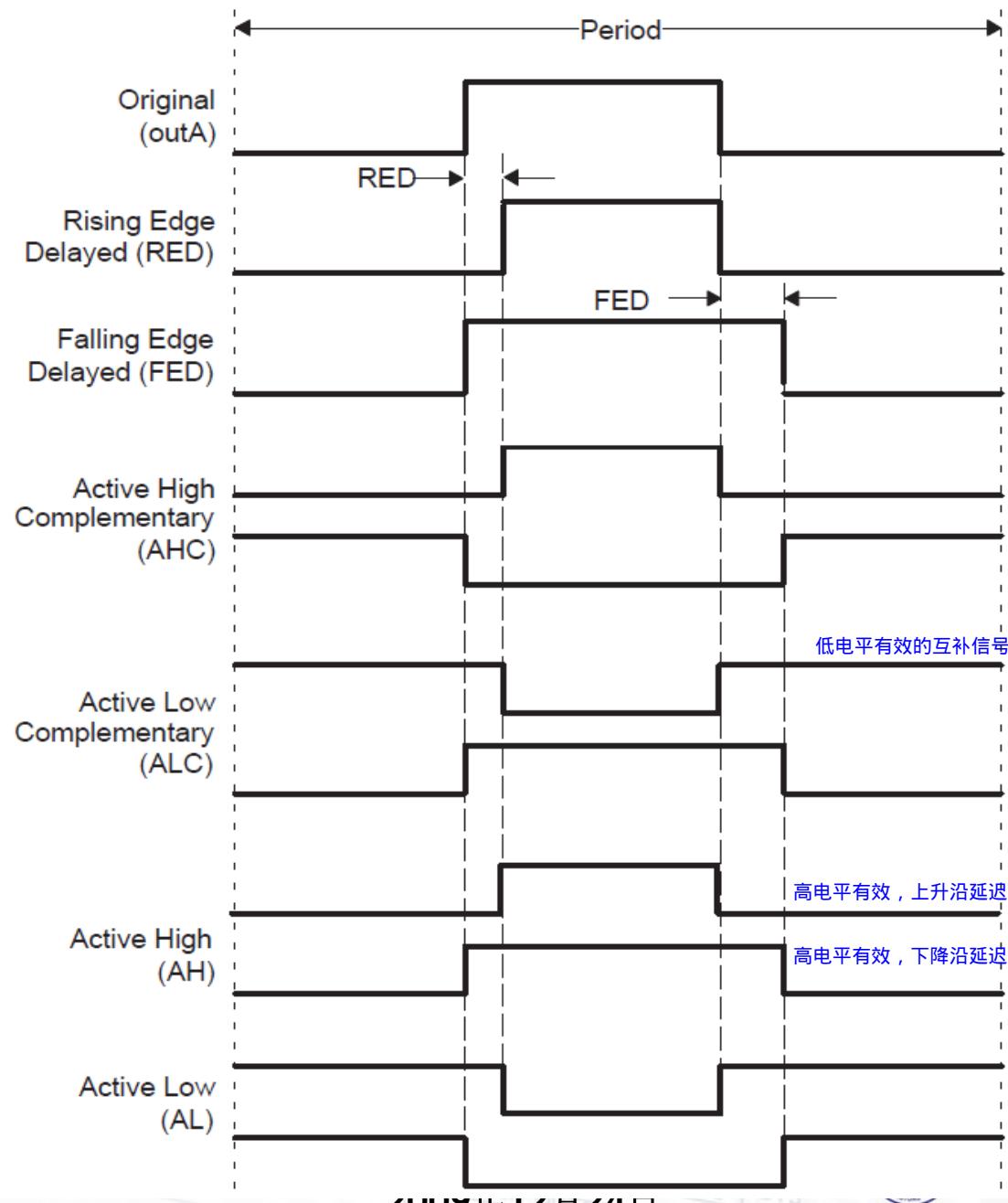


Table 2-14. Dead-Band Delay Values in μ S as a Function of DBFED and DBRED

Dead-Band Value DBFED, DBRED	Dead-Band Delay in μ S (1)		
	TBCLK = SYSCLKOUT/1	TBCLK = SYSCLKOUT /2	TBCLK = SYSCLKOUT/4
1	0.01 μ S	0.02 μ S	0.04 μ S
5	0.05 μ S	0.10 μ S	0.20 μ S
10	0.10 μ S	0.20 μ S	0.40 μ S
100	1.00 μ S	2.00 μ S	4.00 μ S
200	2.00 μ S	4.00 μ S	8.00 μ S
300	3.00 μ S	6.00 μ S	12.00 μ S
400	4.00 μ S	8.00 μ S	16.00 μ S
500	5.00 μ S	10.00 μ S	20.00 μ S
600	6.00 μ S	12.00 μ S	24.00 μ S
700	7.00 μ S	14.00 μ S	28.00 μ S
800	8.00 μ S	16.00 μ S	32.00 μ S
900	9.00 μ S	18.00 μ S	36.00 μ S
1000	10.00 μ S	20.00 μ S	40.00 μ S

死区子模块支持独立上升延沿延时(**RED**)和下降沿延时(**FED**)。延时时间通过**DBRED**和 **DBFED** 寄存器设置。这些是10位寄存器，它们的值代表延时的时基时钟**TBCLK**周期数。升沿延时和下降沿延时计算如下：

$$FED = DBFED \times T_{TBCLK}$$

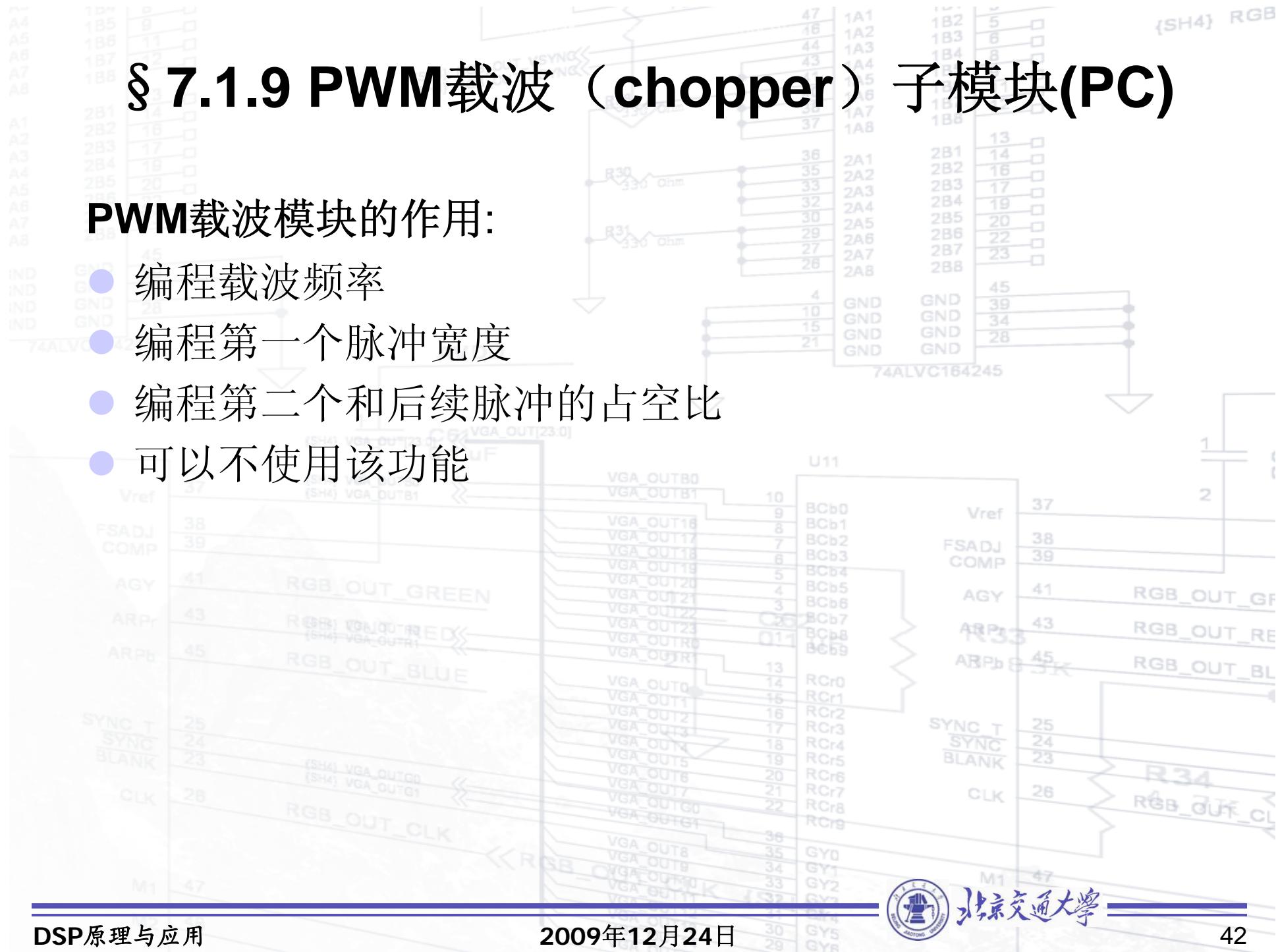
$$RED = DBRED \times T_{TBCLK}$$



§ 7.1.9 PWM载波 (chopper) 子模块(PC)

PWM载波模块的作用:

- 编程载波频率
- 编程第一个脉冲宽度
- 编程第二个和后续脉冲的占空比
- 可以不使用该功能



	107	U
A4	9	
A5	10	
A6	11	
A7	12	
	188	



{SH4} RGB

Figure 2-30. PWM-Chopper Submodule Operational Details

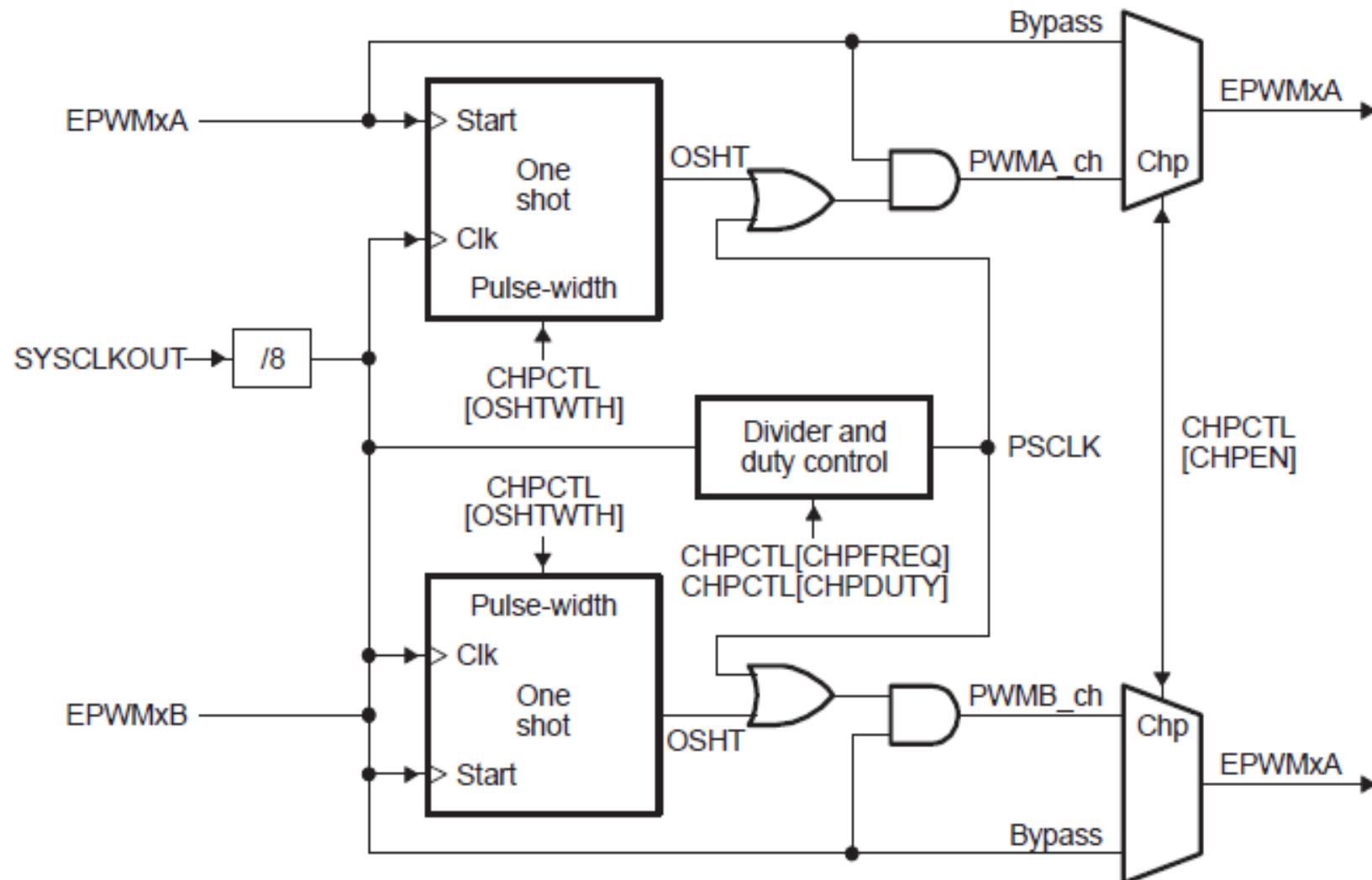


Figure 2-31. Simple PWM-Chopper Submodule Waveforms Showing Chopping Action Only

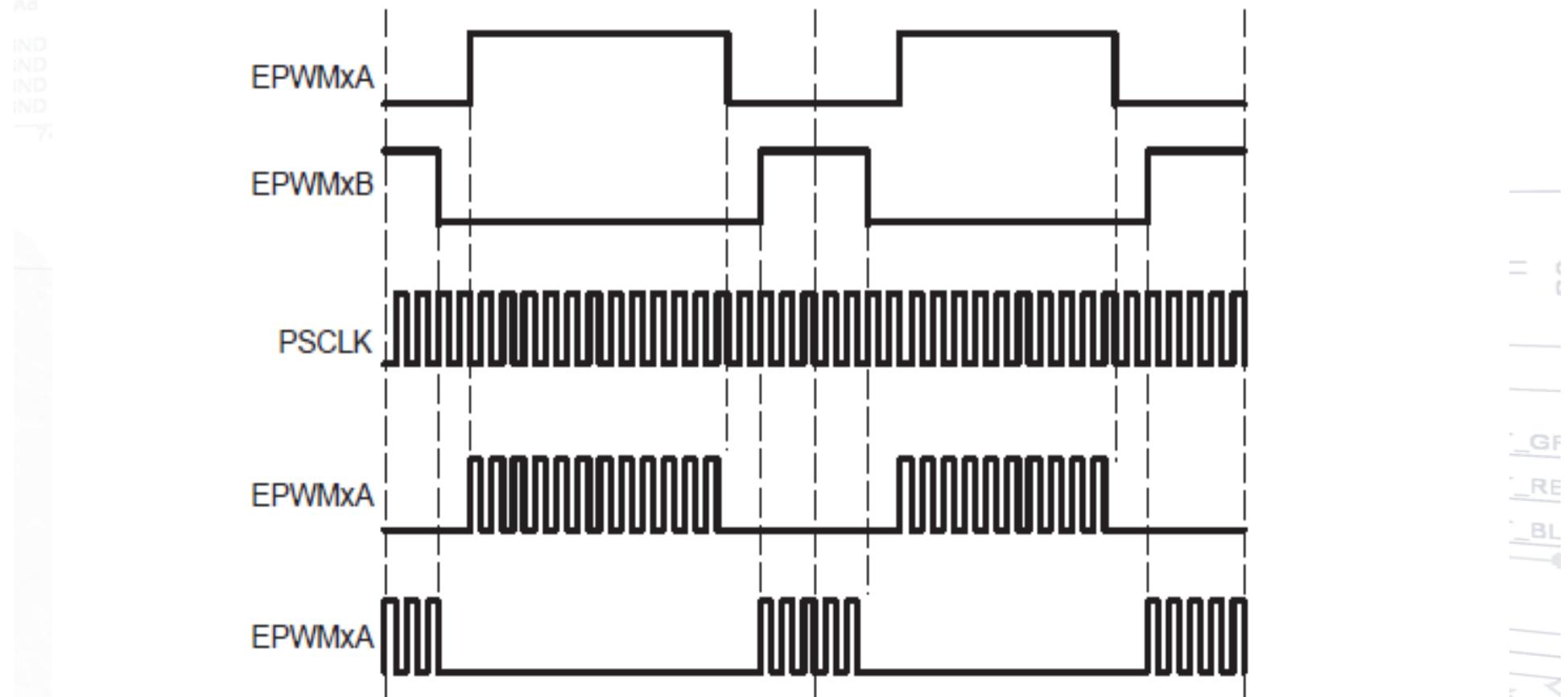
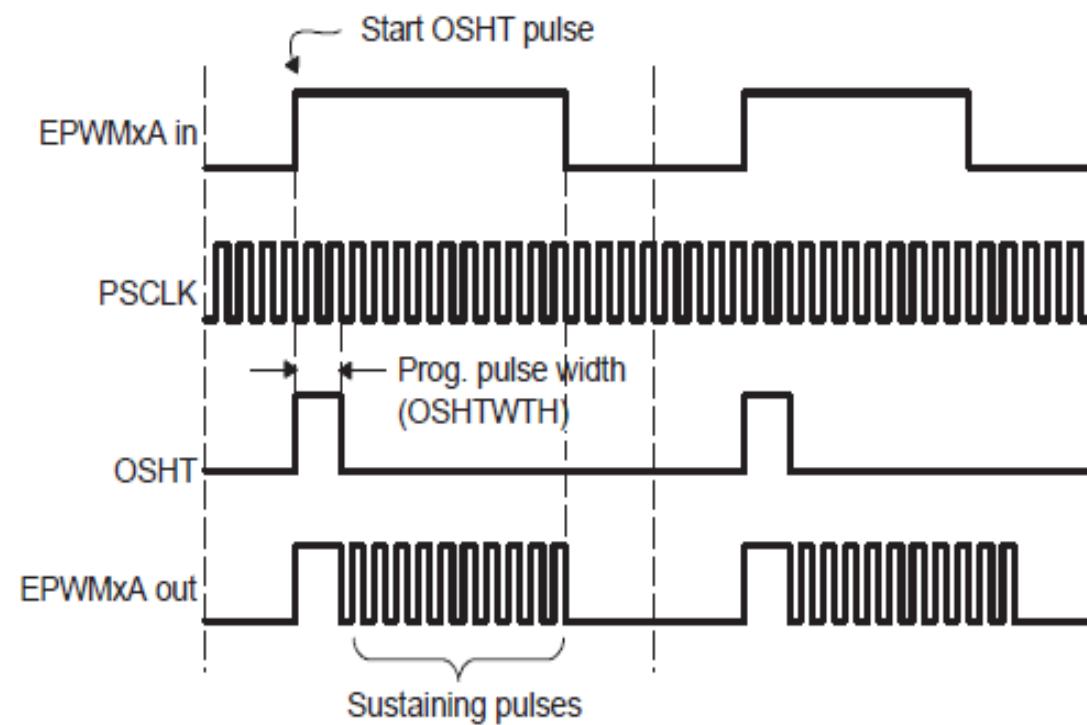


Figure 2-32. PWM-Chopper Submodule Waveforms Showing the First Pulse and Subsequent Sustaining Pulses



第一个脉冲可以是16个可能的脉冲宽度，脉宽或周期如下：

$$T_{1\text{st} \text{pulse}} = T_{\text{SYSCLKOUT}} \times 8 \times \text{OSHTWTH}$$

TSYSCLKOUT是系统时钟 (**SYSCLKOUT**)；
OSHTWTH 是四个控制位，取值范围为1 ~ 16。

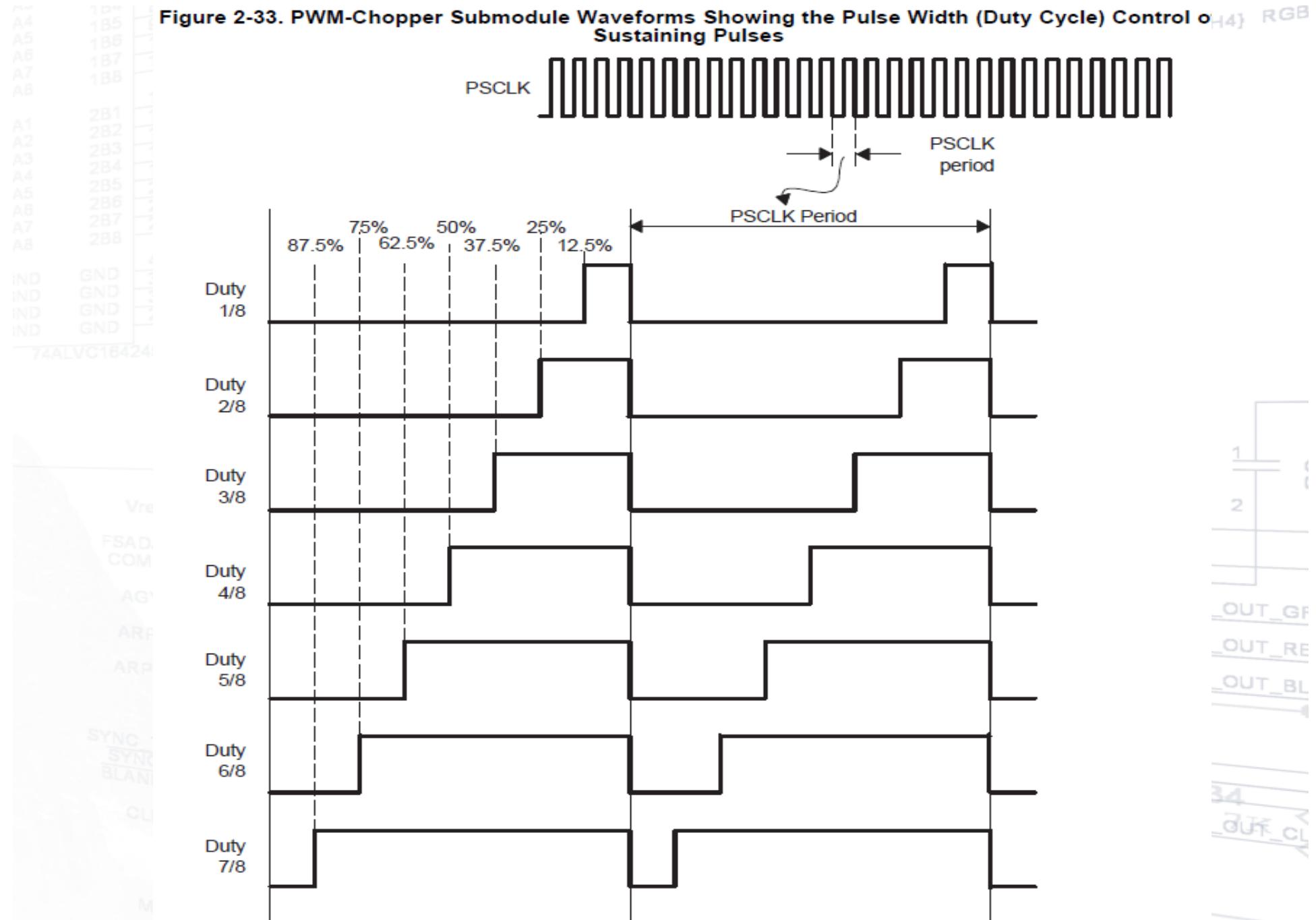


占空比控制

基于脉冲变压器的门极驱动设计需要掌握磁特性、变压器特性和有关的电路。饱和问题必须考虑。为了有助于门及驱动设计者，第二个和后续的脉冲占空比被设计为可编程，这些持续的脉冲在整个周期内确保正确驱动强度和极性施加在功率开关的门极，因此可编程占空比允许通过软件控制进行调谐和优化。

Figure 2-33给出通过**CHPDU** 位编程得到的可能占空比，可以选择七个可能的占空比（12.5% ~ 87.5%）

Figure 2-33. PWM-Chopper Submodule Waveforms Showing the Pulse Width (Duty Cycle) Control of Sustaining Pulses



§ 7.1.10 Trip-Zone (TZ) 子模块

Trip-Zone子模块的关键特性如下：

Trip 输入 **TZ1 to TZ6** 可以灵活编程映射到任意的 **ePWM** 模块；

一旦遇到故障条件输出 **EPWMxA** 和 **EPWMxB** 可被强制为如下几种情况：

- 高 (High)
- 低 (Low)
- 高阻态 (High-impedance)
- 无任何动作 (No action taken)

支持大多数短路或过流条件下的单次 (**one-shot**) 控制 **trip (OSHT)**；

支持当前操作的循环 (**cycle-by-cycle**) 控制 **tripping (CBC)**。

每个 **trip-zone** 输入都可分配为单次 **one-shot** 或 循环 **cycle-by-cycle** 操作

在任何 **trip-zone** 引脚都可以产生中断

支持软件的 **tripping**

如果不要求，则 **trip-zone** 子模块可以彻底旁路。



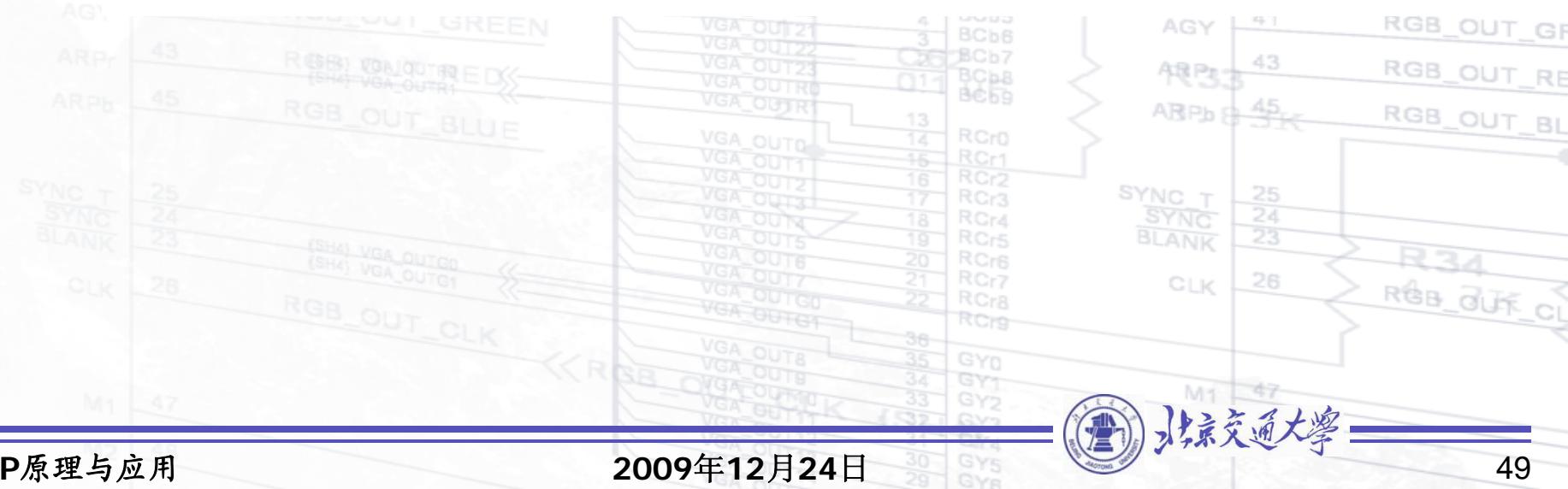
A4	107	8	U
A5	185	9	□
A6	186	11	□
A7	187	12	□
A8	188	13	□
A1	281	14	□
A2	282	16	□
A3	283	17	□
A4	284	19	□
A5	285	20	□
A6	286	21	□
A7	287	23	□
A8	288	24	□



{SH4} RGB

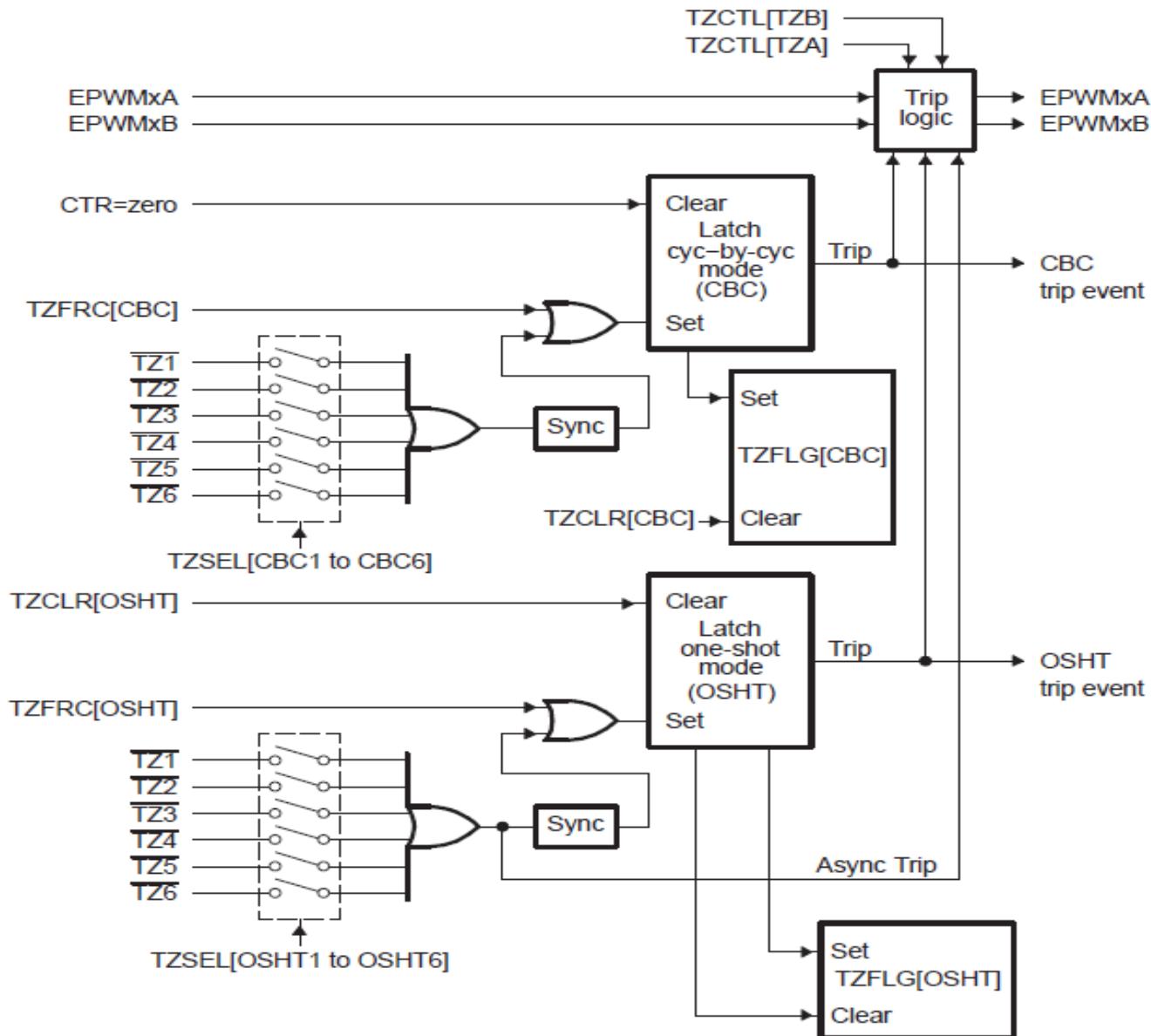
Table 2-18. Possible Actions On a Trip Event

IND	GND	TZCTL[TZA] and/or TZCTL[TZB]	EPWM xA and/or EPWMxB	Comment
IND	GND	0,0	High-Impedance	Tripped
IND	GND	0,1	Force to High State	Tripped
IND	GND	1,0	Force to Low State	Tripped
74ALVC16424	Vre	1,1	No Change	Do Nothing. No change is made to the output.



	107	0	U
A4	185	0	
A5	186	1	
A6	187	1	
A7	188	1	
A8		1	
	281	14	
A1	282	15	
A2	283	1	
A3	284	15	
A4	285	2	
A5	286	2	
A6	287	2	
A7	288	2	
A8		2	
IND	GND	35	
IND	GND	34	
IND	GND	21	
IND	GND	21	
	74ALVC164245	41	
Vref			
FSADJ			
COMP			
AGY			
ARP _r			
ARP _b			
SYNC_T			
SYNC_BLANK			
CLK			
M1			

Figure 2-35. Trip-Zone Submodule Mode Control Logic



Trip-Zone字模块操作说明

在 TZ1 到 TZ6 的信号低有效 (active low)。

当这些引脚变低时，表明一个trip事件已经发生，每个ePWM模块可以分别配置。哪个ePWM模块使用哪个trio-zone引脚由TZSEL寄存器决定。trip-zone信号可以与系统时钟同步也可以不同步，而且可以通过GPIO MUX模块进行数字滤波处理。在TZn的输入信号最小1个SYSCLKOUT低脉冲就可以触发ePWM模块的故障条件。异步trip确保由于其它原因时钟丢失，输出仍旧可以使在TZn 引脚上输入的信号触发 (tripped)。

每个ePWM模块的TZn输入可以单独配置提供周期循环 (cycle-by-cycle) 或单次 (one-shot) trip事件。配置由 TZSEL[CBCn] 和 TZSEL[OSHTn]控制位决定。



Cycle-by-Cycle (CBC):

当周期trip event时间发生时,在**TZCTL**寄存器中指定的动作立刻执行在**EPWMxA**和**EPWMxB**的输出。在周期trip event标志(**TZFLG[CBC]**)被设置时, 如果**TZEINT**和**PIE**外设使能, 将产生**EPWMx_TZINT**中断。当ePWM时基计数器达到零时(**TBCTR = 0x0000**)在引脚上指定的条件将自动清除, 如果trip 事件不再出现。因此在该模式下trip事件在每个PWM周期自动清除或复位。而**TZFLG[CBC]**标志位保持置位, 直到向**TZCLR[CBC]**位写手动清除。如果在**TZFLG[CBC]**位被清除时周期trip事件仍然出现, 它将再次立即被设置。

One-Shot (OSHT):

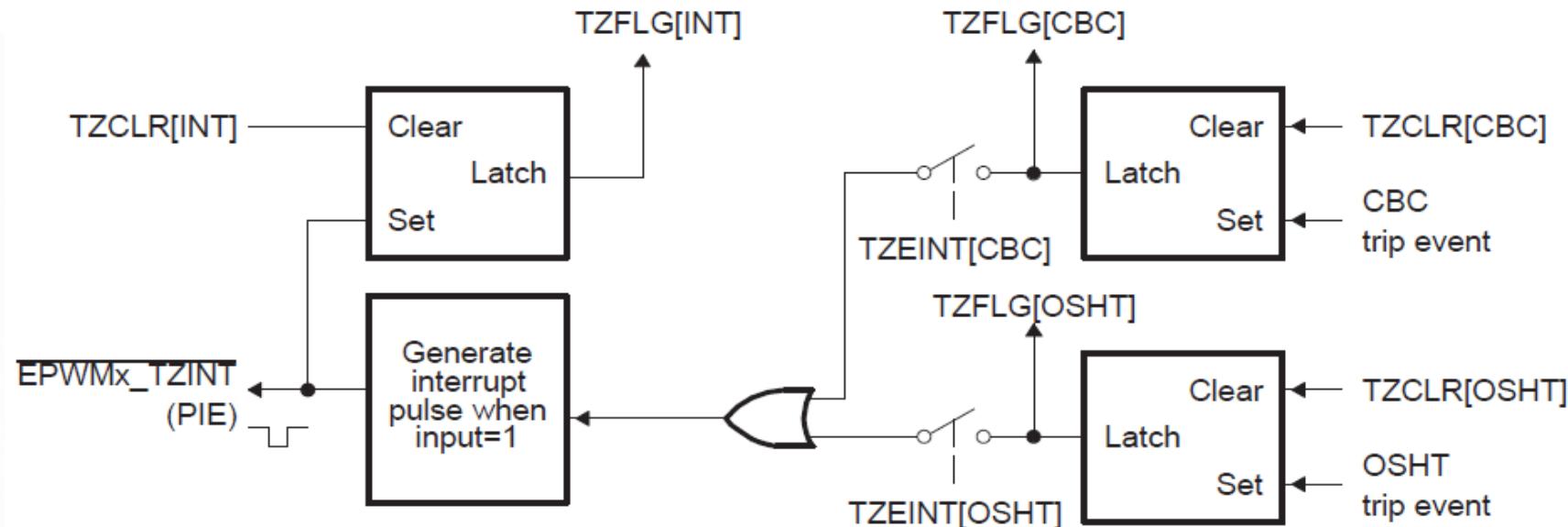
当one-shot trip事件发生时, 在**TZCTL**寄存器中指定的动作将立刻执行到**EPWMxA**或**EPWMxB**输出, 同时one-shot trip事件标志(**TZFLG[OST]**)被置位, 且**EPWMx_TZINT**中断产生, 只要**TZEINT**寄存器和**PIE**外设使能。



Table 2-18. Possible Actions On a Trip Event

TZCTL[TZA] and/or TZCTL[TZB]	EPWM xA and/or EPWMxB	Comment
0,0	High-Impedance	Tripped
0,1	Force to High State	Tripped
1,0	Force to Low State	Tripped
1,1	No Change	Do Nothing. No change is made to the output.

Figure 2-36. Trip-Zone Submodule Interrupt Logic



事件触发子模块Event-Trigger (ET)

事件触发字模块的关键功能如下：

接收时基和计数比较字模块的事件输入

使用时基方向信息响应上升/下键事件：

在下列几种情况下使用比例因子逻辑产生中断请求和启动ADC转换：

- 每次事件 (**Every event**)
- 每两次事件 (**Every second event**)
- 每三次事件 (**Every third event**)

通过事件计数器和标志提供事件产生的全可视化。

允许软件强制中断和ADC开始转换。

当事件产生时事件触发子模块管理时基子模块的事件的产生和计数比

较子模块产生CPU中断，产生ADC开始转换的脉冲。



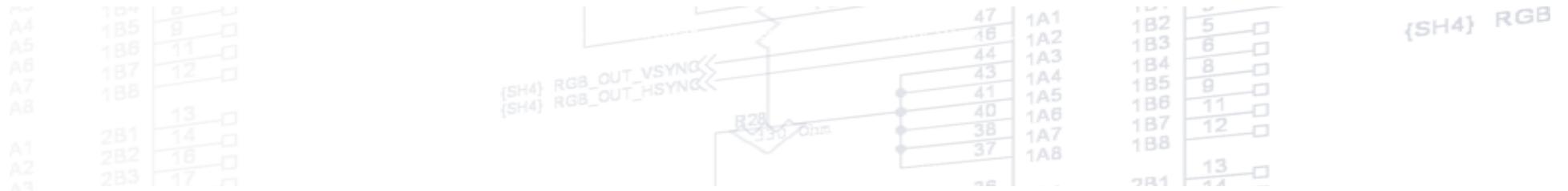


Figure 2-37. Event-Trigger Submodule

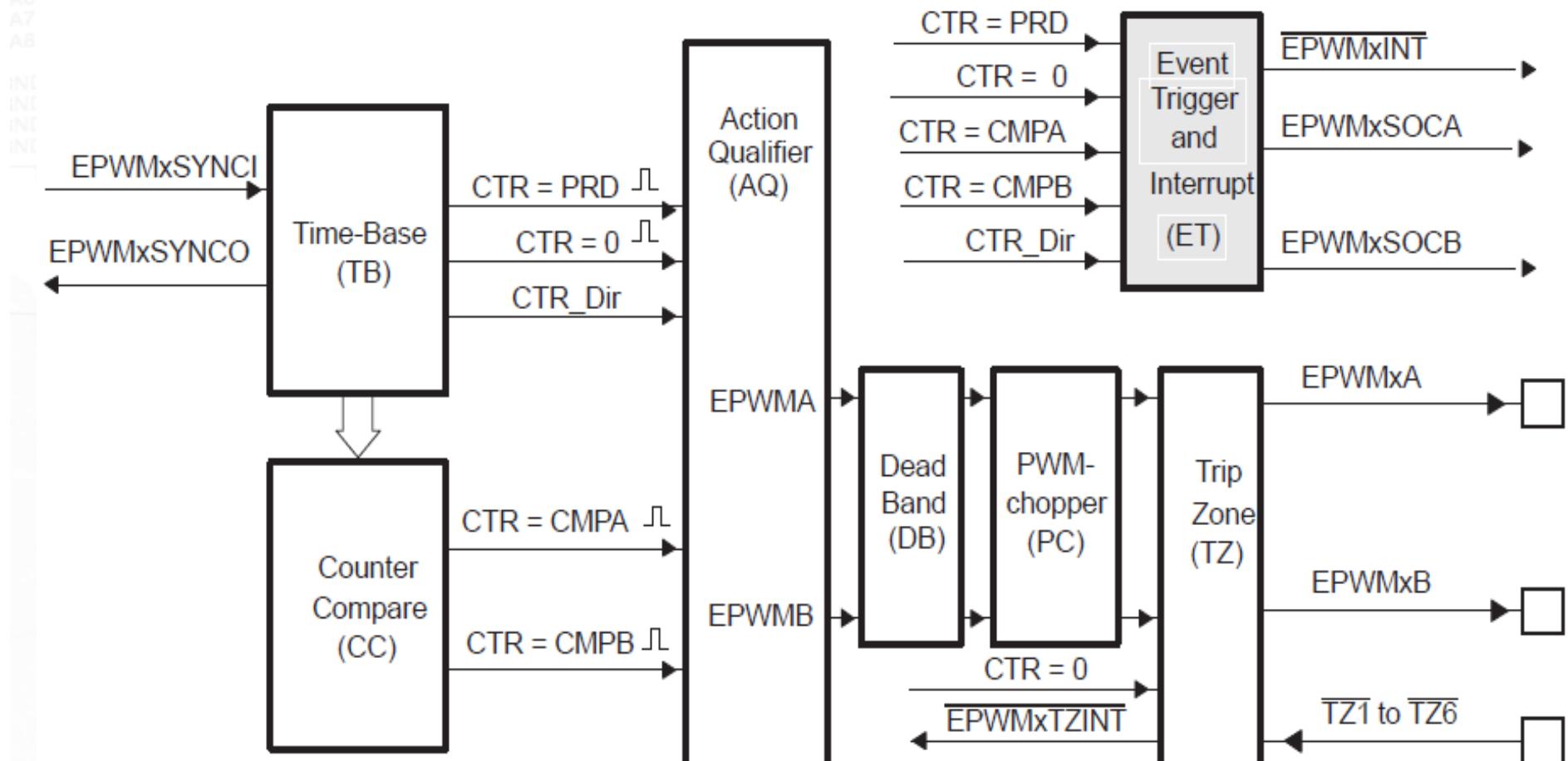


Figure 3-9. Control of Dual 3-Phase Inverter Stages as Is Commonly Used in Motor Control

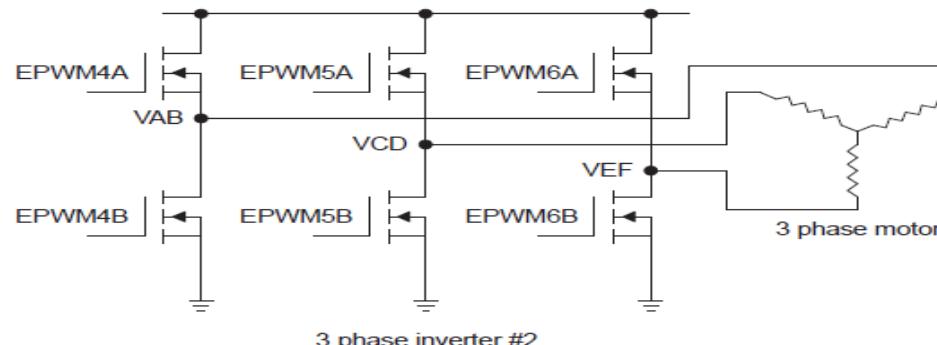
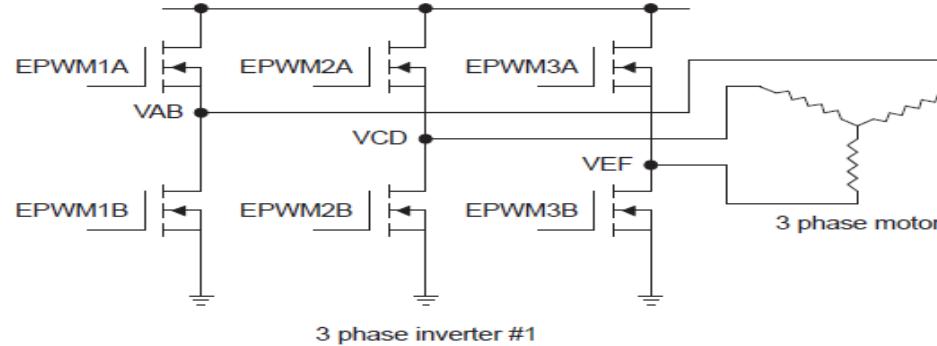
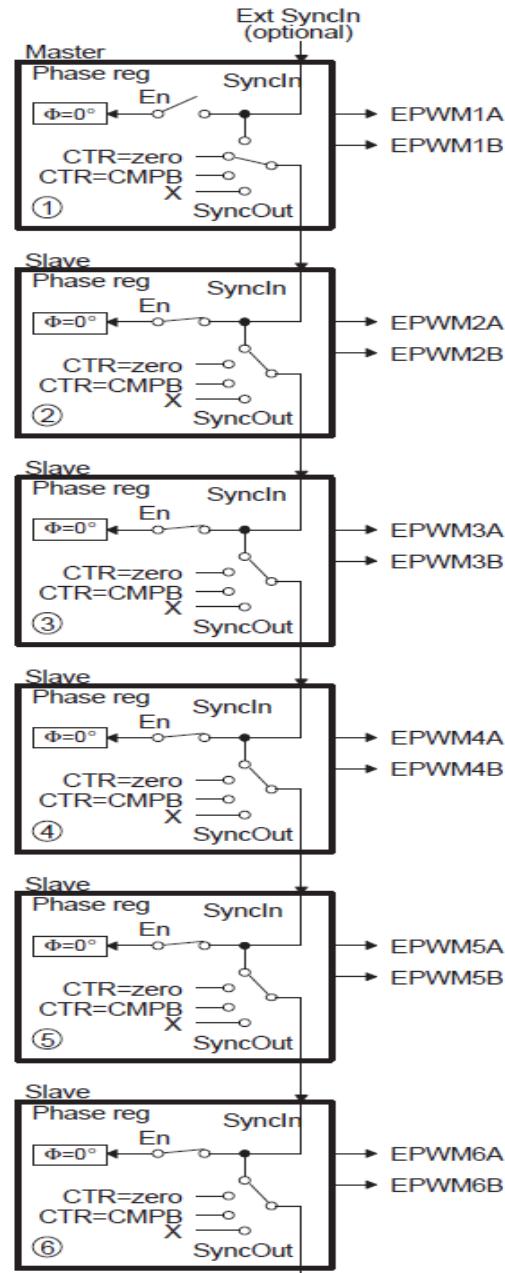


Figure 3-10. 3-Phase Inverter Waveforms for Figure 3-9 (Only One Inverter Shown)

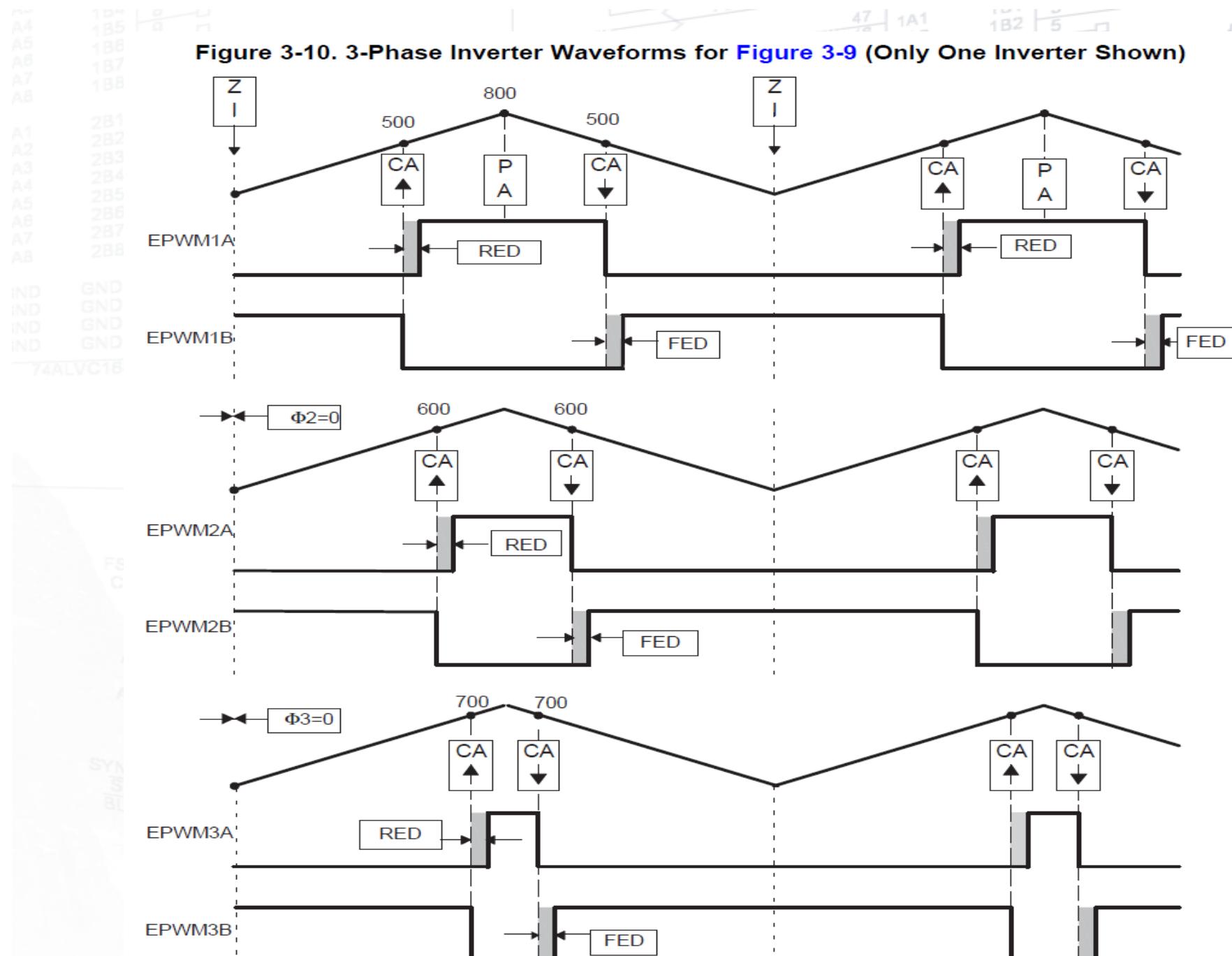


Figure 3-11. Configuring Two PWM Modules for Phase Control

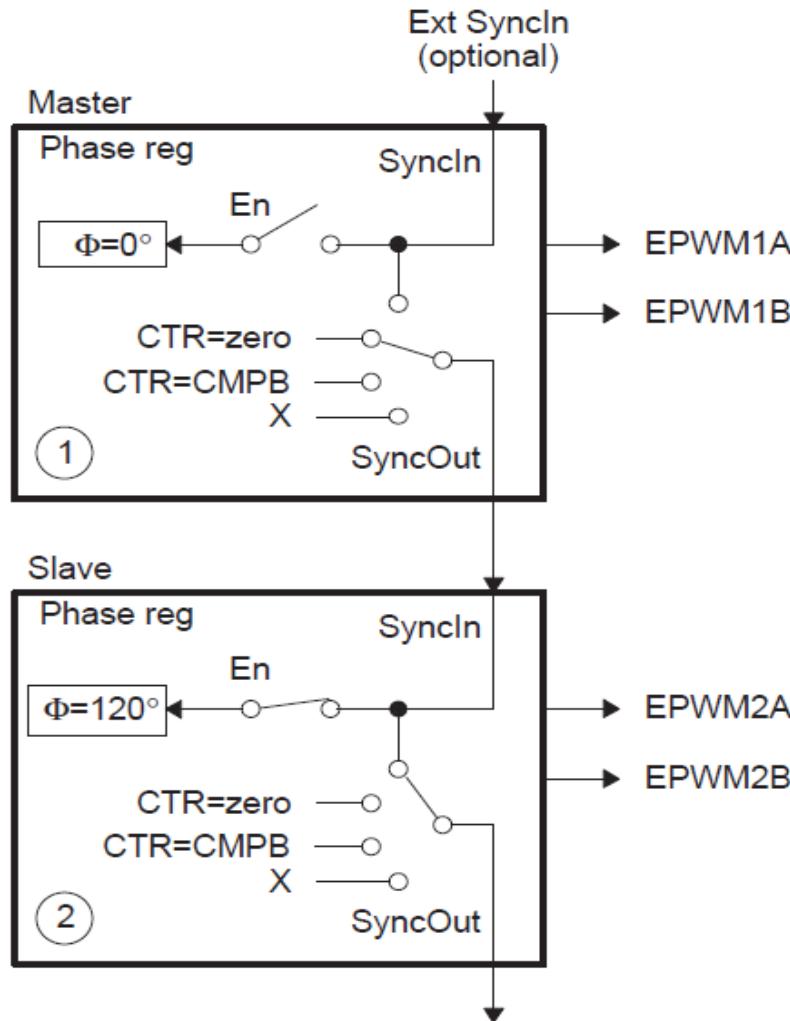
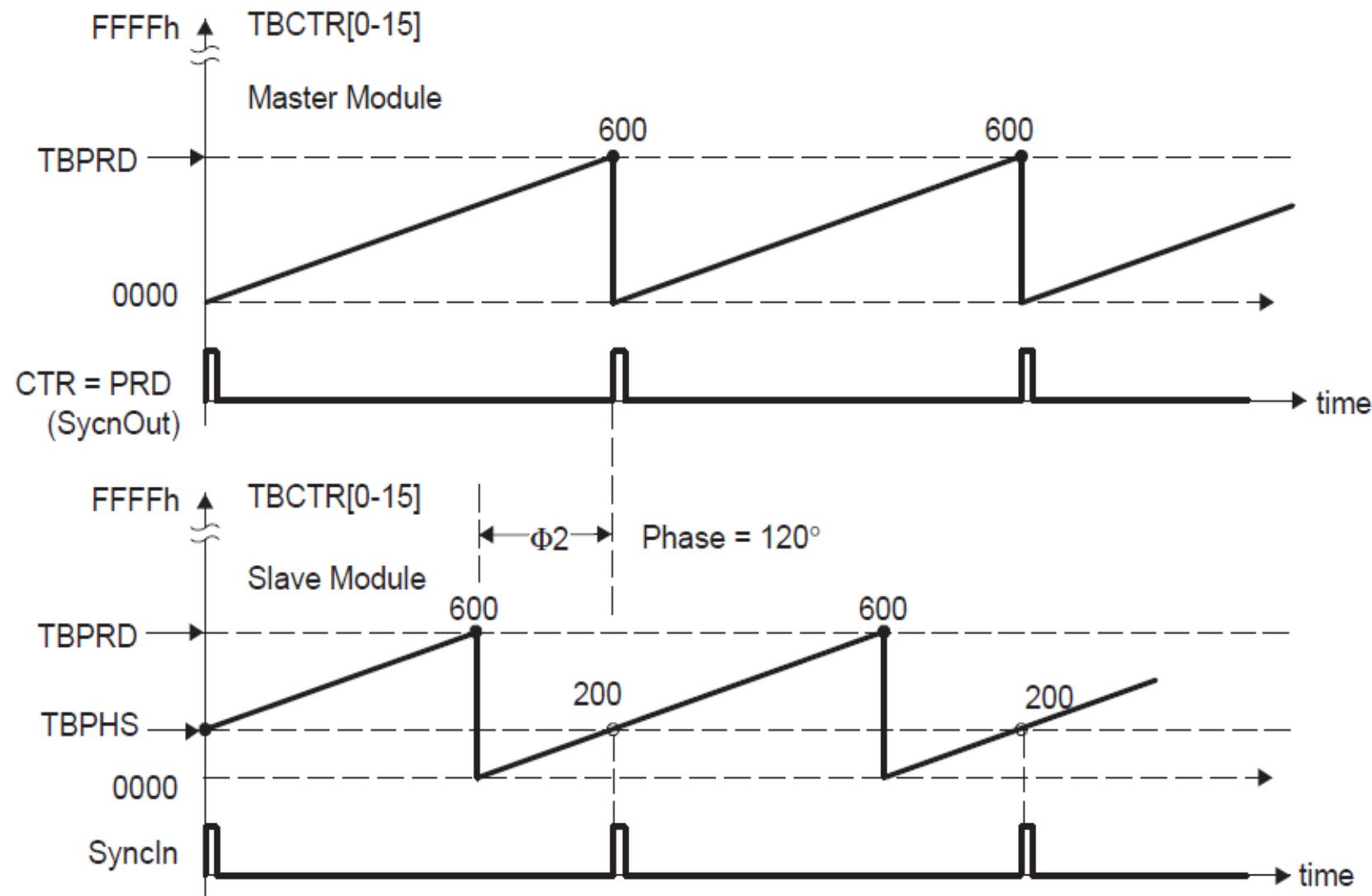


Figure 3-12 shows the associated timing waveforms for this configuration. Here, $TBPRD = 600$ for both master and slave. For the slave, $TBPHS = 200$ (i.e., $200/600 \times 360^\circ = 120^\circ$). Whenever the master generates a SyncIn pulse (CTR = PRD), the value of $TBPHS = 200$ is loaded into the slave TBCTR register so the slave time-base is always leading the master's time-base by 120° .



Figure 3-12. Timing Waveforms Associated With Phase Control Between 2 Modules



107
A4
A5
A6
A7
A8

47
1A1
1A2
44
1B2
5
1B3
6

{SH4} RGB

Figure 3-13. Control of a 3-Phase Interleaved DC/DC Converter

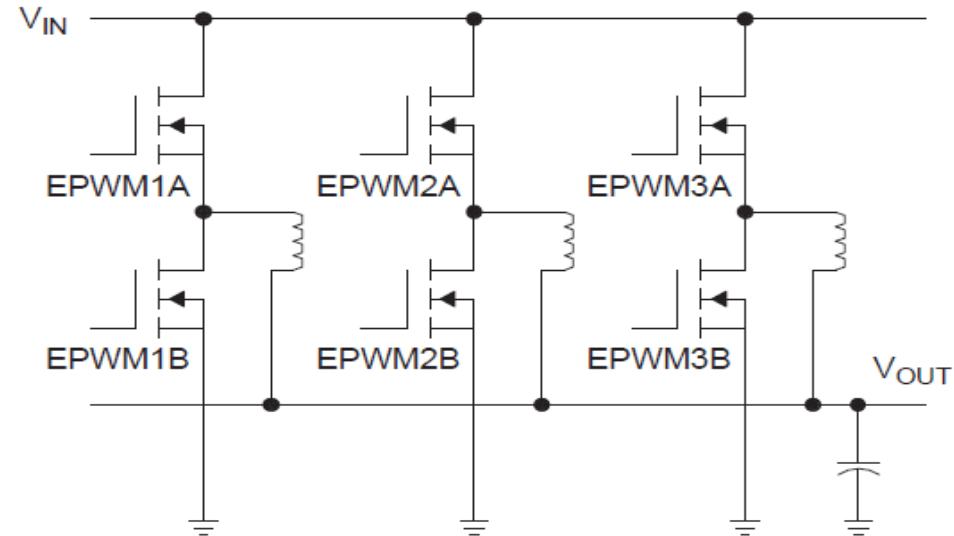
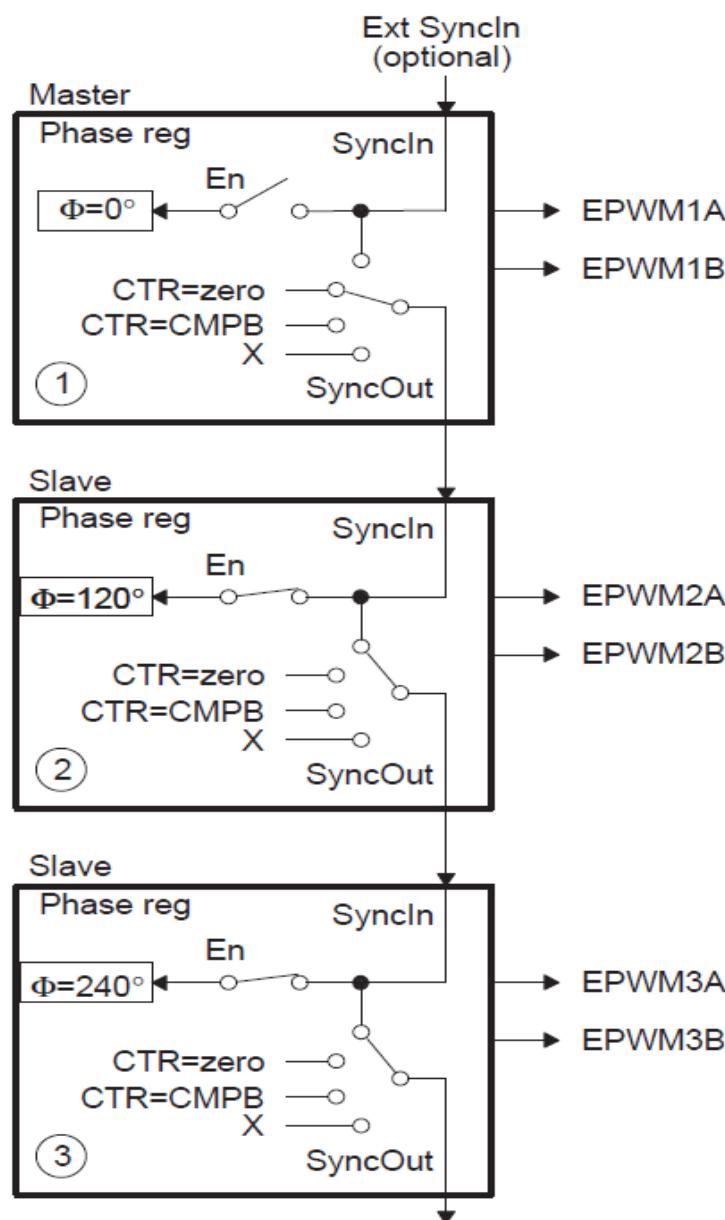
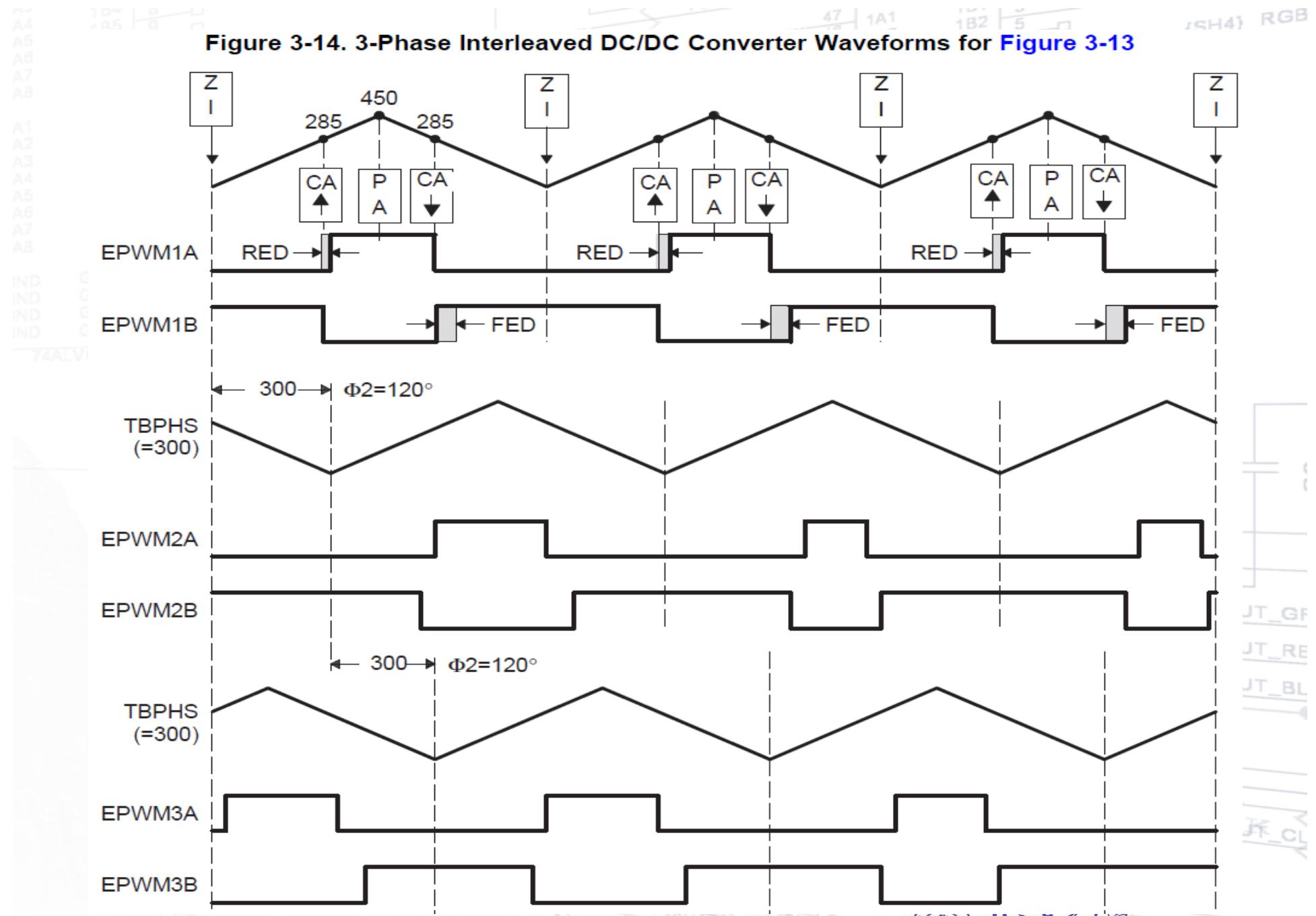


Figure 3-14. 3-Phase Interleaved DC/DC Converter Waveforms for Figure 3-13





{SH4} RGB

Figure 3-15. Controlling a Full-H Bridge Stage ($F_{PWM2} = F_{PWM1}$)

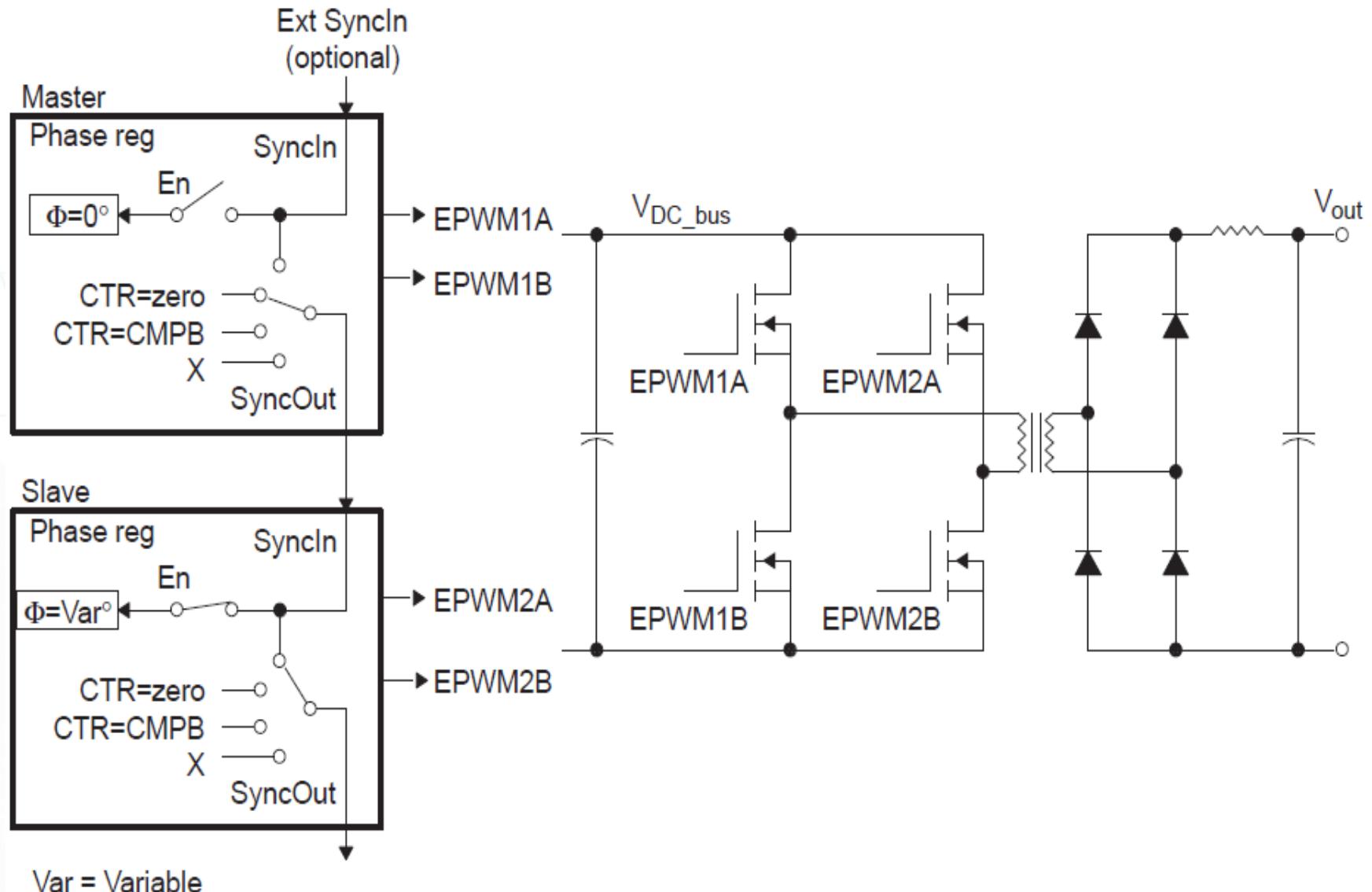
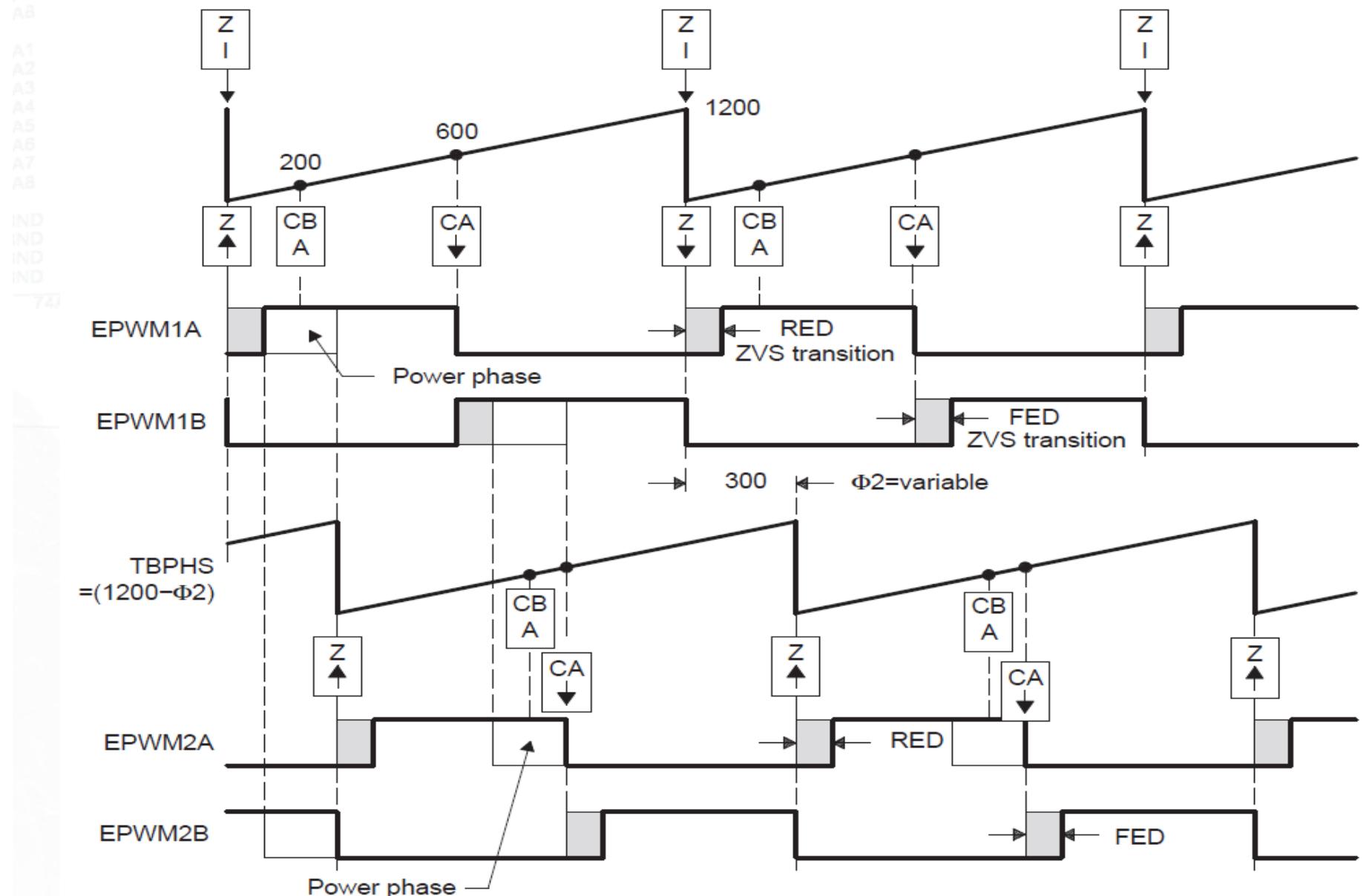


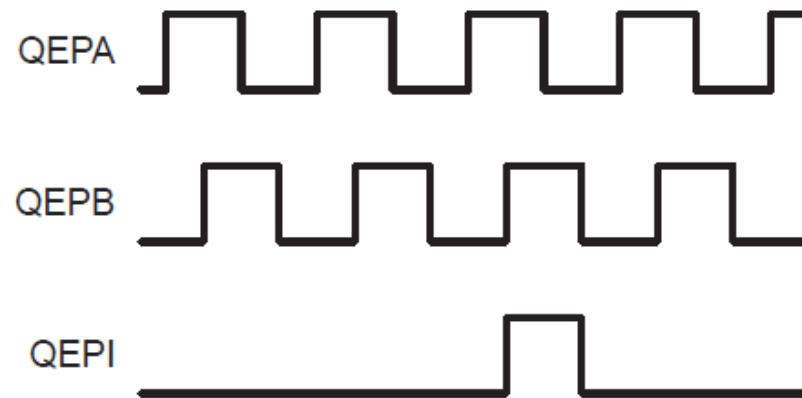
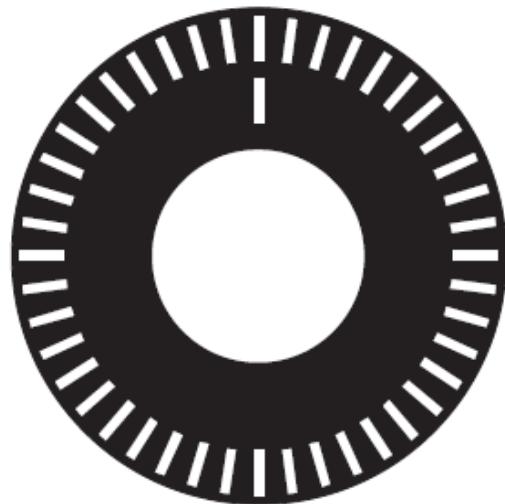
Figure 3-16. ZVS Full-H Bridge Waveforms



§ 7.2 增强正交编码模块 Enhanced QEP (eQEP) Module

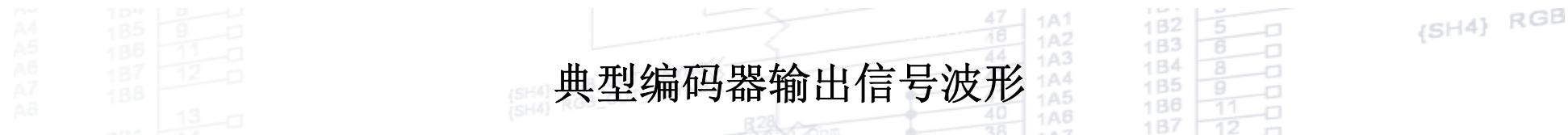
eQEP模块的主要功能是线性和旋转增量编码接口以获得旋转电机的位置、方向和速度信息，适用于高性能运动和位置控制系统。

Figure 1. Optical Encoder Disk



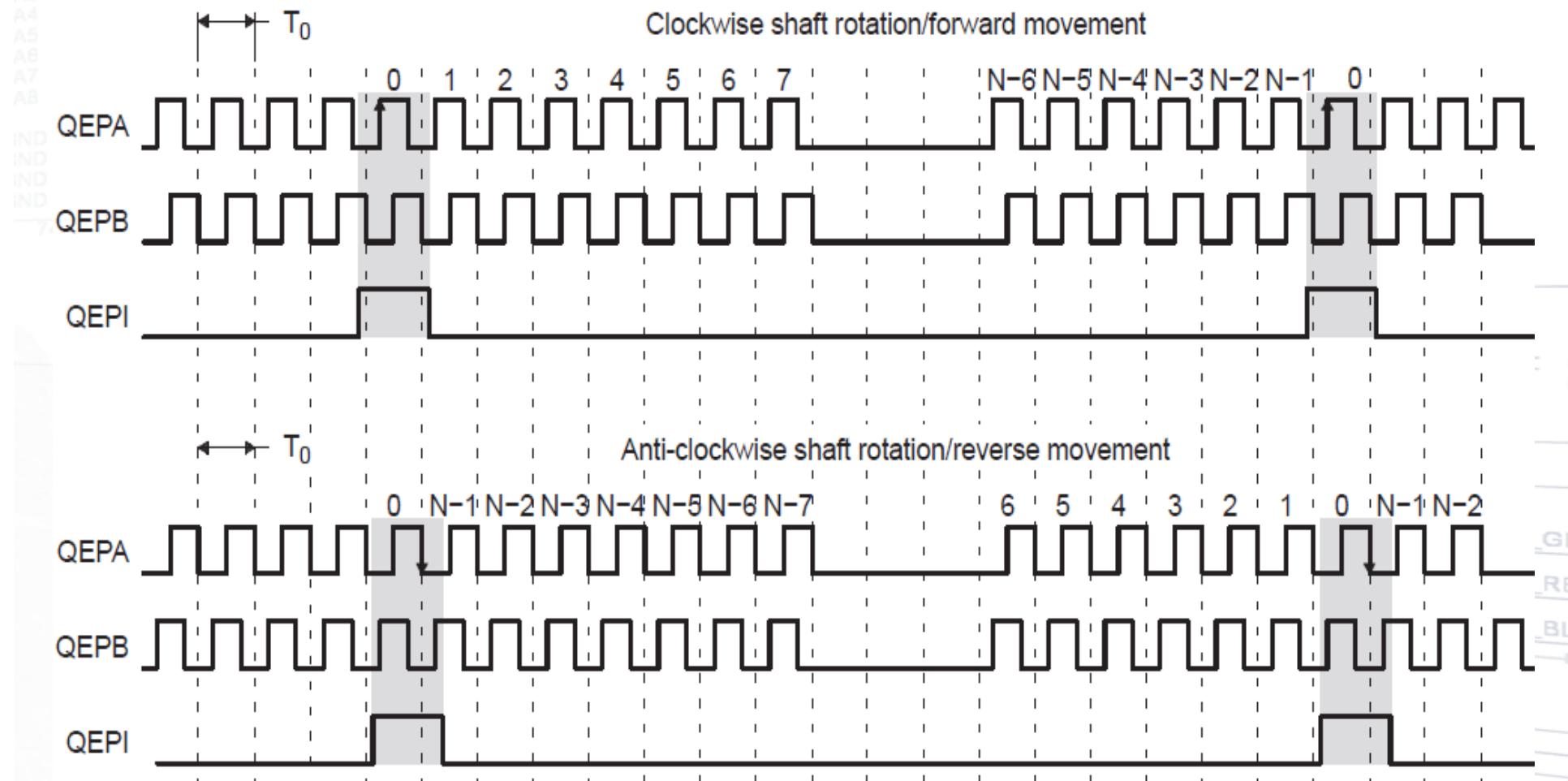
典型的码盘工作原理





典型编码器输出信号波形

Figure 2. QEP Encoder Output Signal for Forward/Reverse Movement



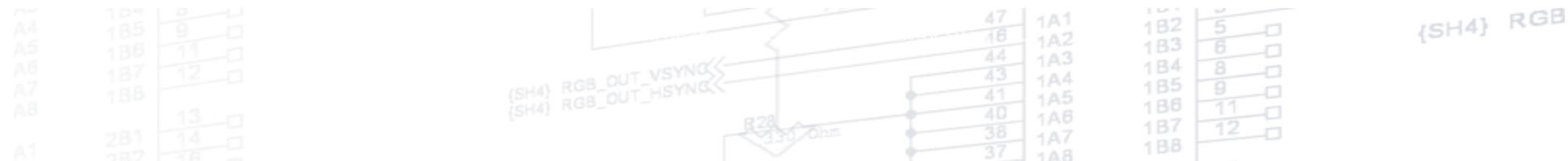
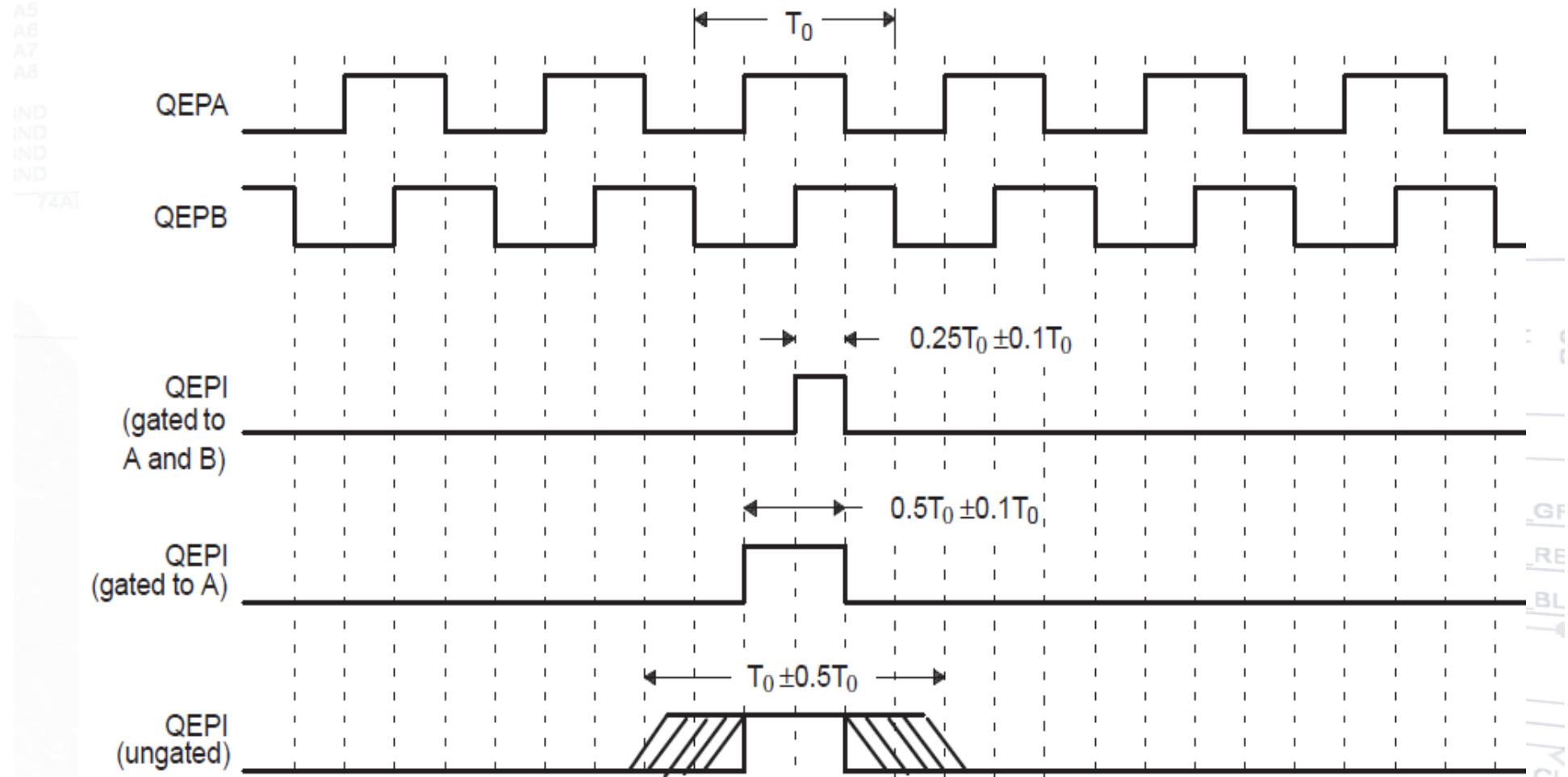
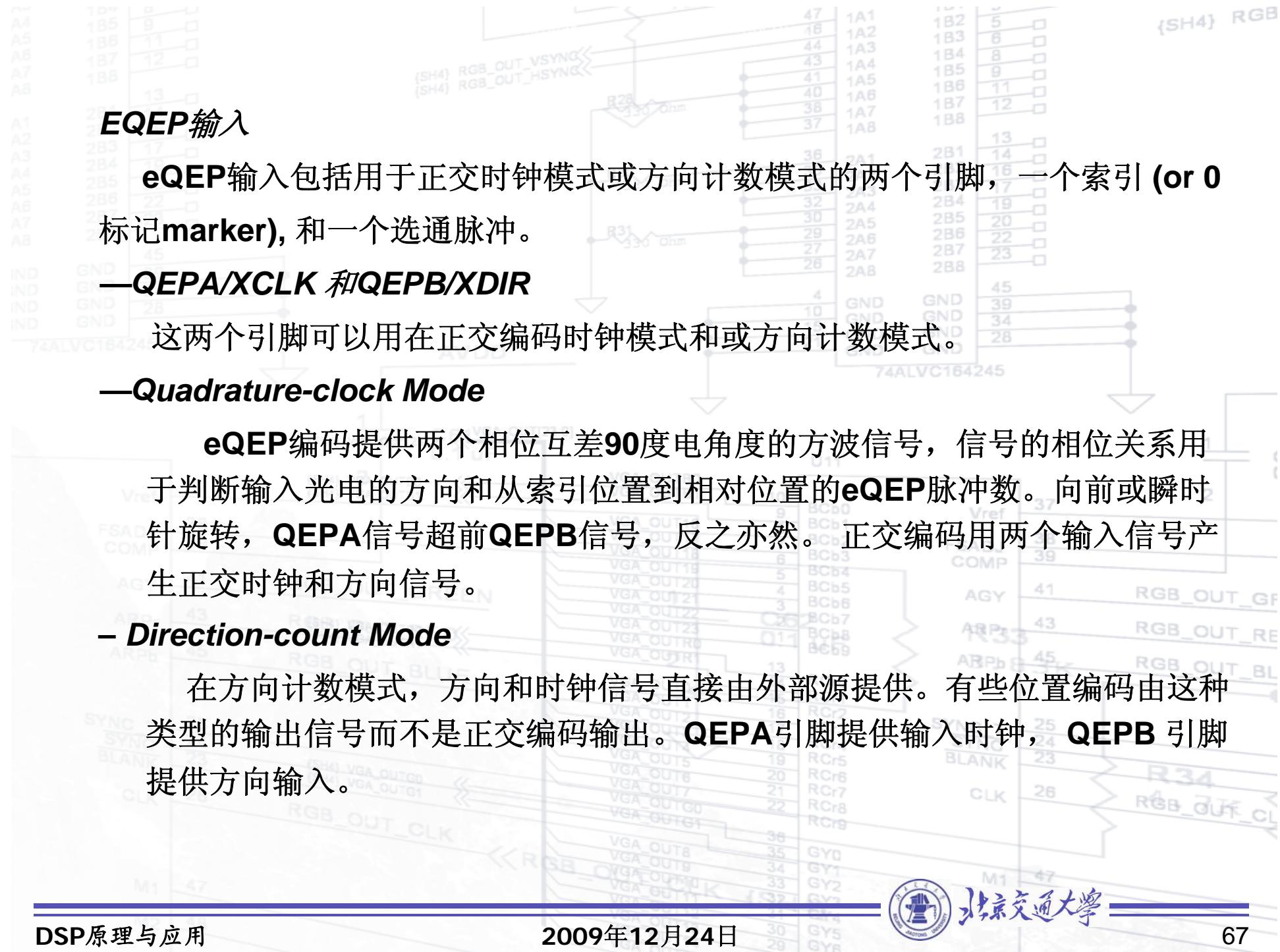
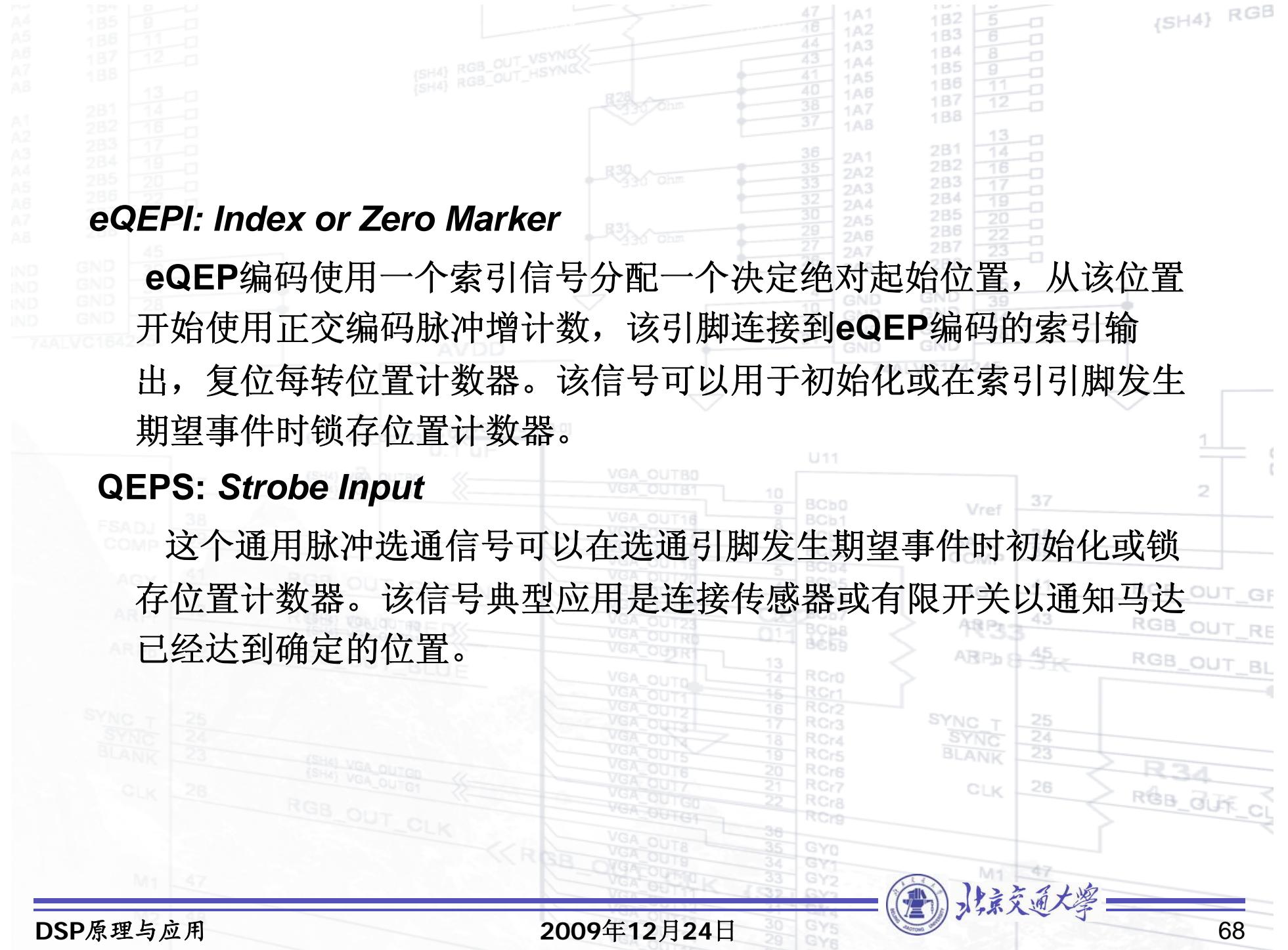


Figure 3. Index Pulse Example







A4 107 | 8 11
 A5 185 | 9 11
 A6 186 | 10 11
 A7 187 | 11 11
 A8 188 | 12 11
 A1 281 | 13 11
 A2 282 | 14 11
 A3 283 | 15 11
 A4 284 | 16 11
 A5 285 | 17 11
 A6 286 | 18 11
 A7 287 | 19 11
 A8 288 | 20 11
 IND GND
 IND GND
 IND GND
 IND GND
 74ALVC164

正交编码外设功能框图

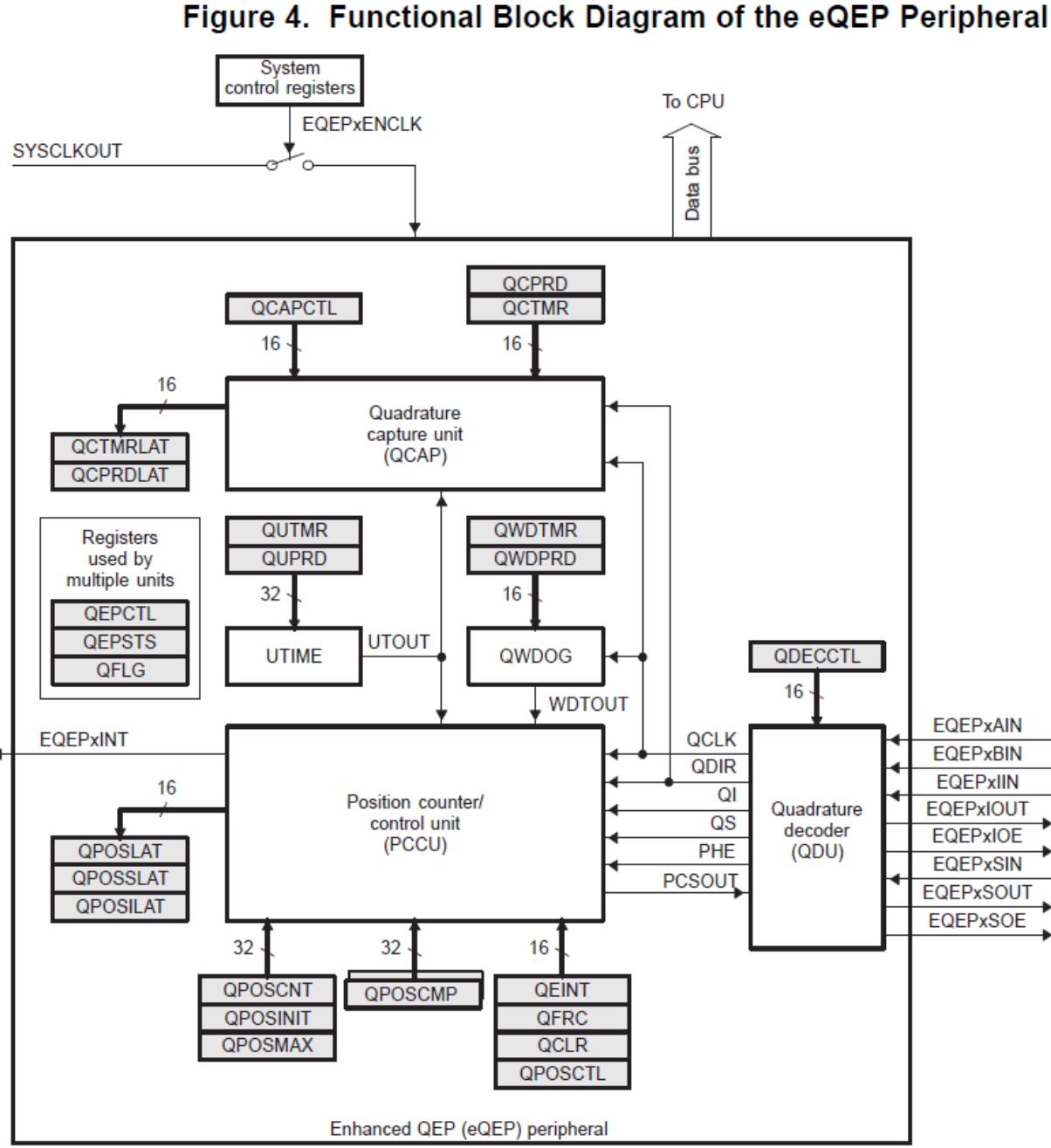
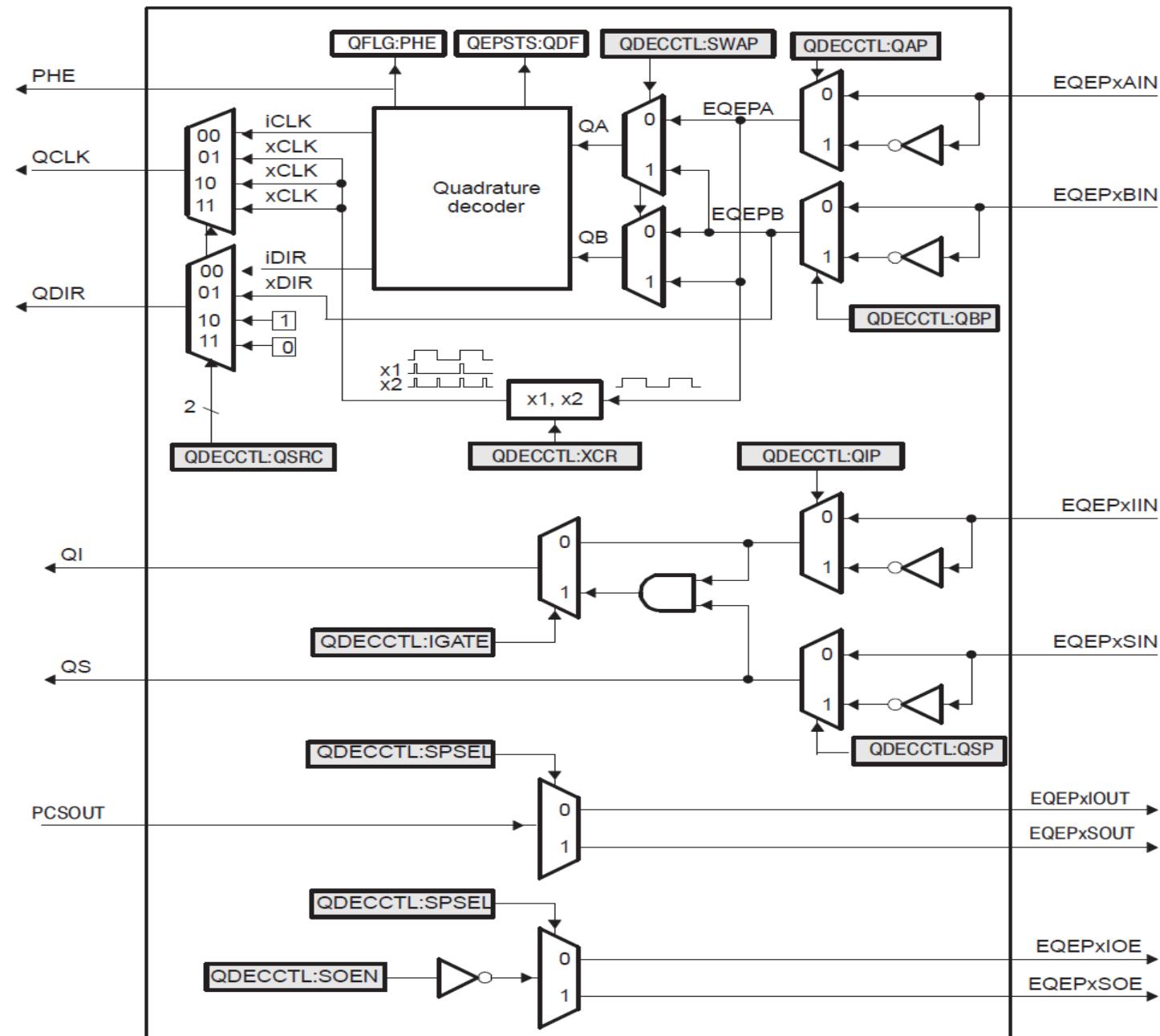


Figure 5. Functional Block Diagram of Decoder Unit

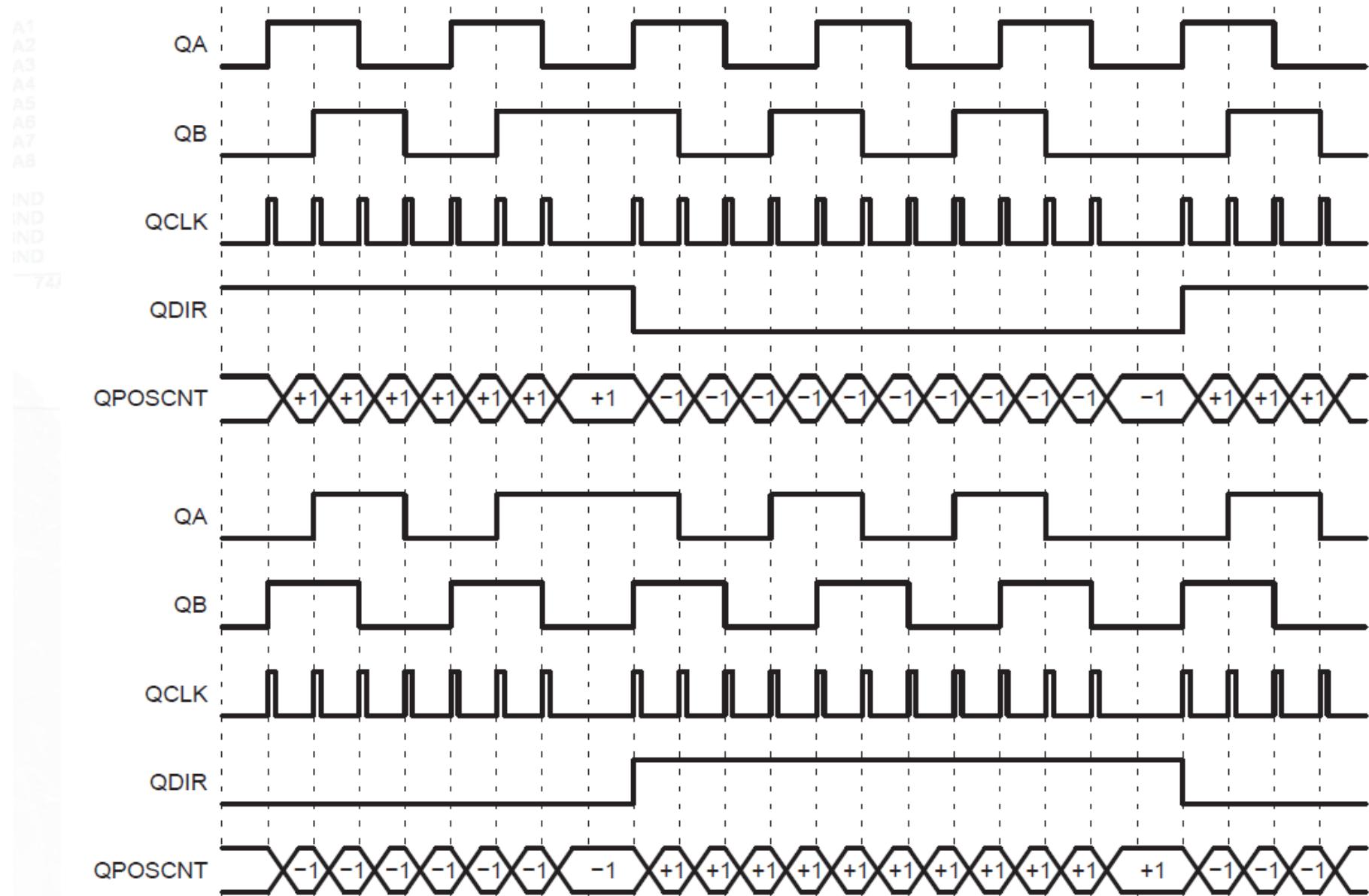


解码单元功能框图



{SH4} RGB

Figure 7. Quadrature-clock and Direction Decoding



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