Piccolo ADC Usage Recommendation

Apr. 2013

Piccolo ADC Spec

6.11.13 On-Chip Analog-to-Digital Converter

Table 6-37. ADC Electrical Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
DC SPECIFICATIONS					
Resolution		12			Bits
ADC clock	60-MHz device	0.001		60	MHz
Sample Window	28035/34/33/32	7		64	ADC Clocks
	28031/30	24		64	
ACCURACY					
INL (Integral nonlinearity) at ADC Clock ≤ 30 MHz (1)		–4		4	LSB
DNL (Differential nonlinearity) at ADC Clock ≤ 30 MHz, no missing codes		–1		1	LSB
Offset error (2)	Executing a single self-recalibration (3)	–20	0	20	LSB
	Executing periodic self-recalibration (4)	–4	0	4	
Overall gain error with internal reference		–60		60	LSB
Overall gain error with external reference		–40		40	LSB
Channel-to-channel offset variation		–4		4	LSB
Channel-to-channel gain variation		–4		4	LSB
ADC temperature coefficient with internal reference			–50		ppm/°C
ADC temperature coefficient with external reference			–20		ppm/°C
V_{REFLO}			–100		µA
V_{REFHI}			100		µA
ANALOG INPUT					
Analog input voltage with internal reference		0		3.3	V
Analog input voltage with external reference		V_{REFLO}		V_{REFHI}	V
V_{REFLO} input voltage (5)		V_{SSA}		0.66	V
V_{REFHI} input voltage (6)		2.64		V_{DDA}	V
	with $V_{REFLO} = V_{SSA}$	1.98		V_{DDA}	
Input capacitance			5		pF
Input leakage current			±2		µA

(1) INL will degrade when the ADC input voltage goes above V_{DDA}.
(2) 1 LSB has the weighted value of full-scale range (FSR)/4096. FSR is 3.3 V with internal reference and V_{REFHI} - V_{REFLO} for external reference.
(3) For more details, see the *TMS320F28030, TMS320F28031, TMS320F28032, TMS320F28033, TMS320F28034, TMS320F28035 Piccolo MCU Silicon Errata* (literature number SPRZ295).
(4) Periodic self-recalibration will remove system-level and temperature dependencies on the ADC zero offset error. This can be performed as needed in the application without sacrificing an ADC channel by using the procedure listed in the "ADC Zero Offset Calibration" section of the *TMS320x2802x, 2803x Piccolo Analog-to-Digital Converter (ADC) and Comparator Reference Guide* (literature number SPRUGE5).
(5) V_{REFLO} is always connected to V_{SSA} on the 64-pin PAG device.
(6) V_{REFHI} must not exceed V_{DDA} when using either internal or external reference modes. Since V_{REFHI} is tied to ADCINA0 on the 64-pin PAG device, the input signal on ADCINA0 must not exceed V_{DDA}.

ADC Resolution/Accuracy Definition

Typically, there're 3 ways to define ADC's resolution/accuracy.

- **Resolution measured by bit**

This is common to users and vendor, but the real resolution is indicated by ENOB (Effective Number of Bits). All current C2000 devices' ADC is 12bit but only have ~11ENOB.

- **Total error expressed by percentage (%)**

This is typically used by users in an application point of view, which tells the total error range for a specific input signal.

i.e. 1% accuracy for 2.5v means converted voltage of sampled ADC result conversion can fall into the range of 2.5v+/-1% (2.475~2.525v), which will be treated as meeting the 1% accuracy.

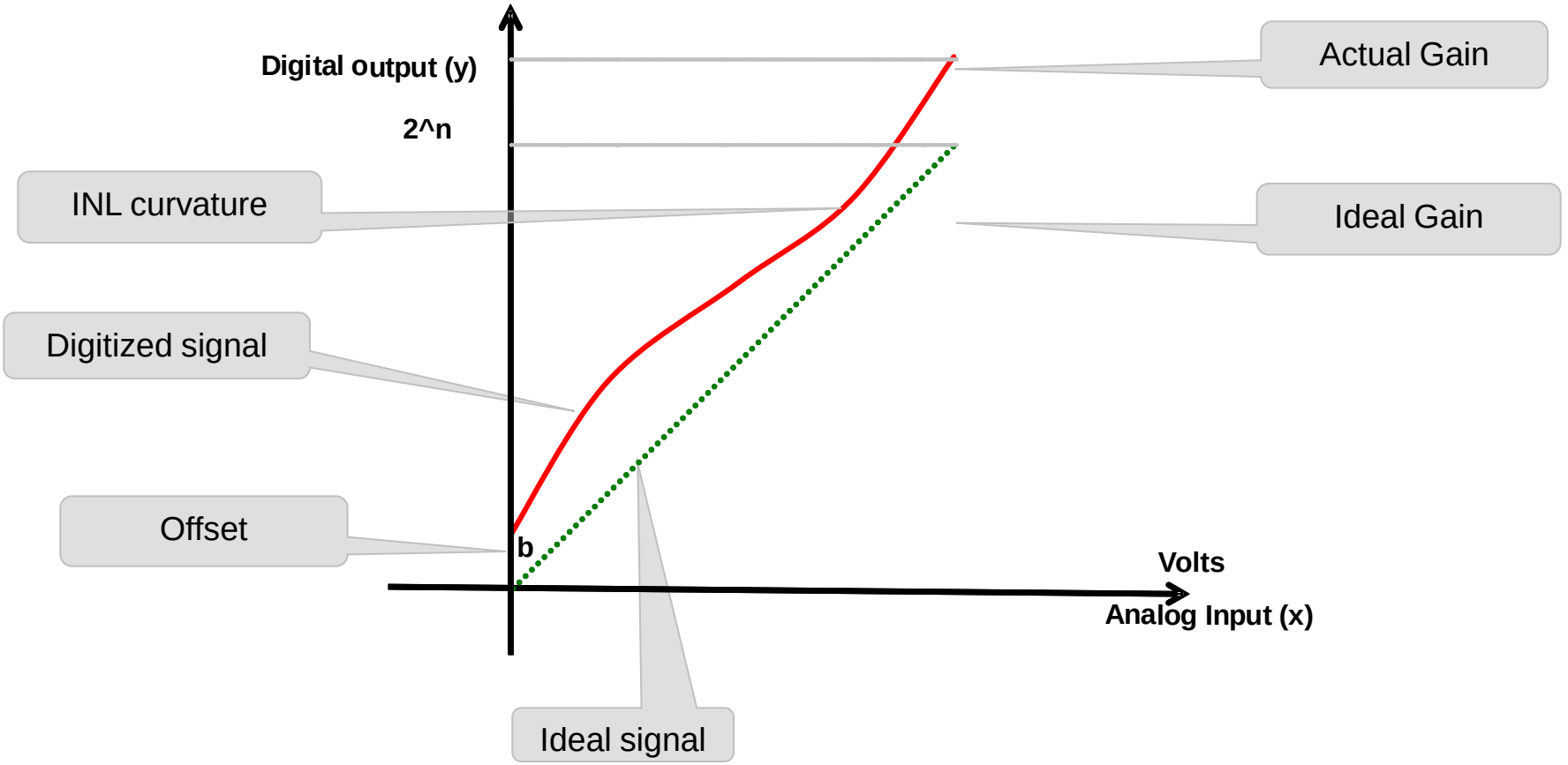
- **Accuracy indicated by LSB (least significant bit)**

This is always described in DS spec by semiconductor vendor, to show the accurate drift error on measured ADC results. This error can generally be divided into three types and the spec for each of them are listed below as indicated in previous spec:

- ✓ Offset error: -20~+20LSBs w/ single cal or -4~+4LSBs w/ periodic cal;
- ✓ Gain error: -60~+60LSBs w/ internal ref or -40~+40LSBs w/ external ref;
- ✓ INL/DNL(Integral/Differential nonlinearity): -4~+4LSBs/-1~+1LSB when ADCCLK ≤ 30 MHz

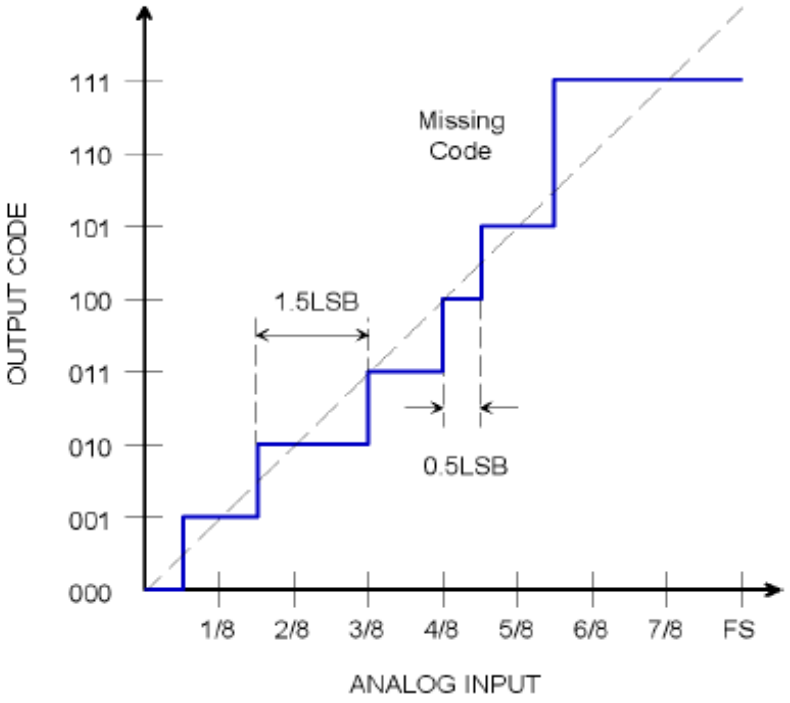
No matter which way is used to define ADC resolution, all of them are compatible and aligned.

What Contributes to ADC Error?

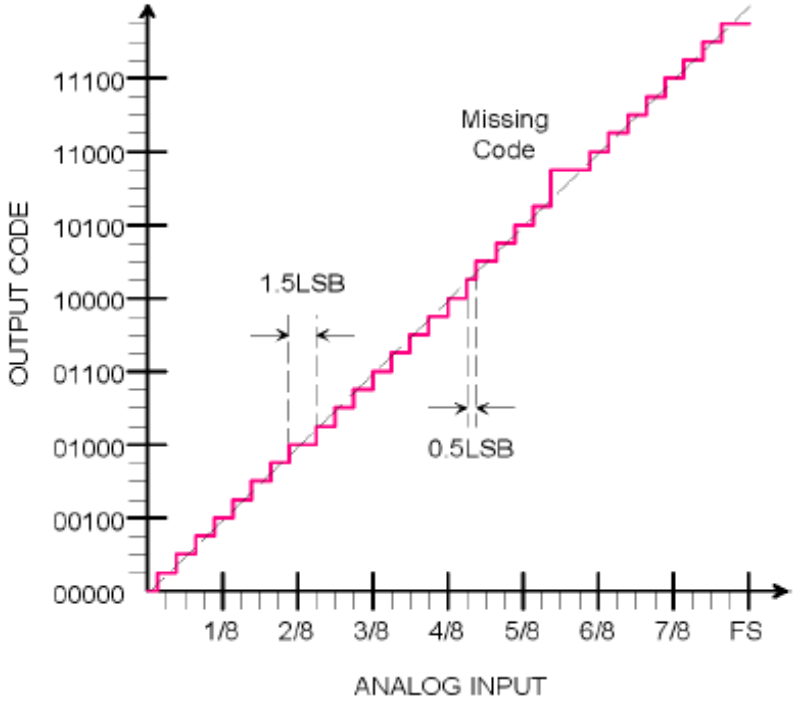


ADC error is mainly determined by three items: Offset error, Gain error and INL.

Impact of Differential Non-Linearity



3-bit resolution ADC



5-bit resolution ADC

Total Error Definition

- Total Error is by definition the summation of all DC related errors shown previously
  - Gain error (in LSBs)
  - Offset error (in LSBs)
  - INL error (in LSBs)
- However, summation method is pessimistic
  - Assumes all max errors for above occur at a common point in the transfer function
  - For Piccolo ADCs, worst case gain/offset errors both occur at temperature corners of the device
  - Gain error max can by definition only occur at full scale range (FSR: 3.3V) of the device
- More accepted approach is sum of squares method
  - $SQRT((Err_{Gain})^2 + (Err_{Offset})^2 + (Err_{INL})^2)$

Error Optimization

There are ways to reduce the error effects of both gain and offset.

- Offset
  - TI provides ability to self correct for offset error
  - Range of +/-255LSBs of offset correction
  - Logic resides in the analog domain, so no loss of signal range
  - Internal connection to VREFLO so external pin connection is un-necessary
  - Ability to re-calibrate based on system need dynamically
  - Then the offset error will be zero after recalibration

- Gain
  - Through use of 1 other known input can remove gain error
  - Only as accurate as the external source
  - Must use one channel for this
  - Gain error correction must be applied mathematically by SW post conversion
  - Then the gain error will be also zero after recalibration

ADC Usage Recommendation(1) -- ACQPS

All the items mentioned below can refer to related to DS/Errata/ADC UG.

- Sample window recommended in the DS (SPRS584B/SPRS523D, Sep./Oct. 2009)
  - For different device, different minimum sample window is suggested to use.

Sample Window	28027/26/23/22	7	64	ADC Clocks
	28021/20/200	14	64	
Sample Window	28035/34/33/32	7	64	ADC Clocks
	28031/30	24	64	

- Invalid ACQPS selections showed in ADC UG (SPRUGE5B, Dec. 2009)

Table 18. ADC SOC0 - SOC15 Control Registers (ADCSOCxCTL) Register Field Descriptions (continued)

Bit	Field	Value	Description
5-0	ACQPS		SOCx Acquisition Prescale. Controls the sample and hold window for SOCx. Minimum value allowed is 6.
		00h	Invalid selection.
		01h	Invalid selection.
		02h	Invalid selection.
		03h	Invalid selection.
		04h	Invalid selection.
		05h	Invalid selection.
		06h	Sample window is 7 cycles long (6 + 1 clock cycles).
		07h	Sample window is 8 cycles long (7 + 1 clock cycles).
		08h	Sample window is 9 cycles long (8 + 1 clock cycles).
		09h	Sample window is 10 cycles long (9 + 1 clock cycles).
		...	...
		3Fh	Sample window is 64 cycles long (63 + 1 clock cycles)
Other invalid selections: 10h, 11h, 12h, 13h, 14h, 1Dh, 1Eh, 1Fh, 20h, 21h, 2Ah, 2Bh, 2Ch, 2Dh, 2Eh, 37h, 38h, 39h, 3Ah, 3Bh			

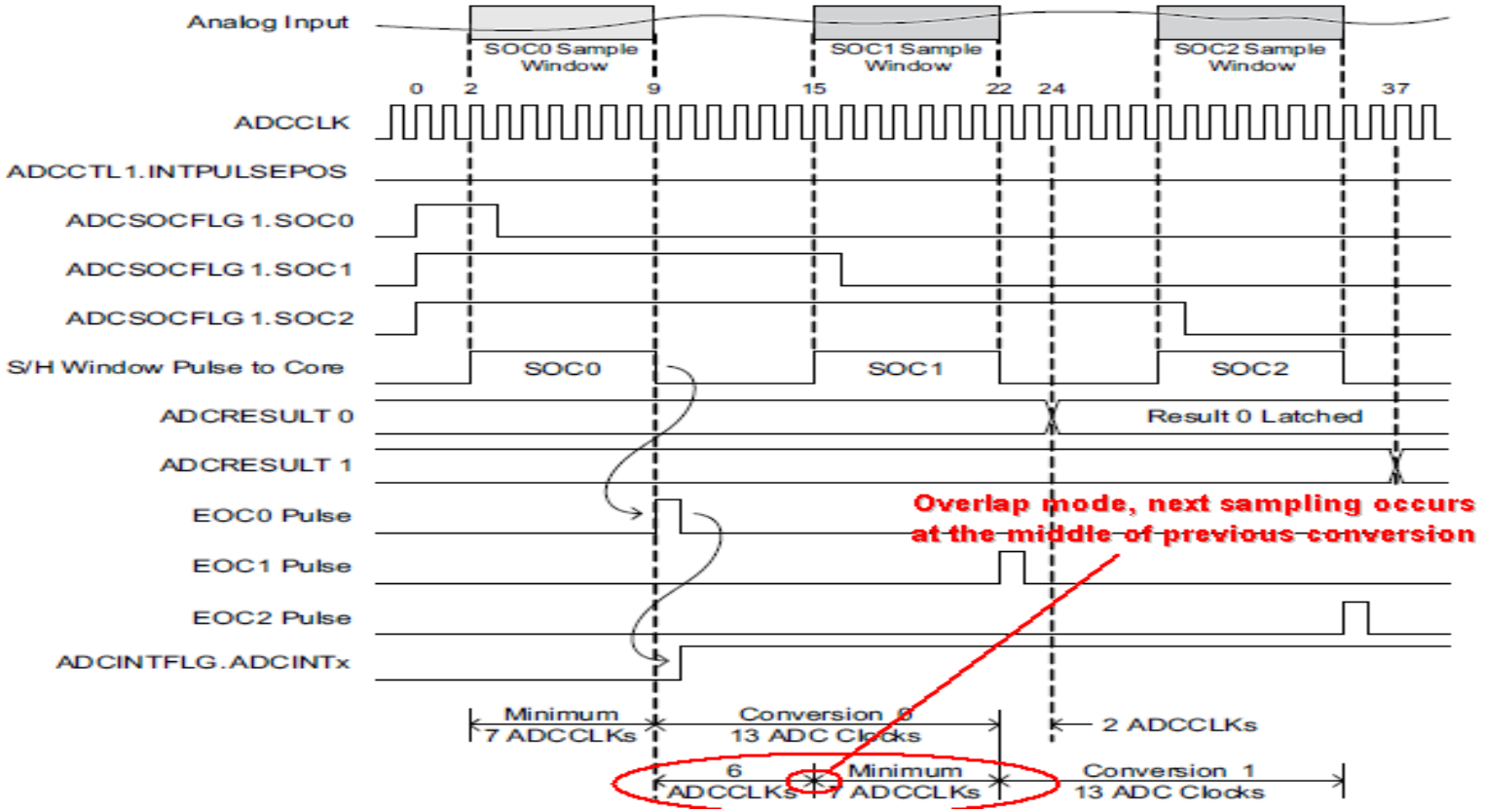
ADC Usage Recommendation(2) -- ACQPS Continued

➢ ADC Result Conversion When Sampling Ends on 14th Cycle of Previous Conversion (SPRZ292D, Jul. 2010, SPRZ295E, Apr. 2011)

- ACQPS can not be all 7
- ACQPS can not be 6 and 7 in successive SOC's configuration
- Recommend ACQPS to be all 6 or 8 or above according to previous limitations

Advisory	***ADC: ADC Result Conversion When Sampling Ends on 14th Cycle of Previous Conversion, ACQPS = 6 or 7***
Revision(s) Affected	0, A
Details	The on-chip ADC takes 13 ADC clock cycles to complete a conversion after the sampling phase has ended. The result is then presented to the CPU on the 14th cycle post-sampling and latched on the 15th cycle into the ADC result registers. If the next conversion's sampling phase terminates on this 14th cycle, the results latched by the CPU into the result register are not assured to be valid across all operating conditions.
Workaround(s)	Some workarounds are as follows: • Due to the nature of the sampling and conversion phases of the ADC, there are only two values of ACQPS (which controls the sampling window) that would result in the above condition occurring—ACQPS = 6 or 7. One solution is to avoid using these values in ACQPS. • When the ADCNONOVERLAP feature (bit 1 in ADCTRL2 register) is used, the above condition will never be met; so the user is free to use any value of ACQPS desired. • Depending on the frequency of ADC sampling used in the system, the user can determine if their system will hit the above condition if the system requires the use of ACQPS = 6 or 7. For instance, if the converter is continuously converting with ACQPS = 6, the above condition will never be met because the end of the sampling phase will always fall on the 13th cycle of the current conversion in progress.

ADC Usage Recommendation(3) -- ACQPS Continued



It's not allowed that the next conversion's sampling phase terminates on previous conversion's 14th cycle, since the results latched by the CPU into the result register are not assured to be valid across all operating conditions.

ADC Usage Recommendation(4) -- Offset Periodic Re-calibration

- Offset Self-Recalibration Requirement (SPRZ295J, Feb. 2012)
  - Factory offset calibration from Device_cal() may not ensure ADC offset remains within spec under all operating condition especially with respect to temperature drift
  - Periodic offset re-calibration can help to keep the offset error within -4~+4LSBs
  - Users can determine the re-calibration period in background based on their system

Advisory	***ADC: Offset Self-Recalibration Requirement***
Revision(s) Affected	0, A
Details	The factory offset calibration from Device_cal() may not ensure that the ADC offset remains within specifications under all operating conditions in the customer's system.
Workaround(s)	• To ensure that the offset remains within the data sheet's "single recalibration" specifications, perform the AdcOffsetSelfCal() function after Device_cal() has completed and the ADC has been configured. • To ensure that the offset remains within the data sheet's "periodic recalibration" specifications, perform the AdcOffsetSelfCal() function periodically with respect to temperature drift. For more details on AdcOffsetSelfCal(), refer to the "ADC Zero Offset Calibration" section of the *TMS320x2802x, 2803x Piccolo Analog-to-Digital Converter (ADC) and Comparator Reference Guide* (literature number SPRUGE5).

ADC Usage Recommendation(5) -- Initial Conversion

Advisory	***ADC: Initial Conversion***
Revision(s) Affected	0
Details	When the ADC conversions are initiated by any source of trigger in either sequential or simultaneous sampling mode, the first sample may not be the correct conversion result.
Workaround(s)	For sequential mode, discard the first sample at the beginning of every series of conversions. For instance, if the application calls for a given series of conversions, SOC0→SOC1→SOC2, to initiate periodically, then set up the series instead as SOC0→SOC1→SOC2→SOC3 and only use the last three conversions, ADCRESULT1, ADCRESULT2, ADCRESULT3, thereby discarding ADCRESULT0. For simultaneous sample mode, discard the first sample of both the A and B channels at the beginning of every series of conversions. User application should validate if this workaround is acceptable in their application. **The following is applicable to the revision A silicon:** • For 30-MHz operation and below, this is fixed completely by writing a 1 to the ADCNONOVERLAP and CLKDIV2EN bits in the ADCTRL2 register. This will give a 30-MHz ADC clock when the CPU clock = 60 MHz, and will only allow the sampling of ADC channels when the ADC is finished with any pending conversion. • For 60-MHz or 40-MHz operation, the first sample deviation is still under characterization by TI. The current recommendation is to observe the rev 0 errata until this characterization is complete.

SPRZ292, Dec. 2008
SPRZ295, Apr. 2009

ADC Usage Recommendation(6)
-- DC Specifications: Linearity Limitation

Advisory	***ADC: DC Specifications: Linearity Limitation***
Revision(s) Affected	0, A
Details	The linearity degrades with increasing temperature in the upper half of the transfer function.
Workaround(s)	The impact from this limitation has been addressed in the revision A silicon. The following features have been added: 1. ADC clock divider-by-2 enable bit. At 60 MHz, the effective sample rate will be 2.3 MSPS. This offers a 30-MHz ADC and a 60-MHz system clock, and improves linearity. 2. Existing pipeline mode with 4.6 MSPS at 60-MHz system clock will have improved linearity compared to revision 0 silicon.

NOTE: For 60-MHz operation, there are periodic missing codes, and INL will be bounded by ±28 LSBs MAX/MIN.

For 30-MHz operation, see the *TMS320F28030, TMS320F28031, TMS320F28032, TMS320F28033, TMS320F28034, TMS320F28035 Piccolo Microcontrollers Data Manual* (literature number SPRS584).

SPRZ292B, Jun. 2009
SPRZ295C, Dec. 2009

The end