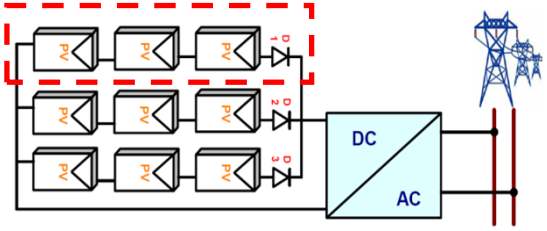
C2000 Solar Inverter Development Kits

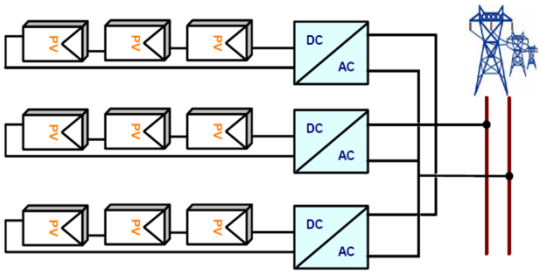
C2000 Digital Power System Applications Team

QUICK INTRODUCTION

Solar Inverter Types



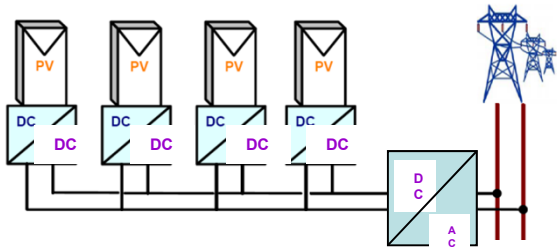
Central Inverter
DC/AC = DC/DC + DC/AC



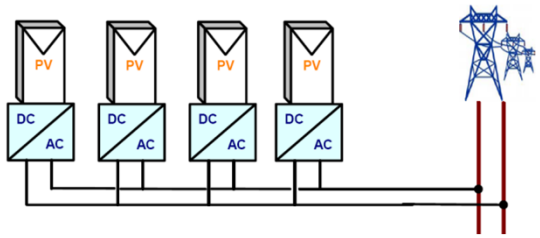
StringInverter
DC/AC = DC/DC + DC/AC

Traditional

Micro



Micro Converter
+
Central Inverter

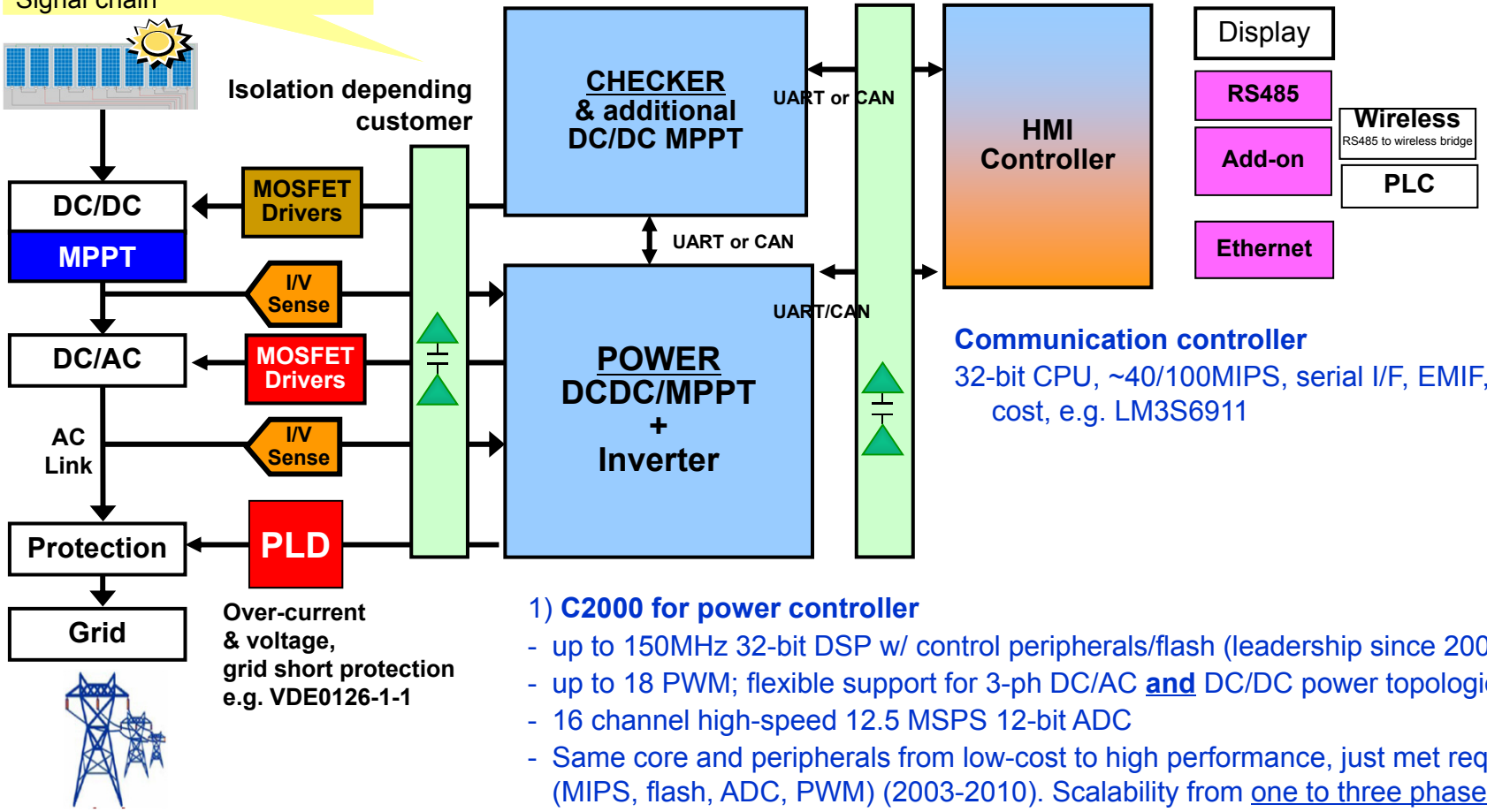


Micro Inverter

What Constitutes an Solar Inverter?

ISO55x + Topas
DS ADC w/ ISO AMC12xx
Maximizer: Helion
Signal chain

1) **C2000 as checker** to offload power control: DC/DC & MPPT



Communication controller
32-bit CPU, ~40/100MIPS, serial I/F, EMIF, flash, cost, e.g. LM3S6911

1) **C2000 for power controller**
- up to 150MHz 32-bit DSP w/ control peripherals/flash (leadership since 2003)
- up to 18 PWM; flexible support for 3-ph DC/AC **and** DC/DC power topologies
- 16 channel high-speed 12.5 MSPS 12-bit ADC
- Same core and peripherals from low-cost to high performance, just met requirements (MIPS, flash, ADC, PWM) (2003-2010). Scalability from one to three phase, or one to three string inverter.
- In production at customers since more than 10 years ago.

QUICK SNAPSHOT

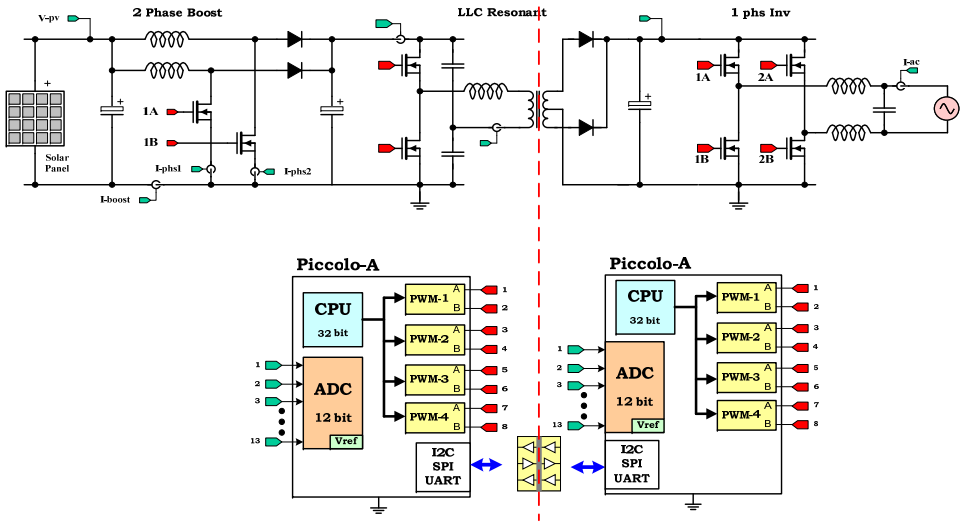
C2000 HV Solar Inverter Dev/Eval Kit

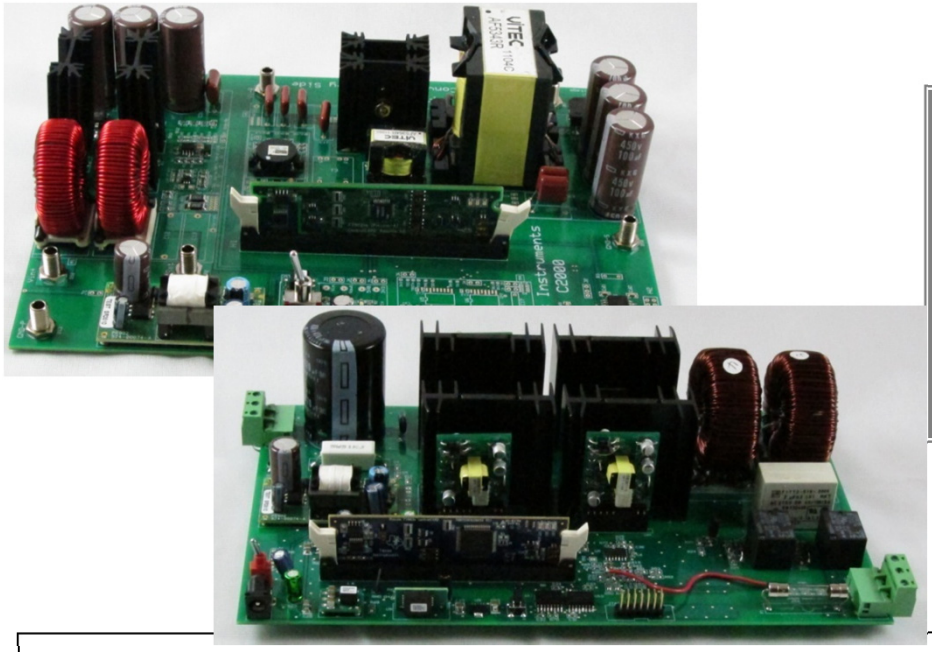
Description

- 200~400VDC input from PV array
- Isolated design ~ 500W (dual PCBs)
- Dual controllers (Pri / Sec)
- DCDC for MPPT (2 switch IL Boost)
- ISO-DCDC (Resonant LLC)
- Inverter (Full Bridge) - 120/240VAC Grid
- Host comms / Isolated JTAG

Markets / EEs

- Central Inverter, Micro Inv, Micro Conv





HW status

Proto 1Q TE 2Q EVM 3Q

SW deliverables

- Boost I-loop + MPPT V-Loop
- ISO Resonant DCDC V-loop (?)
- 1 phase I-mode Inverter with PLL

Quick Update on HV Kit Status

- DC/AC
  - Proto: Done
    - Schematic, PCB layout, BOM, PCB build all done
    - Initial h/w testing, e.g. life support circuits, current sensing circuits, driver circutis, etc. all done
    - Inititial I-loop testing done
    - Initial grid-tie testing done
  - Next 30-45 days
    - Finetune transient response, efficiency. Final s/w and algo
    - Final h/w including fixing current sensing circuit, adding PLC module, switching to iso JTAG module, etc.
- MPPT DC/DC
  - Pre-proto stage
    - First rev. schematic, PCB layout, BOM, and PCB build all done.
    - Initial h/w testing started, h/w including I loop working at 200V
  - Next 30-45 days
    - Complete h/w testing at full voltage and full load
    - Revised h/w if needed
    - Complete MPPT algo and testing

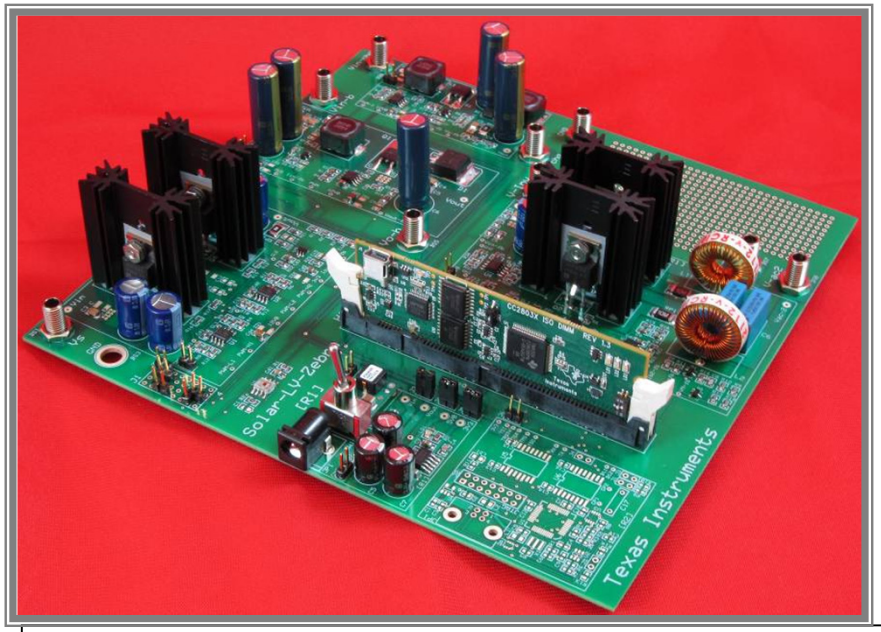
LV Solar Inverter with PV emulation

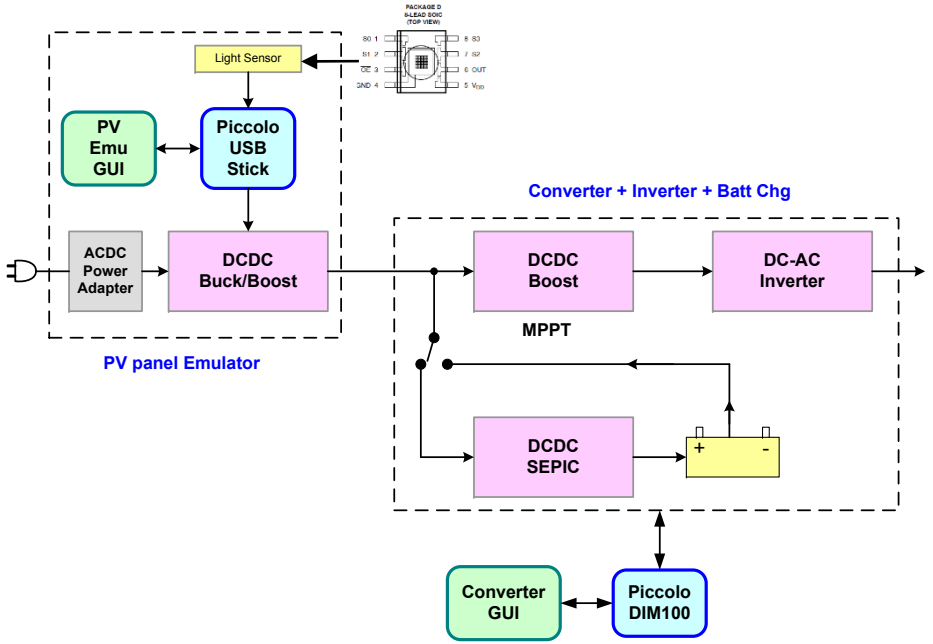
Description

- 12V DC input (for PV emulator)
- Non-isolated design ~ 100W
- PV emulator (Buck-Boost)
- DCDC for MPPT (1 switch Boost)
- Inverter (Full Bridge)
- Host comms / Isolated JTAG

Markets / EEs

- Central Inverter, Micro Inv, Micro Conv





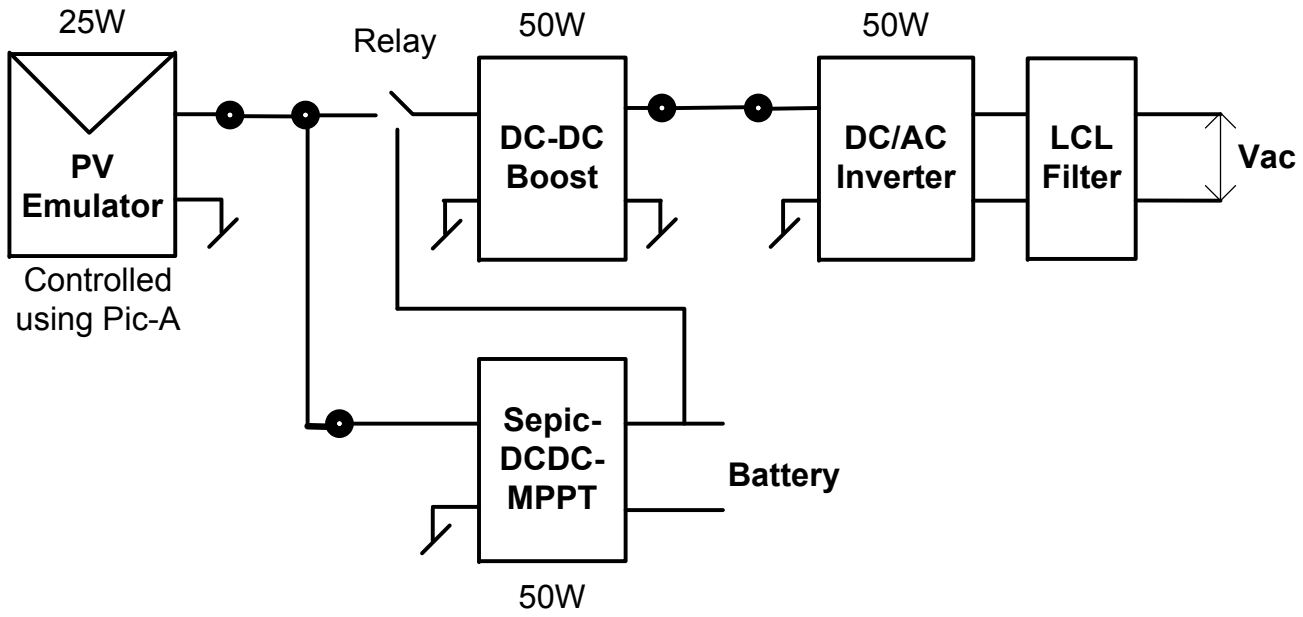
HW status

Proto ☑ TE 2Q EVM 2Q

SW deliverables

- Buck-Boost for PV emulation
- Boost I-loop + MPPT
- 1 phase Sine Inverter with PLL

LV Kit



Piccolo A

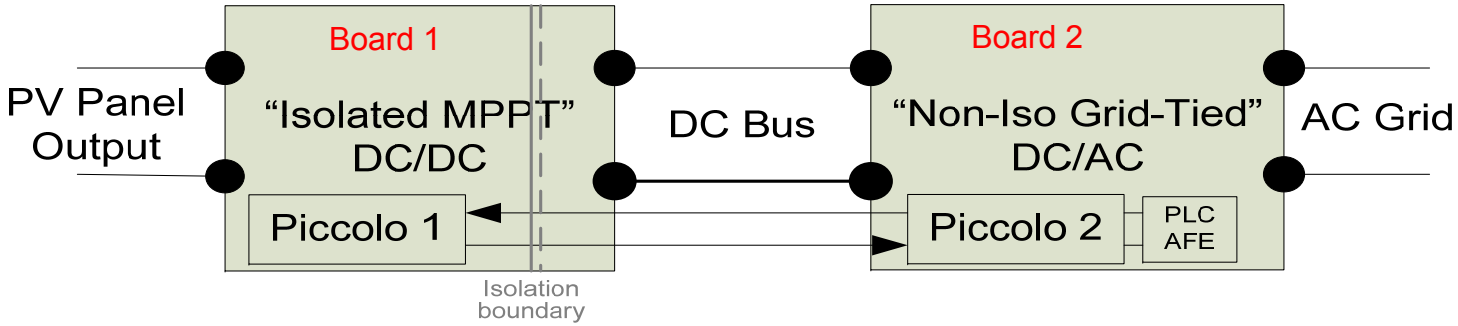
- PV Panel Emulator
  - Synchronous Buck-Boost
  - Input: 12V/5A
  - Output: 0-22V/0-3.5A
  - 50W
  - 200KHz (?)

Piccolo B

- Single-Phase DC/DC Boost
  - Input: 0-22V/0-3.5A
  - Output: 35V Nom (30-40V), 0-2A
  - 50W
  - 200KHz
- Battery Charger Sepic
  - Input: 0-22V//0-3.5A
  - Output: 12-16V, 0-3.5A
  - 50W
  - 200KHz
- Full-Bridge DC/AC Boost
  - Input: 35V/0-2A
  - Output: 24VAC Max, 0-2A
  - 50W
  - 10-20KHz

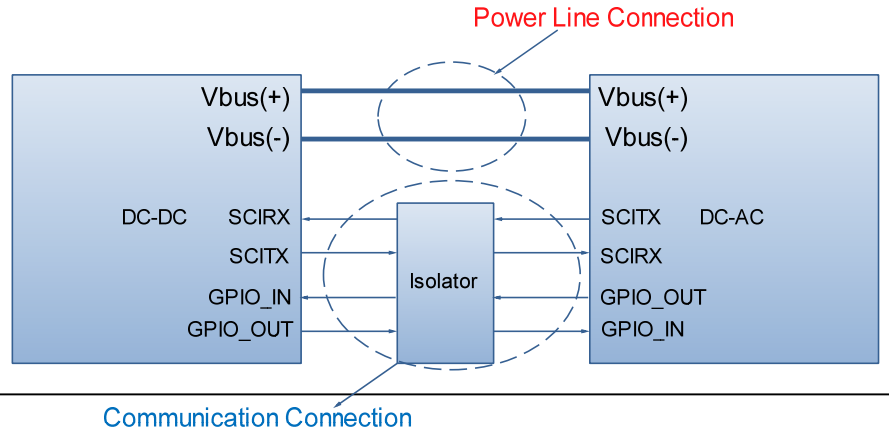
HV SOLAR KIT

Two-Board System Architecture



- Energy Transfer from PV Panel to DC Bus
- MPPT
- DC Bus Over Voltage Limiting
- Comm – SCI with Secondary, Isolated

- Energy Transfer from DC Bus to Grid
- DC Bus Voltage Regulation
- Grid Current Injection Regulation
- Grid Connect and Disconnect
- Comms – SCI with Primary, PLC with host

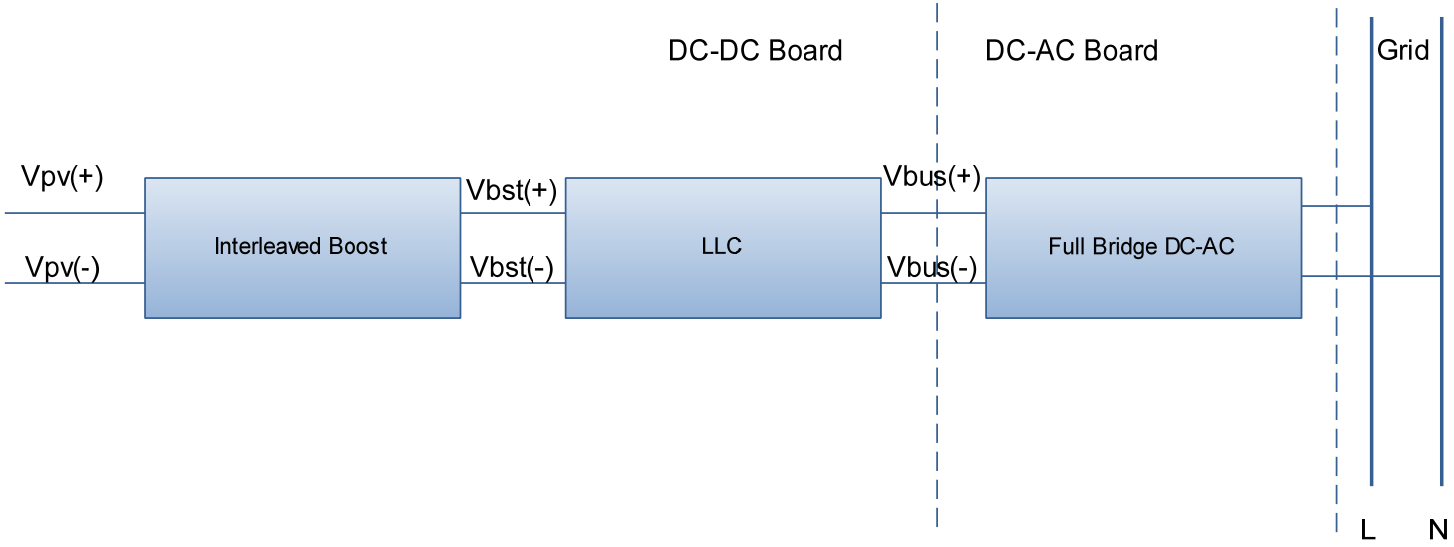


System Specification

- Input voltage rage, Vpv: 200-400VDC
- Maximum input voltage, Vpv_max: 450VDC
- Minimum input voltage, Vpv_min: 150VDC
- Maximum input power, Pin: 600W
- Nominal grid voltage, Vac_grid: 110 or 220VAC (may need different DC/AC modules for 110/220VAC)
- Maximum grid voltage, Vac_grid_max: Nominal+10%
- Minimum grid voltage, Vac_grid_min: Nominal-10%
- AC output frequency range, F: 50-60Hz, +-10%
- Maximum AC output current, Iac_max: 2.7A at 220VAC, 5.4A at 11VAC
- AC output power factor, PF: 1
- AC output THD, THD: <5%

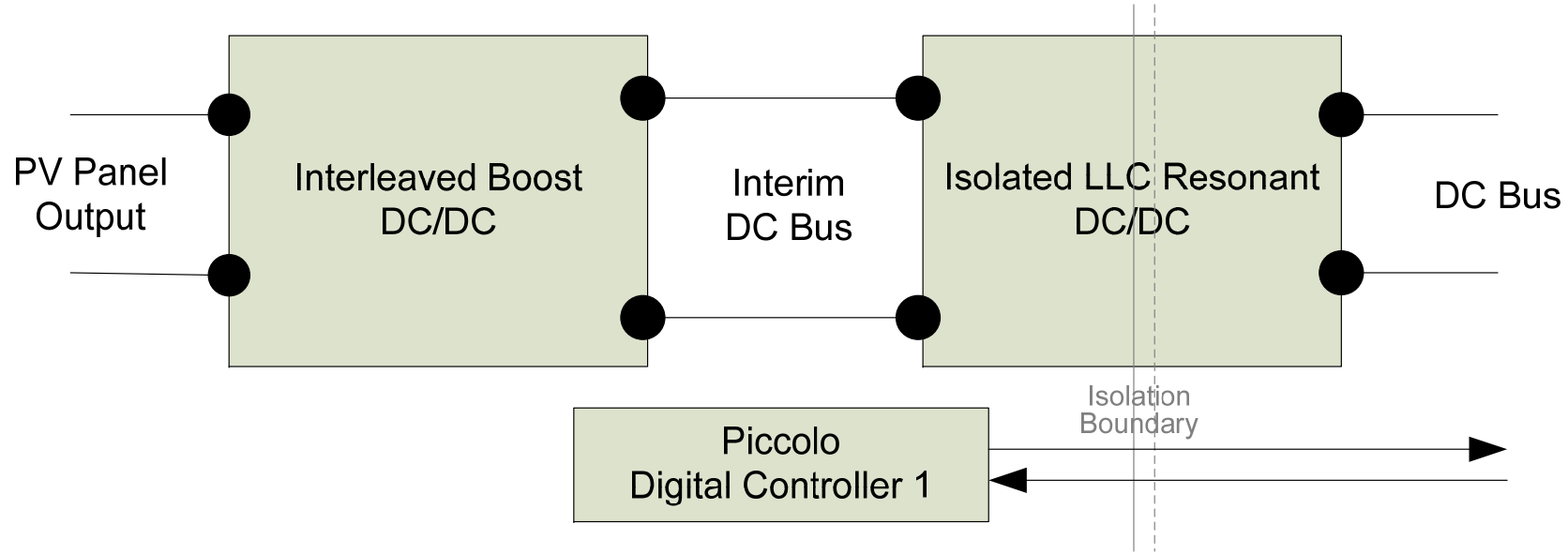
- Subject to changes
- Additional regulation compliance related specifications: TBD

Three-Stage Power Conversion



- Interleaved Boost for “Wide Input Voltage Range” and “Efficiency”
- Open-Loop Controlled Isolation Resonant LLC DC/DC for “Bypass-able” “Efficient” “Isolation”

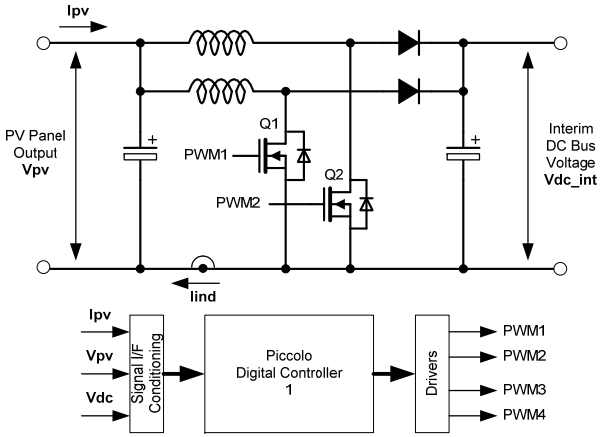
Isolated MPPT DC/DC



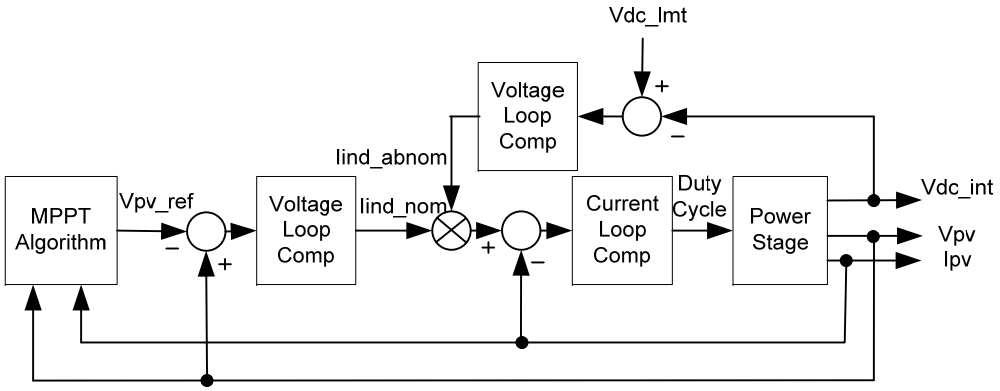
Isolated MPPT DC/DC

- DC/DC boost
- PV panel voltage and current regulation (<3%?)
- MPPT (98%?)
- DC bus over voltage limiting (<5% ripple?) under no load
- For isolation only, open-loop controlled with transfer ratio of 1:1

Interleaved Boost DC/DC for MPPT



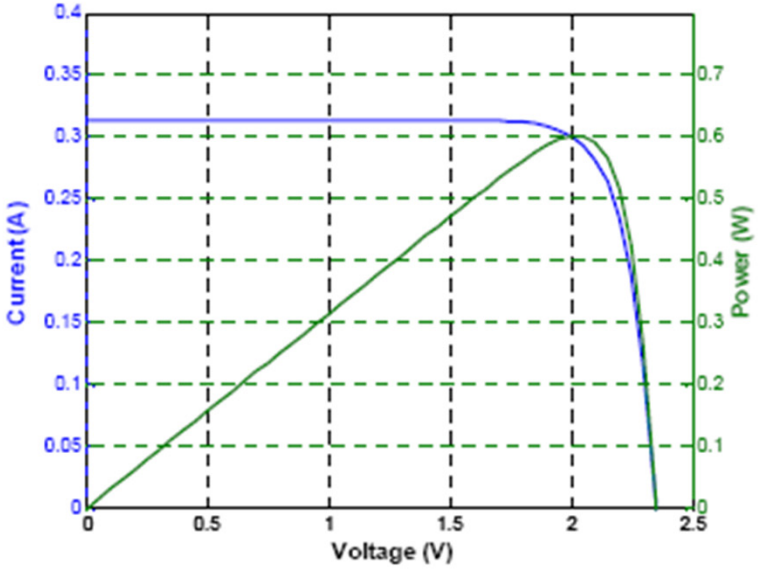
Interleaved boost DC/DC



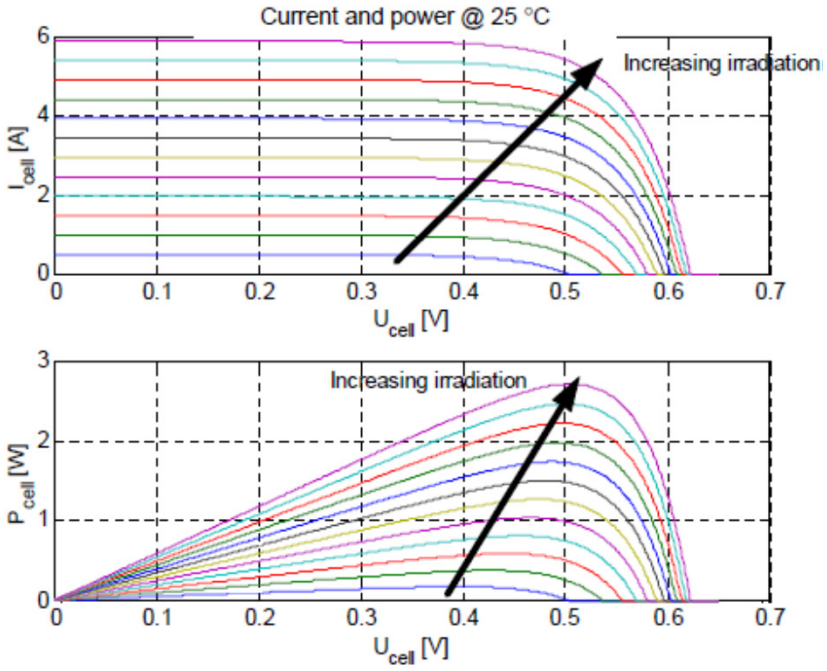
Interleaved boost DC/DC Control Block Diagram

- Inner Control Loop – Average Inductor Current Control Per Outer Loop Determined Reference
- Outer Control Loop 1 – PV Voltage Control Per MPPT Algorithm Determined Reference, in Normal Operation
- Outer Control Loop 2 – DC Bus Voltage Limiting When Bus Voltage Shoots Up, In Bus Voltage Protection Mode
- Only one current sensor (for Iind) is needed. Ipv is determined by low-pass filtering Iind
- Iind_abnom is “1” in normal mode; Iind_abnom is “1” in abnomal mode.

PV Panel Characteristics and MPPT

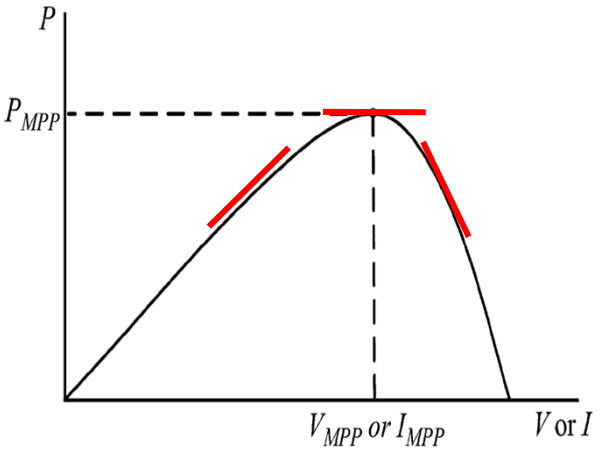


The *i-v* and *p-v* characteristics of the dual junction cells at 28° and 1000 W/m2.

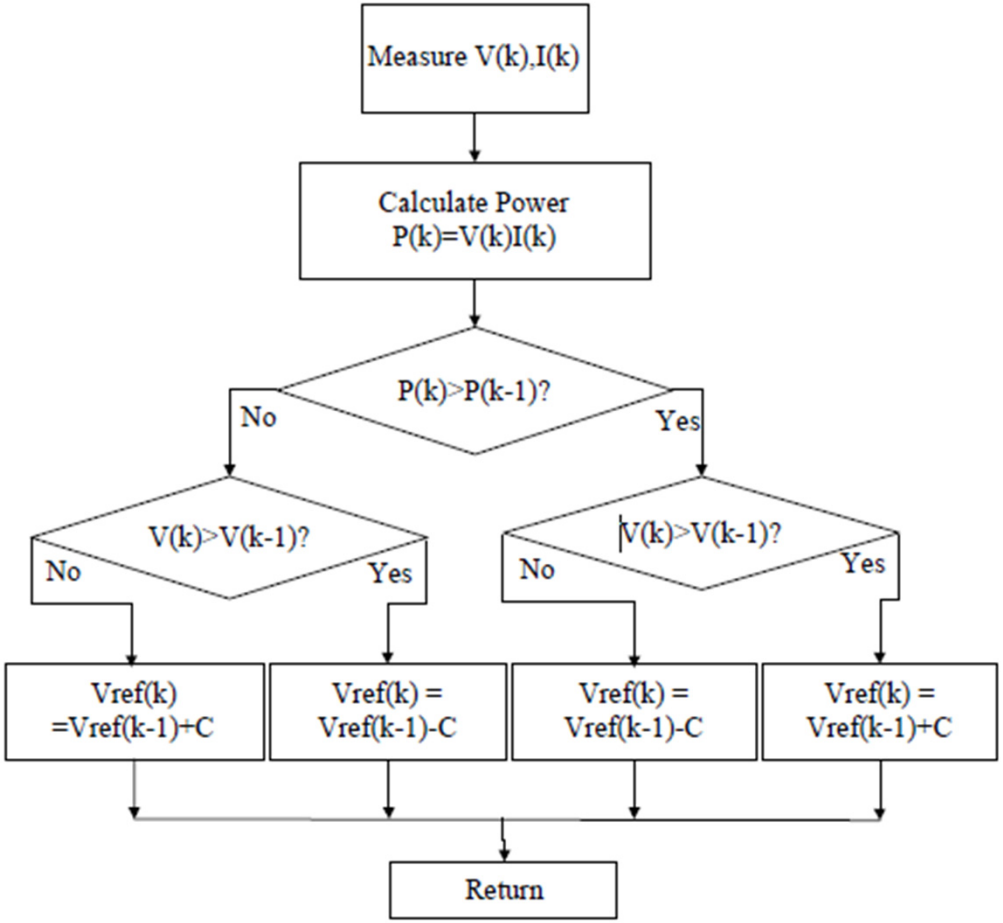


- Curve moves with lighting condition and temp and etc. So, does MPP
- So, it's necessary to always regulate PV panel output voltage and current to track MPP (MPPT)

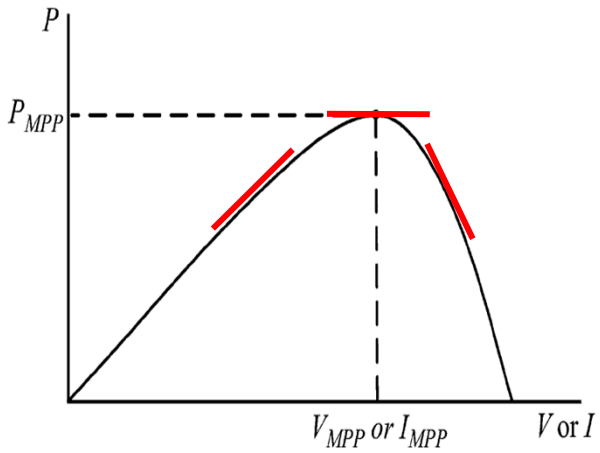
MPPT Algorithm 1 – Perturb &Observe



- Continue disturbing alongdirection of positive gradient
- Change disturbance direction when gradient becomes negative
- Step size and oscillation, local and global maxima (sweeping), etc.



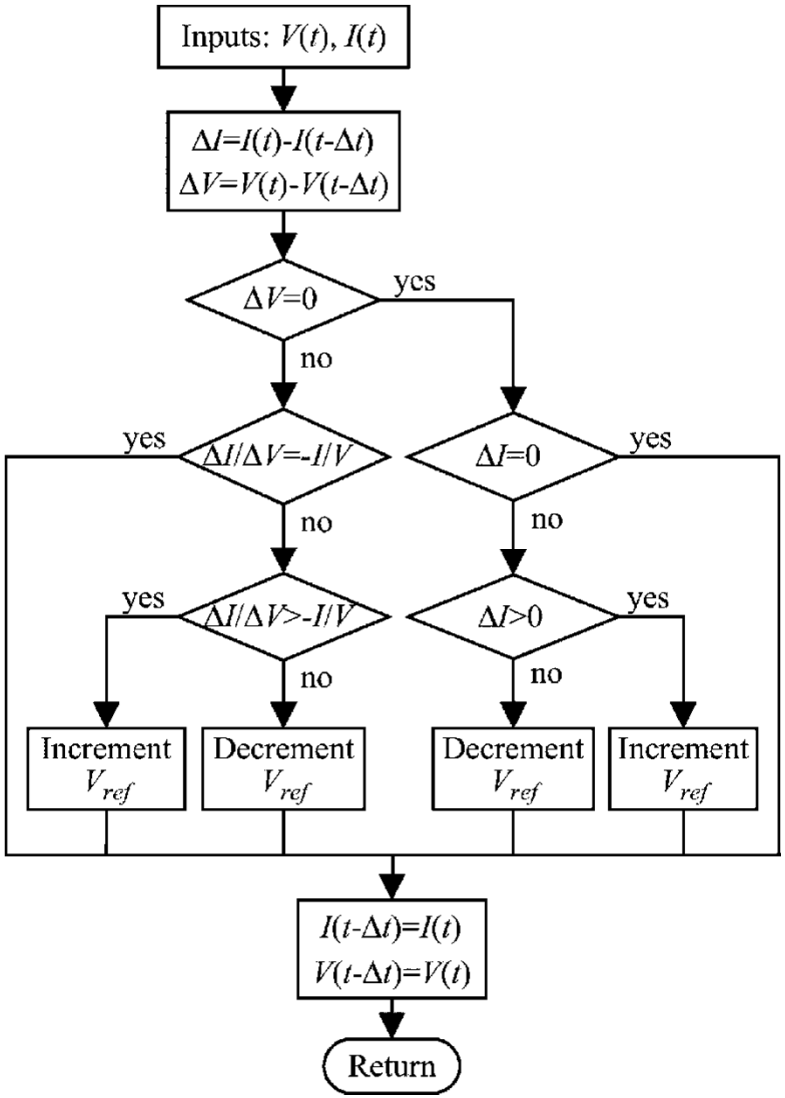
MPPT Algorithm 2 – Incremental Conductance



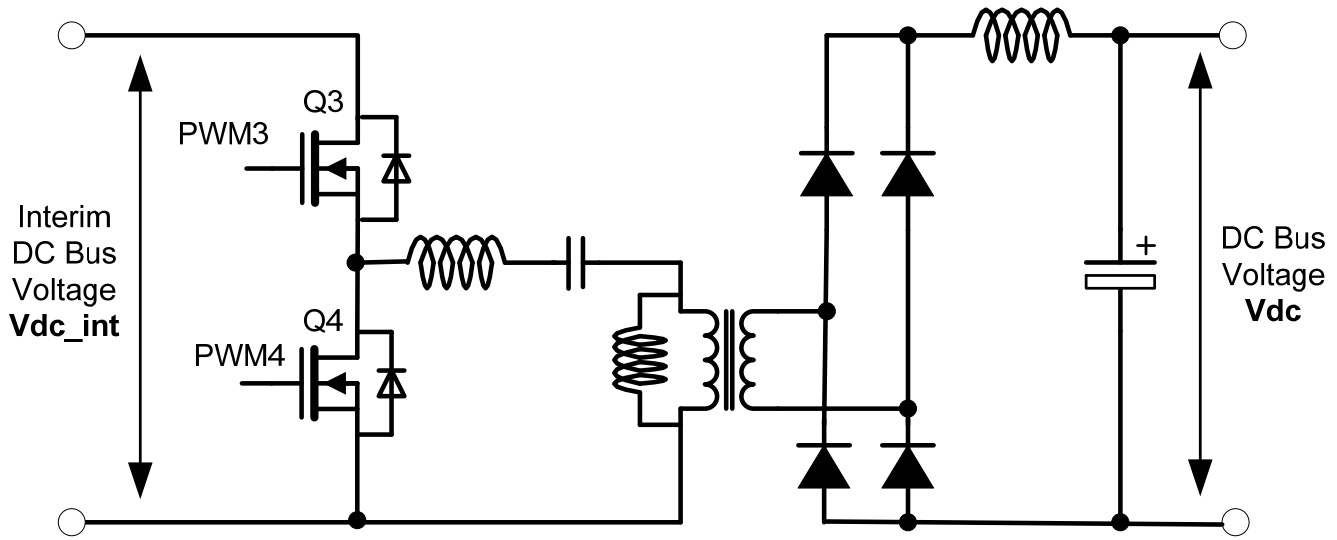
$$\frac{dP}{dV} = \frac{d(IV)}{dV} = I + V\frac{dI}{dV} \cong I + V\frac{\Delta I}{\Delta V}$$

$$\begin{cases} \Delta I/\Delta V = -I/V, & \text{at MPP} \\ \Delta I/\Delta V > -I/V, & \text{left of MPP} \\ \Delta I/\Delta V < -I/V, & \text{right of MPP.} \end{cases}$$

- Move per determined MPP direction
- Step size and oscillation, small voltage delta, local and global max (sweeping), etc.



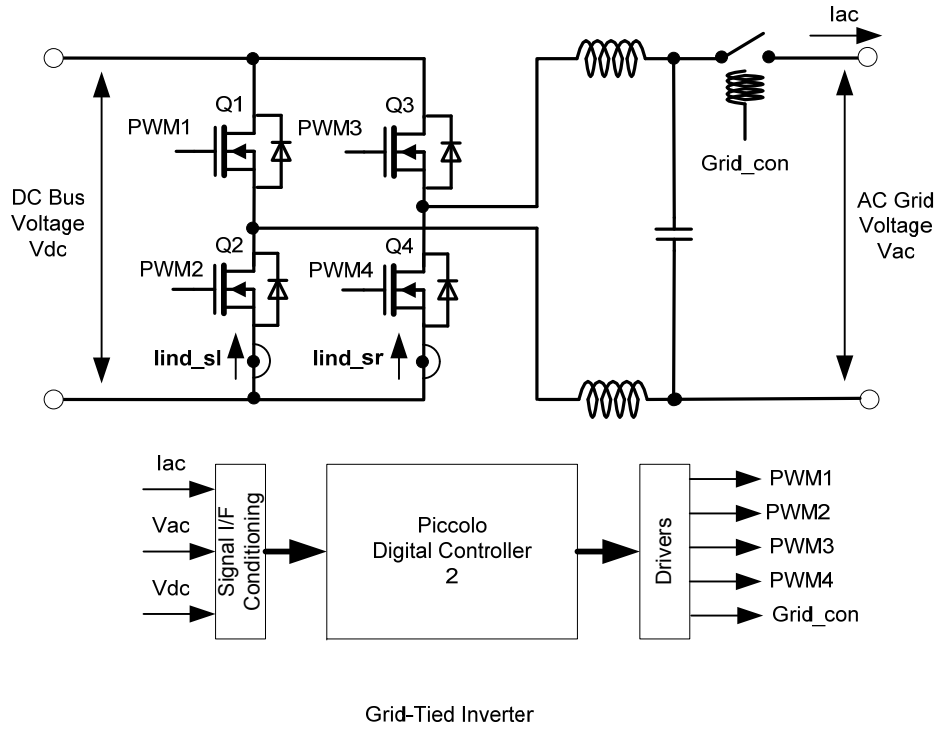
Isolated LLC Resonant DC/DC



Isolated LLC Resonant DC/DC
(The output inductor may not be necessary.)

- Diode Based Rectifier vs. MOSFET Based Synchronous Rectifier
- 1:1 Transfer Ratio
- Open-Loop Control

Grid-Tied DC/AC



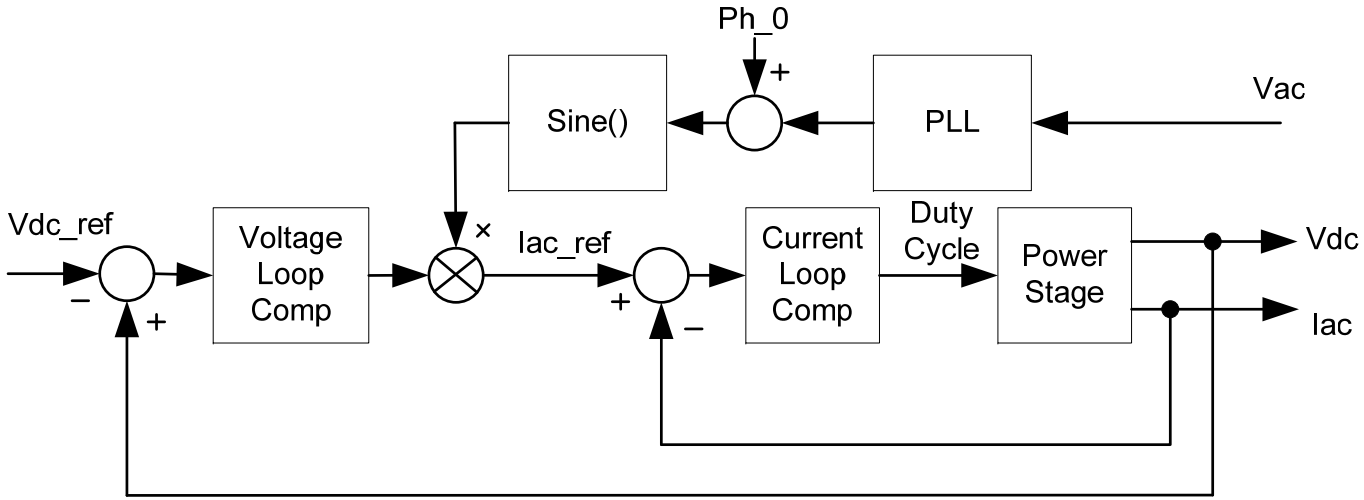
Grid-Tied Inverter

- By maintaining DC bus voltage constant, transfers all PV panel output to grid
- Inductor Current Sensing
  - Low-Cost Shunts
  - Iac Derived from Iind by Low-Pass Filtering
- Vs. CT or Hall based approach

- DC/AC Conversion
- DC Bus Voltage Regulation (3%?)
- PLL wrt Grid Voltage

- Grid Current Injection Regulation
  - Shape Per PLL w/ Phase Offset (Reactive Power), or Grid Voltage (Through Mode)
  - Magnitude per DC Bus Voltage Loop

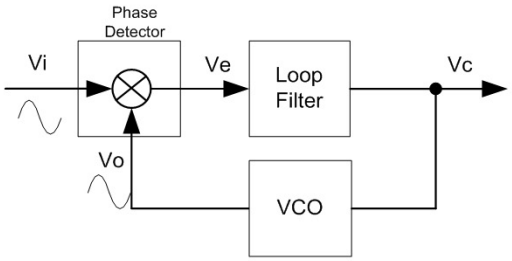
Grid-Tied DC/AC Control

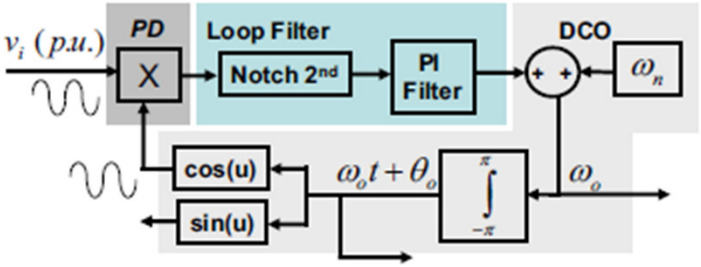


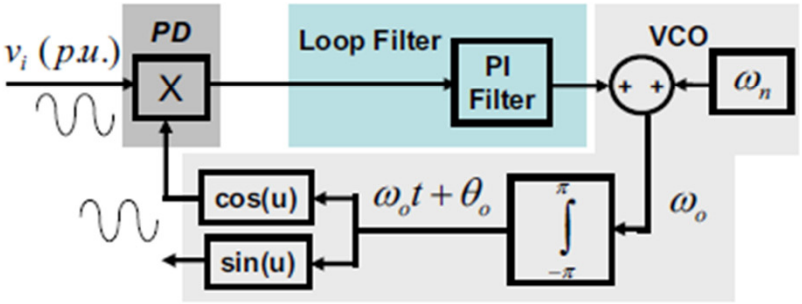
Grid-Tied DC/AC Control

- Inner Control Loop – Average Inductor Current Control Per Outer Loop Determined Ref
- Outer Control Loop – DC Bus Voltage Control Per Set Ref and Determined Freq and Phase
- Phase angle injection and reactive power, feed-through mode
- System Protection Shut Down – If Vdc < Vdc_lmt_low, shut down DC/DC and DC/AC

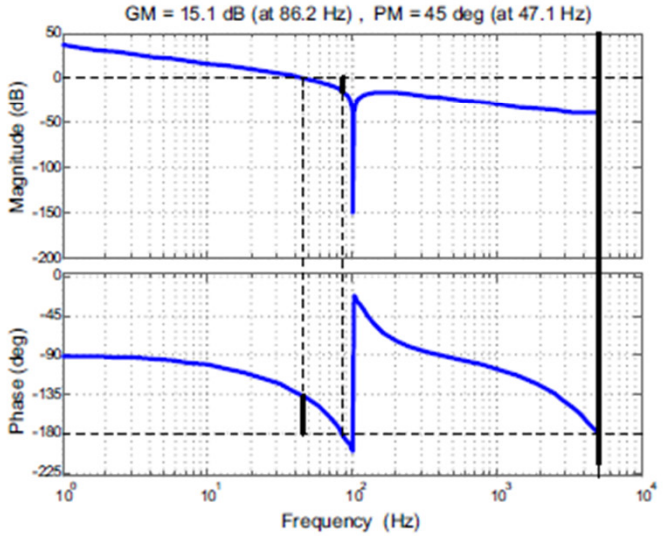
Phase-Locked Loop







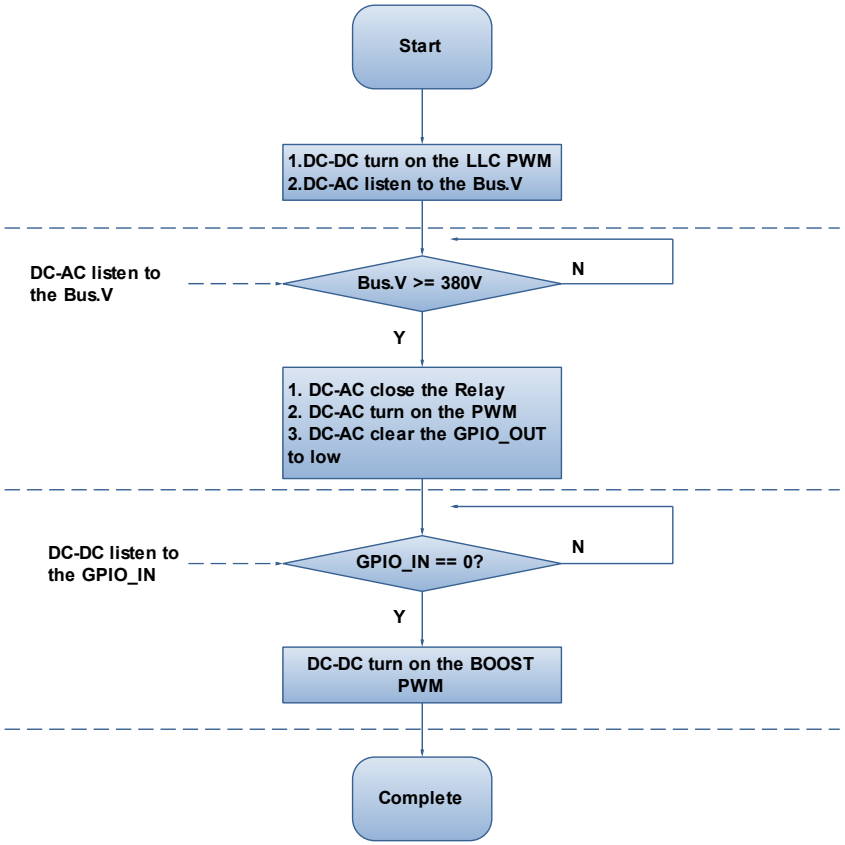
$$v_i \times \underbrace{\cos(\omega_o t + \theta_o)}_{Feedback\ wave} = \frac{1}{2}\sin(\omega_i t + \theta_i - \omega_o t - \theta_o) +$$
$$+ \frac{1}{2}\sin(\omega_i t + \theta_i + \omega_o t + \theta_o) + f(2\omega_i, 4\omega_i, 6\omega_i, \ldots)$$

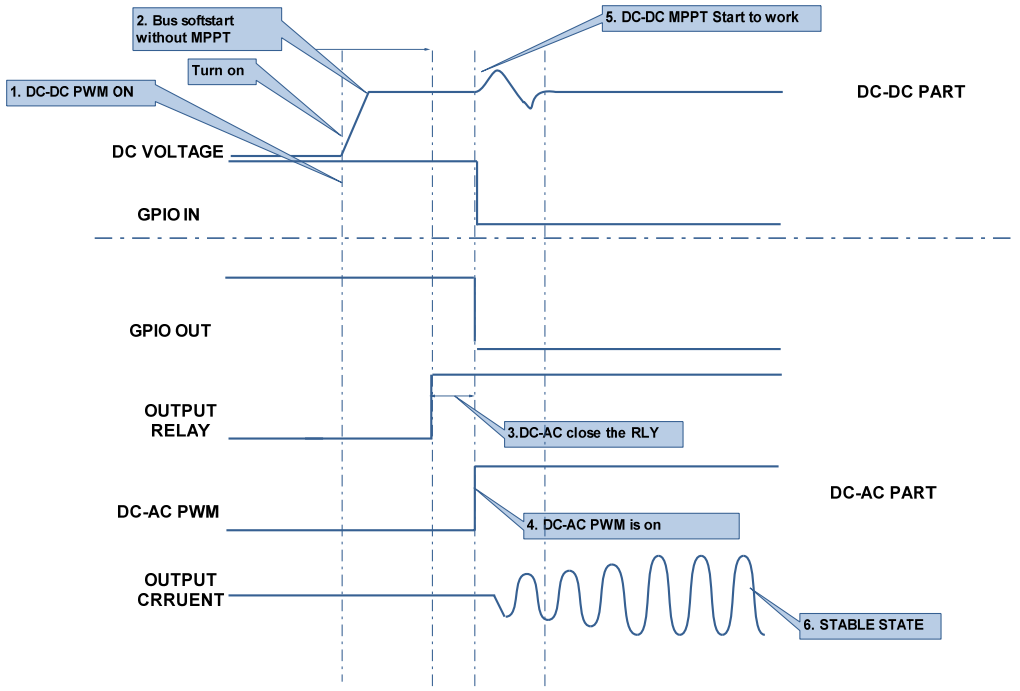


- 2nd Harmoinc in Error and Control Signal
- Notch (2nd) Filter Used to Filer Out 2nd Harmonic

- Other Methods
  - Zero-Crossing Detection
  - d-q Method for Three-Phase

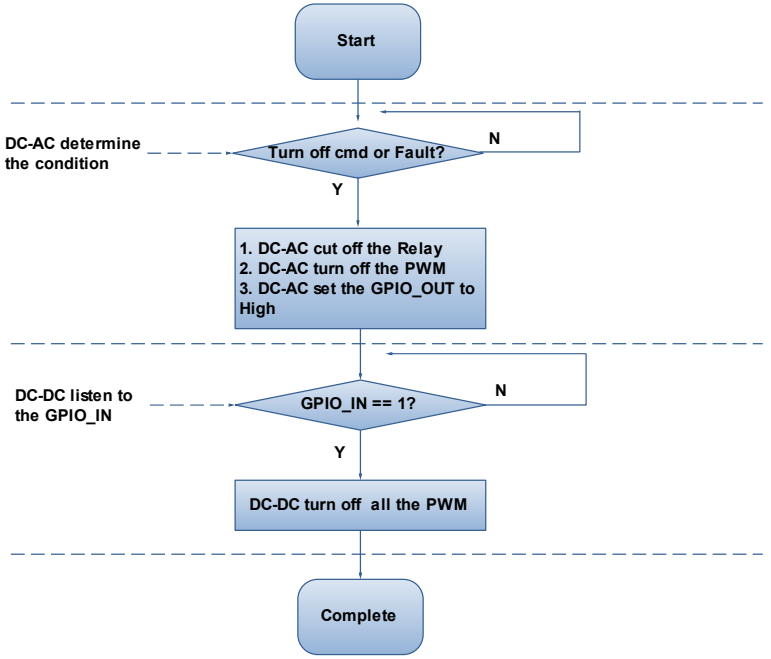
Power Up Sequence

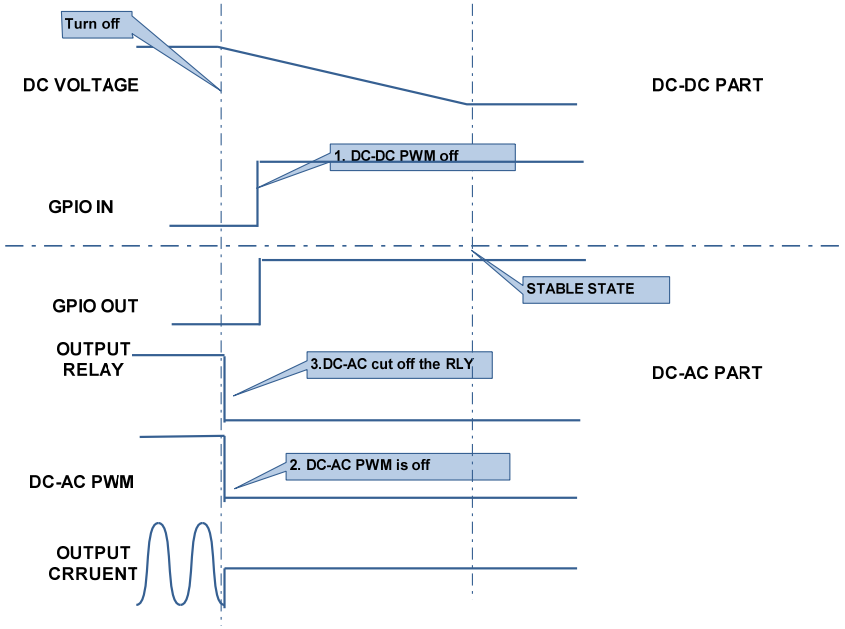




- DC/DC stage can't not operate in MPPT mode without pumping generated power to grid
- For MPPT to be one, DC/AC must be working in normal mode

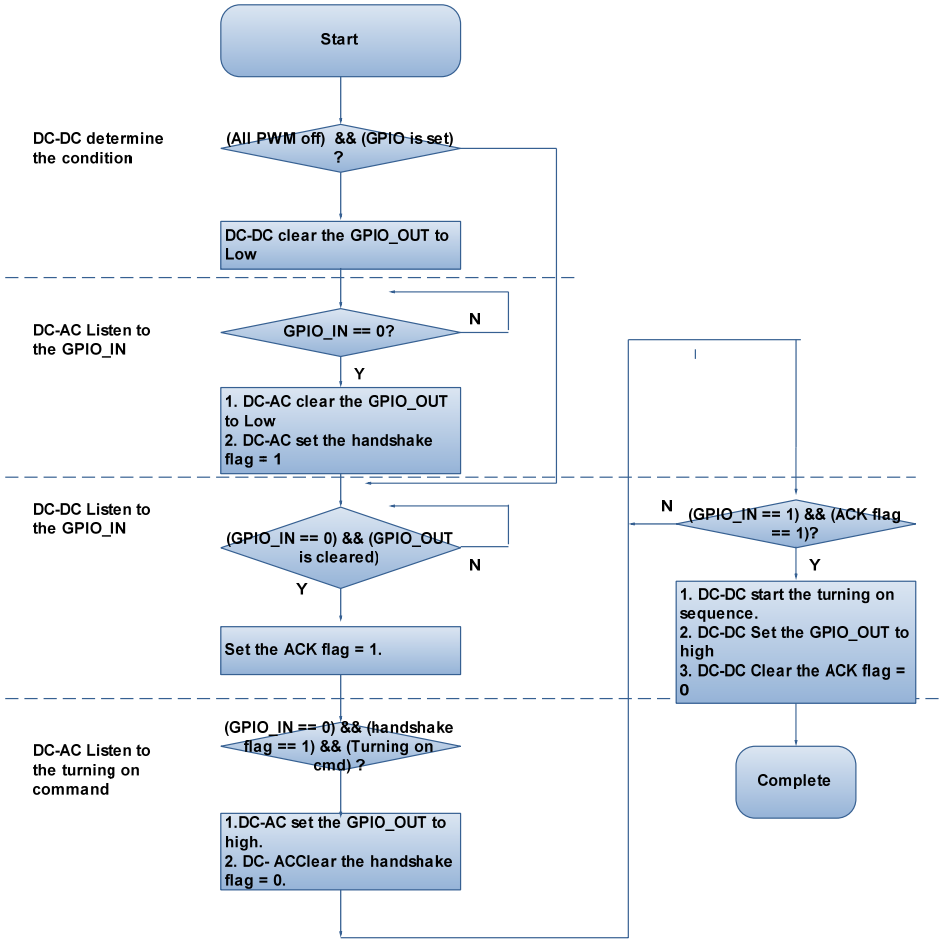
Shut Off Sequence

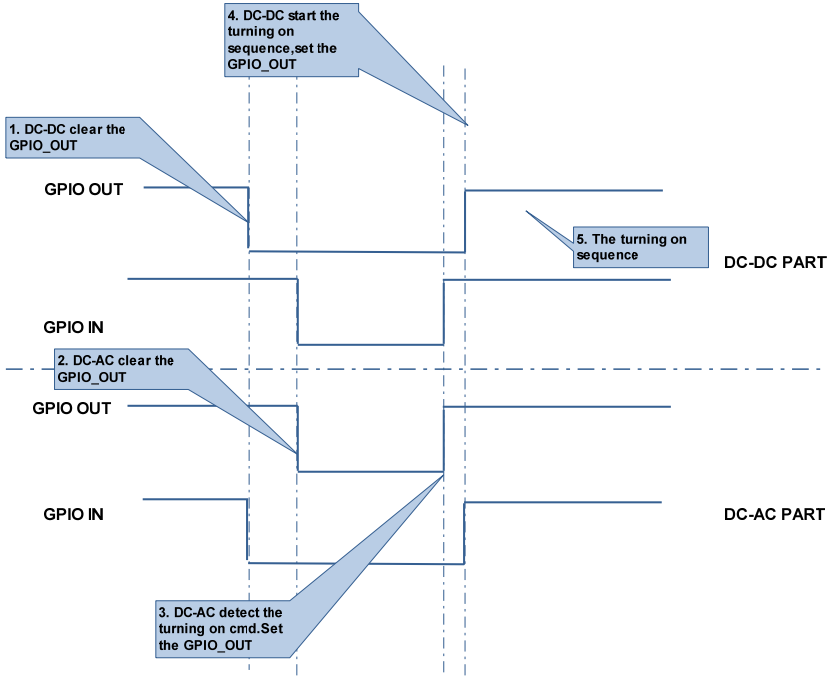




- DC/DC stage can't not operate in MPPT mode without pumping generated power to grid
- For MPPT to be one, DC/AC must be working in normal mode

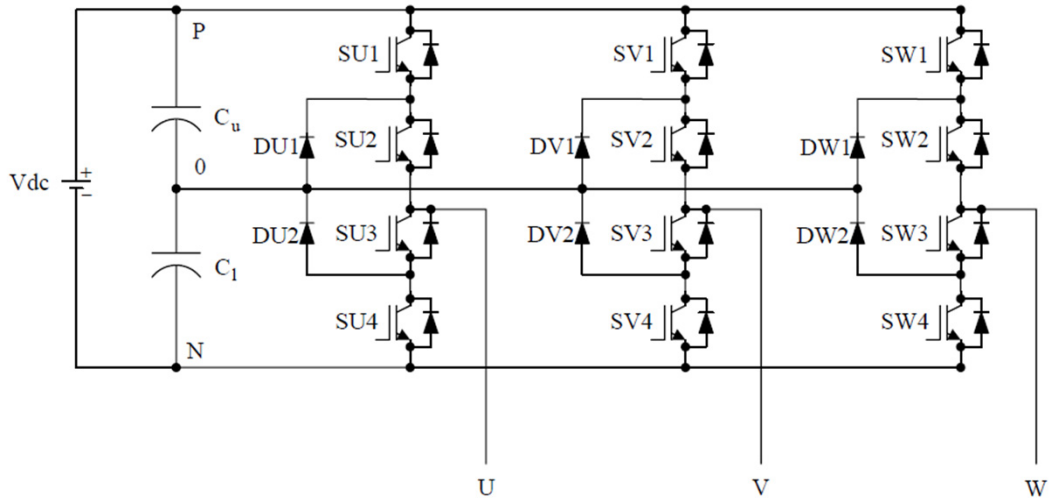
Restart Proposal





- DC/DC stage can't not operate in MPPT mode without pumping generated power to grid
- For MPPT to be one, DC/AC must be working in normal mode

Other DC/AC Inverter Topologies



- Multi-level (3, 5, …) topologies are commonly used in high voltage/power inverters
- Multi-level topologies require
  - More PWMs, e.g. three-level three phase inverter typically requires 12 PWMs vs 6 for regular (two-level) inverter
  - More complex PWM waveforms
  - More operational, or energy transfer, modes, e.g. more Vout levels, pos and neg half cycles, neutral point control
- Current and Voltage Loops Are Similar, Just More Energy Transfer Modes

Anti-Islanding And Operation Modes

As a grid tied solar inverter, it's required to disconnect from the grid when there is a power outage per specific regulation requirements. This is called anti-islanding. Another way to look at this is YOU DON'T Your Inverter to Electrocute the Technician Servicing the Grid.

- Detection of Islanding
  - Under/over Voltage and Under/over Frequency
  - Voltage Phase Jump Detection
  - Detection of Voltage Harmonics
  - Impedance Measurement
  - Detection of Impedance at Specific Frequency
  - Slip Mode Frequency Shift
  - Frequency Bias
  - Sandia Frequency Shift
  - Sandia Voltage Shift
  - Frequency Jump
  - Etc.
  - Other Methods
- Anti-Islanding Test Methods
  - IEEE Std. 929-2000, UL1741
  - International Standard IEC62116

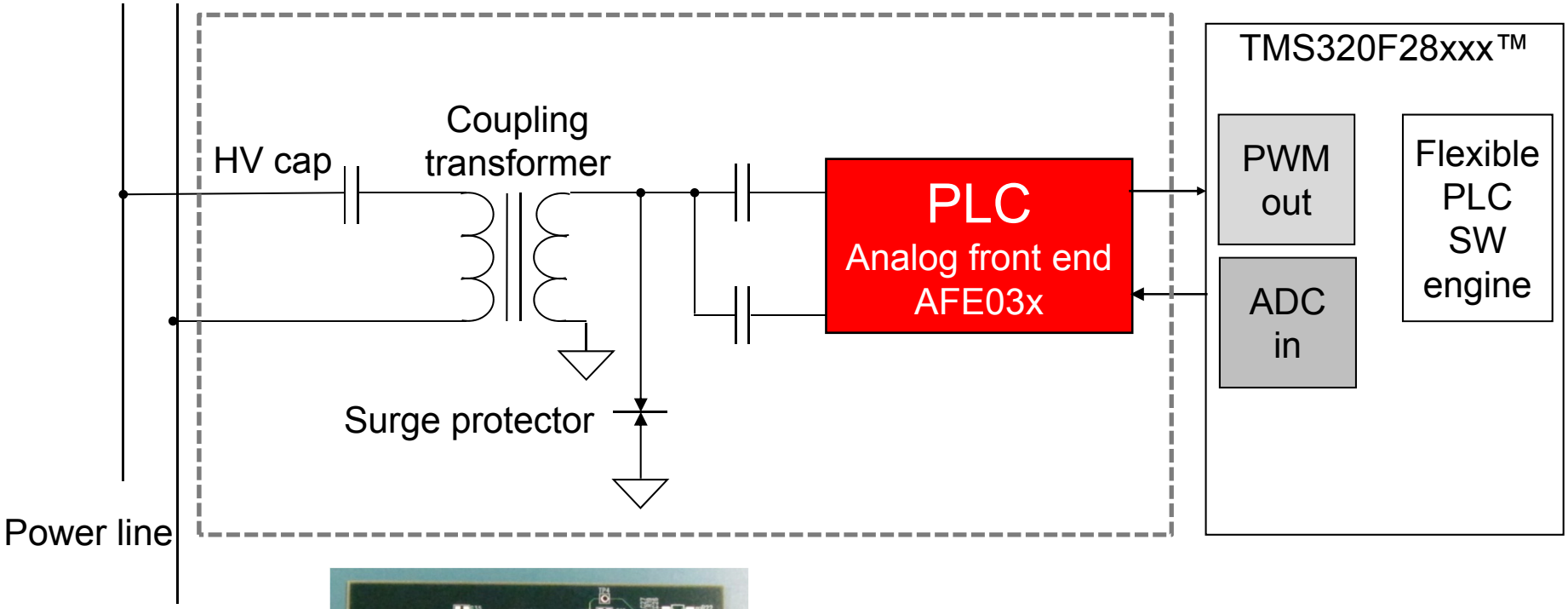
- Connect, Disconnect Condition Detection
- Connect, Disconnect Action Execution

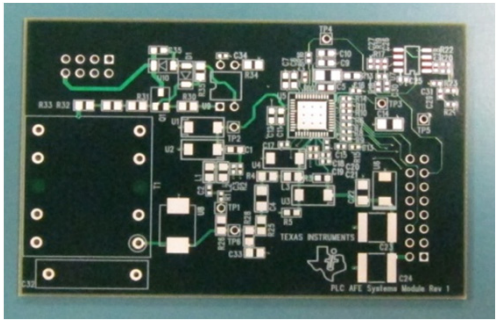
- Regulation Dependent
- System Supervision
- First Priority Is Connect and Disconnect Operation
- We will Only Implement Some Anti-Islanding Functions

Anti-Islanding and Operation Control Variables and Parameters

- Threshold voltage, Vac_off, for grid off detection
- Time length,Tac_off, for grid off detection
- When grid AC voltage is lower than Vac_off for Tac_off or longer time, s/w will assume the grid is off.
- Hold-up time, Thold.
- After grid off is detected, the inverter will stay connected for Thold amount of time.
- Shut off time, Tshut.
- The inverter must be shut down in Tshut amount of time after grid off is detected.
- Threshold voltage, Vac_on, for grid on detection
- Time length, Tac_on, for grid on detection
- When grid AC voltage goes back above Vac_on for Tac_on or longer time, s/w will assume the grid is back up.
- Threshold phase error, Pherr
- Threshold frequency error, Ferr
- Rms Voltage and Current, Harmonics, etc.

PLC





AFE031 Based PLC Module ⟷ F28xxx ControlCard

- Options of PLC-Lite (Piccolo B or Octave based) or Prime/G3 (Octave only)

Solar Library

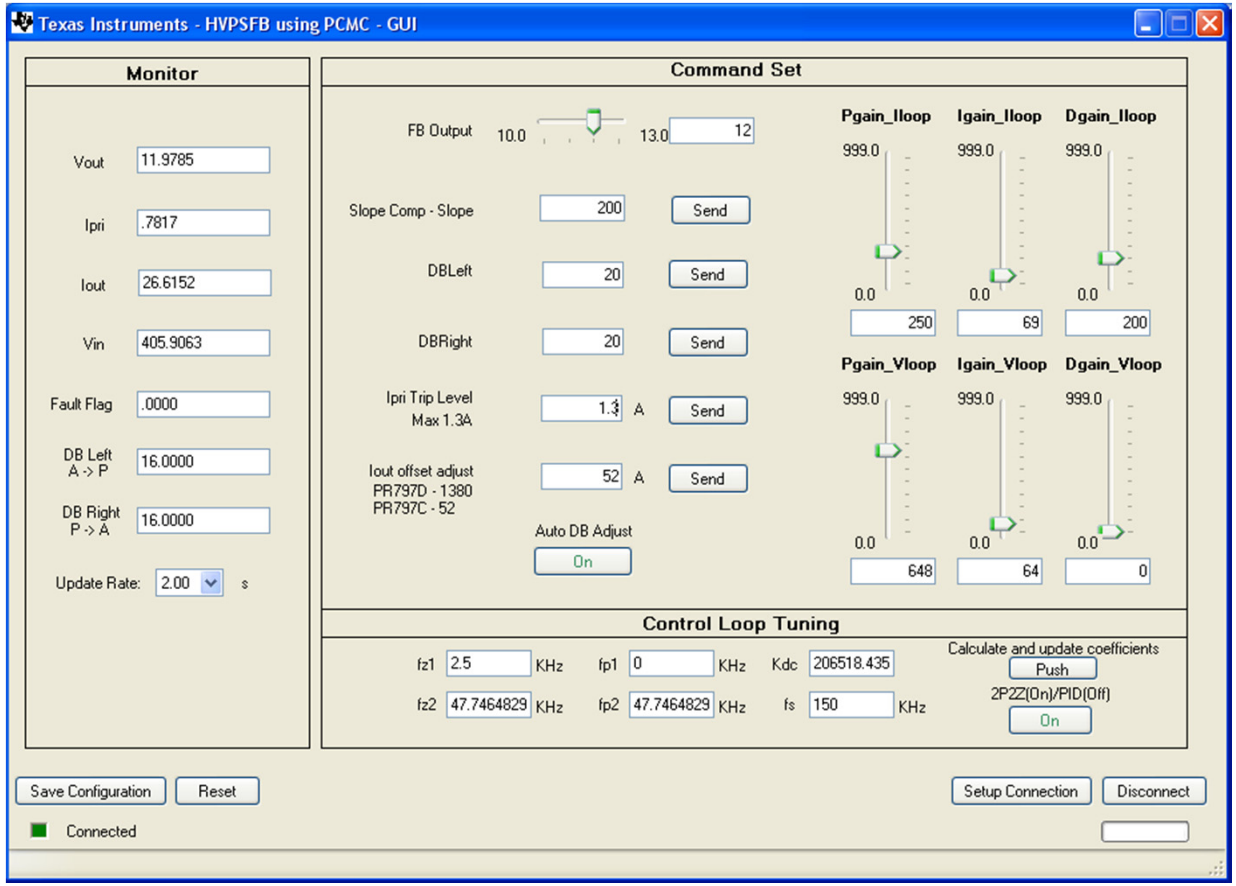
- MPPT DC/DC Stage
  - MPPT
    - P&O
    - Inc Conductance
  - MPPT DC/DC PWM Driver, LV
  - MPPT DC/DC PWM Driver, HV (or I/L)
  - MPPT DC/DC ADC Driver, LV
  - MPPT DC/DC ADC Driver, HV
  - MPPT DC/DC Control
  - Etc.

- Inverter
  - Inverter PWM Drivers
    - Unipolar
    - Bipolar
  - Inverter ADC Driver, LV
  - Inverter ADC Driver, HV (or Shunts Based)
  - Voltage and Current Analyzers
    - Freq, Avg, RMS
    - Rectifiefd Input, Bipolar Input
  - Grid Frequency and Phase Tracking
    - ZCD Based
    - PLL Based
    - d-q Baed In the Future (for Three-Phase)
  - Inverter Control
    - LV
    - HV

Most functions will be deployed when the kits are released to market late 2Q.

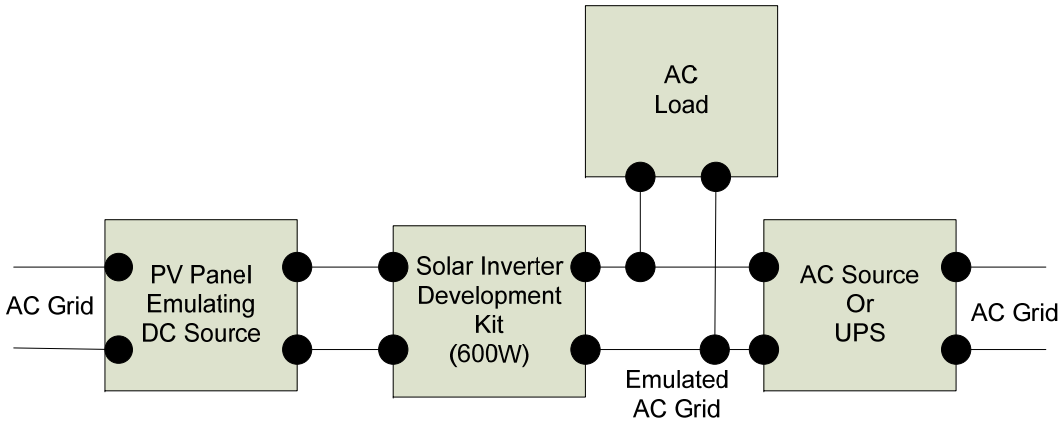
Selected functions such as MPPT algorithms, PLL, and drivers etc. will be available earlier in draft format.

Demo/Debug GUI



- GUI Used In Other Power Supply Dev/Eval Kits. Similar GUI Will Be Used Here.

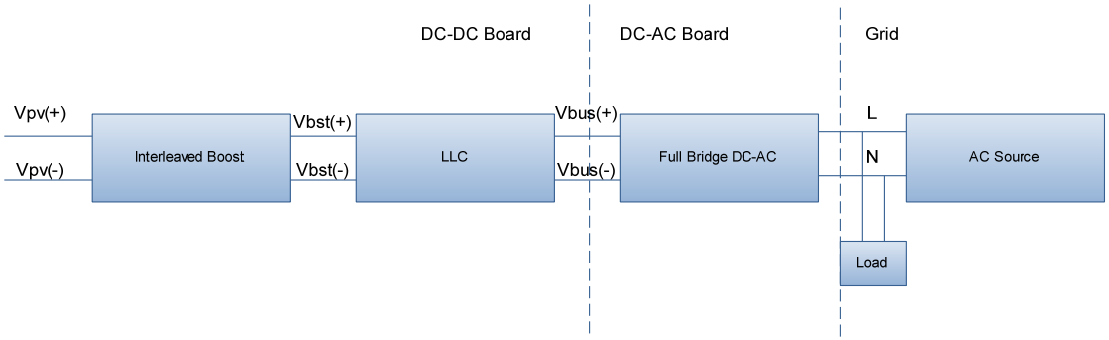
System Testing and Demonstration

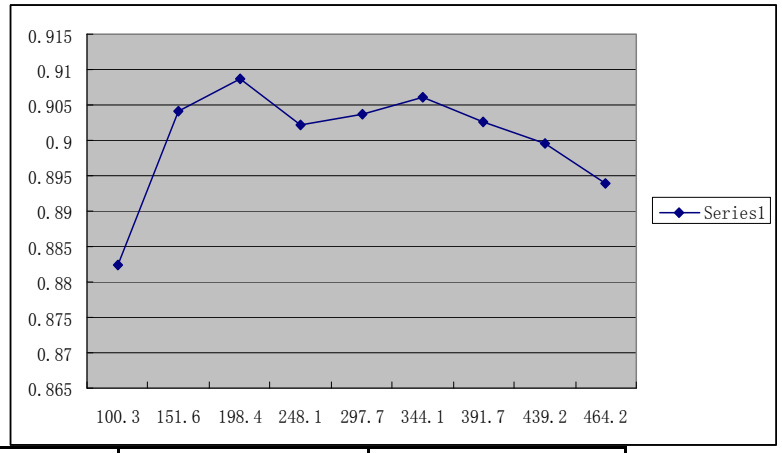


Solar Inverter Development Kit Test Setup

- UPS + Resistor Bank As Grid Emulator
  - System Functions
  - MPPT
  - No Load, by Disconnecting Both
- AC Source (In Constant Voltage Mode) + Resistive Bank As Grid Emulator
  - System Functions
  - MPPT
  - No Load, by Disconnecting Both
  - Grid Characteristics, Depending on AC Source Used
- AC Source (In Constant Voltage Mode) + AC Load As Grid Emulator
  - System Functions
  - MPPT
  - No Load, by Disconnecting Both
  - Grid Characteristics, Depending on AC Source Used
  - Variable Load Including Under Load

Initial Test Results – Efficiency





V_bus	Inv V_out	Inv P_out	Panel_V_out	Panel_I_out	Panel_P_out	Efficiency
376	119.5	100.3	203	0.56	113.68	0.882301196
376	119.8	151.6	207	0.81	167.67	0.904156975
376	119.2	198.4	212	1.03	218.36	0.908591317
376	119.5	248.1	214	1.285	274.99	0.902214626
376	119.8	297.7	216	1.525	329.4	0.90376442
376	120.1	344.1	217	1.75	379.75	0.906122449
376	119.6	391.7	217	2	434	0.902534562
376	119.9	439.2	217	2.25	488.25	0.899539171
376	120	464.2	221	2.35	519.35	0.89380957

3.5mH Output Inductor

Initial Test Results – Efficiency

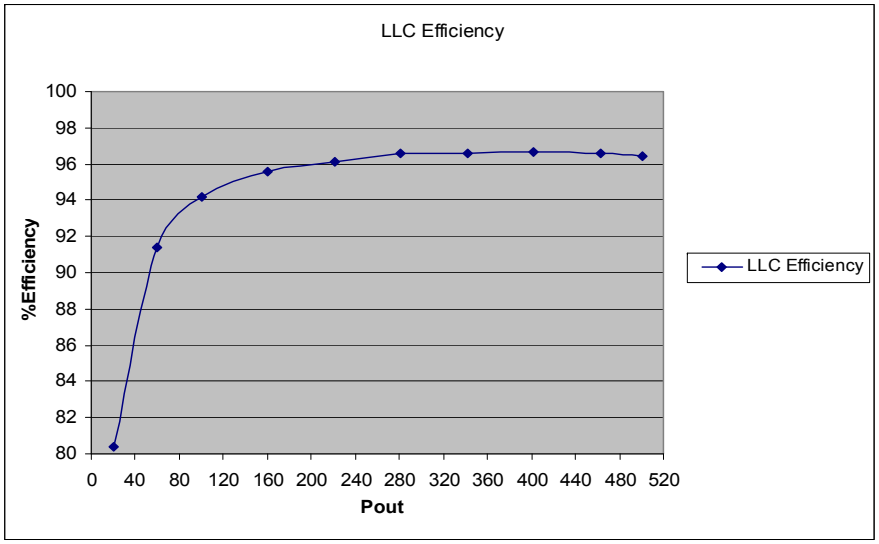
V_bus	Inv V_out	Inv P_out	Panel_V_out	Panel_I_out	Panel_P_out	Efficiency
376	120	306	207	1.62	335.34	0.91250671
376	120	470.8	221	2.35	519.35	0.906517763

2.5mH Fe-Si Output Inductor

DC/DC Efficiency

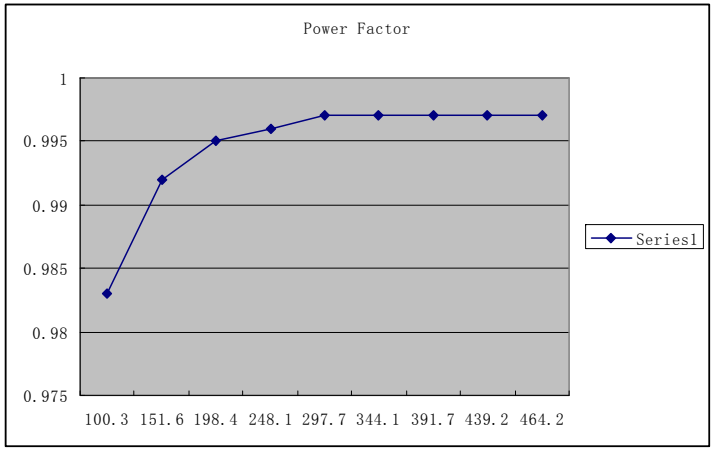
Frequency	Vout	Rload	Pout	Vin	Iin (A)	Pin (W)	Eff
100000	400.3	399.9	400.7004	203.93	2.008	409.49144	0.97853181
100000	393.7	333.5	464.766687	203.93	2.324	473.93332	0.98065839
100000	399	333.5	477.364318	349.5	1.387	484.7565	0.984750731

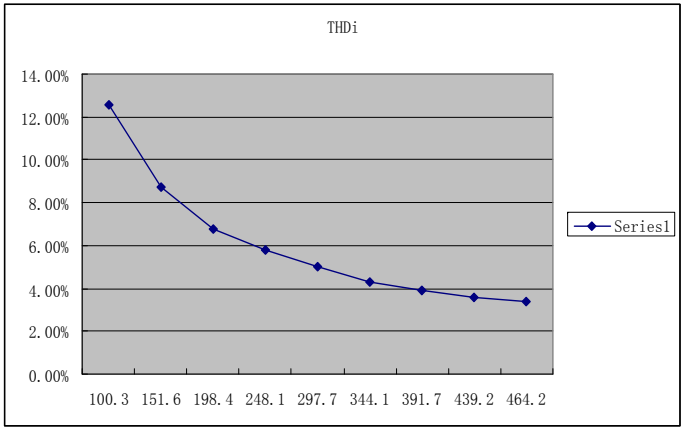
Boost DC/DC Efficiency



Initial Test Results – PF and THD

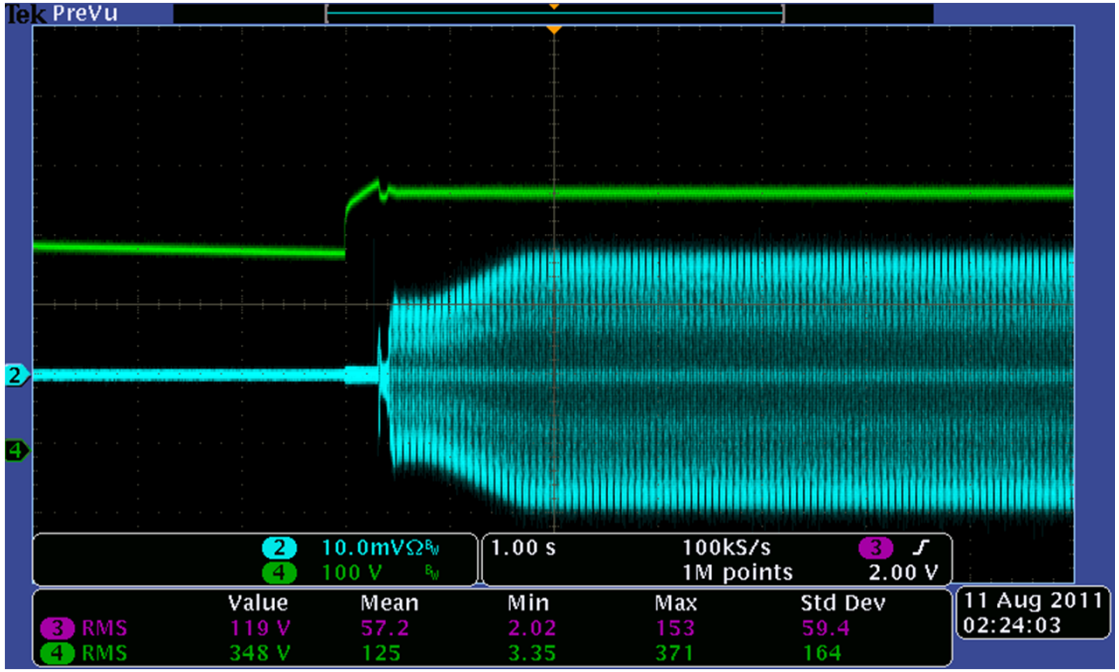
Inv V_out	Inv P_out	Output PF	THDi
119.5	100.3	0.983	12.60%
119.8	151.6	0.992	8.70%
119.2	198.4	0.995	6.80%
119.5	248.1	0.996	5.80%
119.8	297.7	0.997	5%
120.1	344.1	0.997	4.30%
119.6	391.7	0.997	3.90%
119.9	439.2	0.997	3.60%
120	464.2	0.997	3.40%





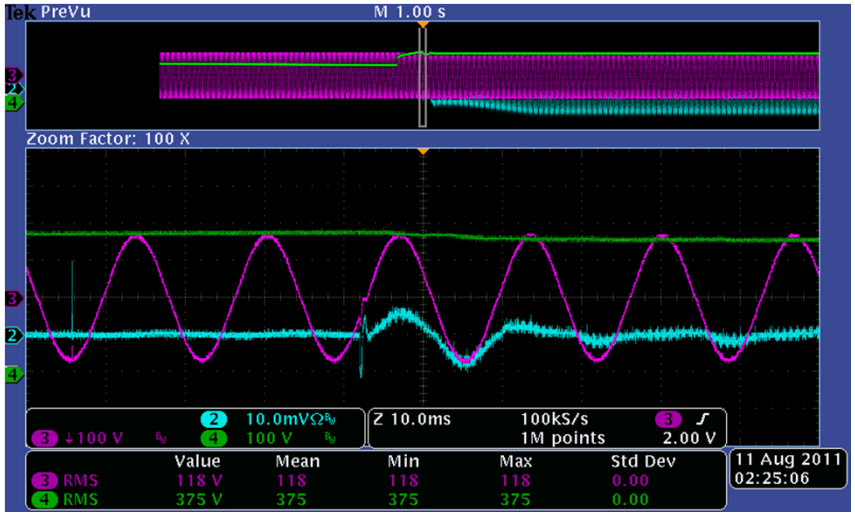
Waveforms – Start Up

120VAC/60Hz, turning on
CH2: Output Current(Blue)
CH3: Grid Voltage(Red)
CH4: Bus voltage

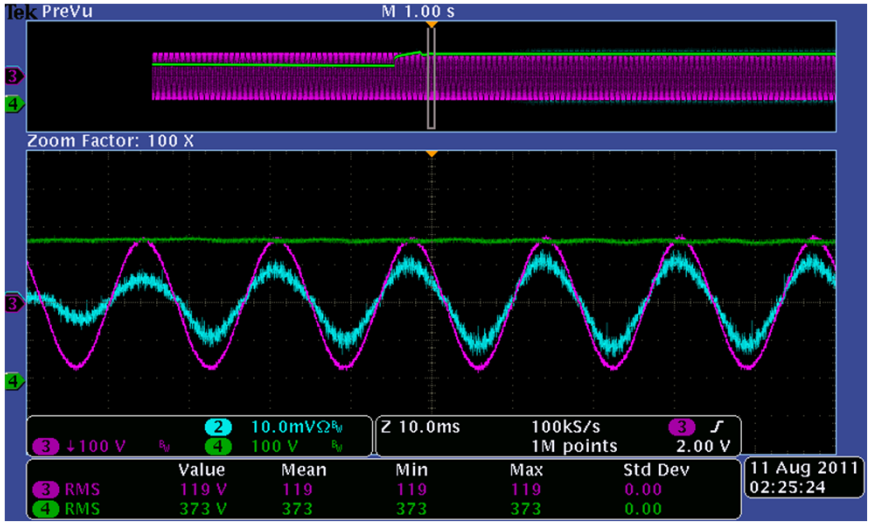


The turning on overview

Waveforms – Start Up



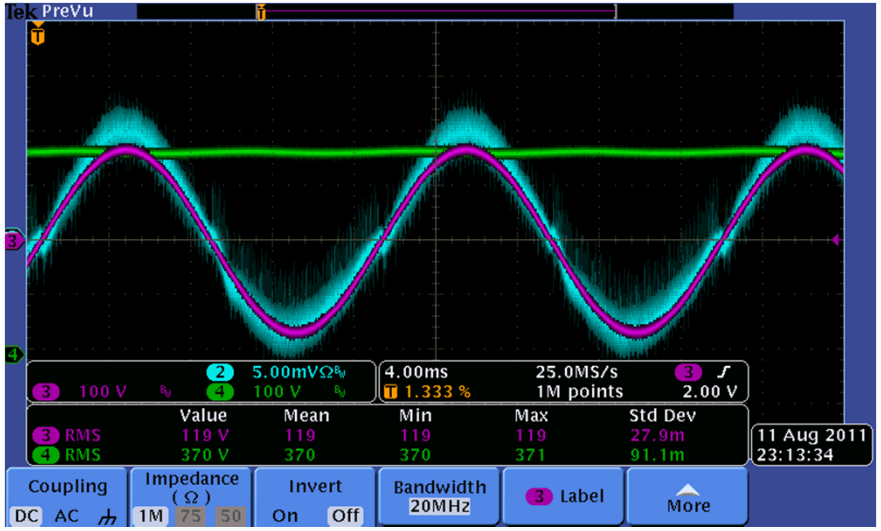
The DC-AC turn on the PWM



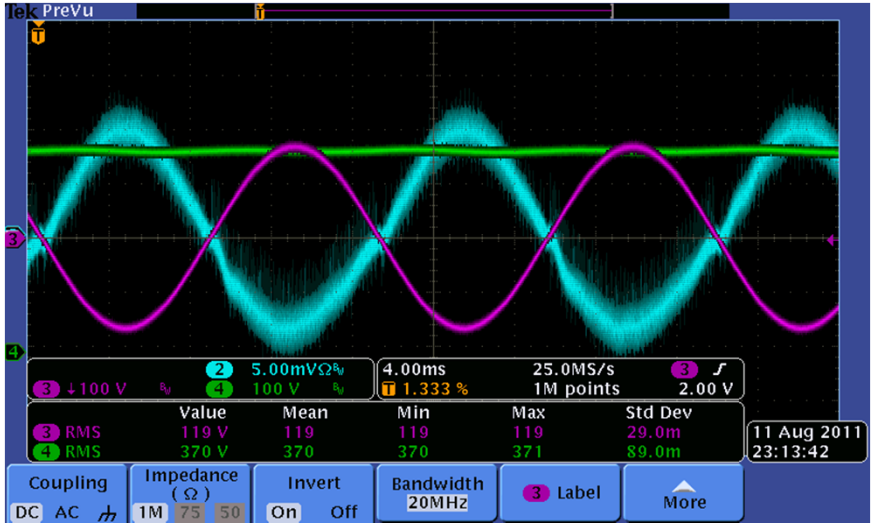
The MPPT is on

Waveforms – Normal Operation

120VAC/60Hz, 100W
CH2: Output Current(Blue)
CH3: Grid Voltage(Red)
CH4: Bus voltage



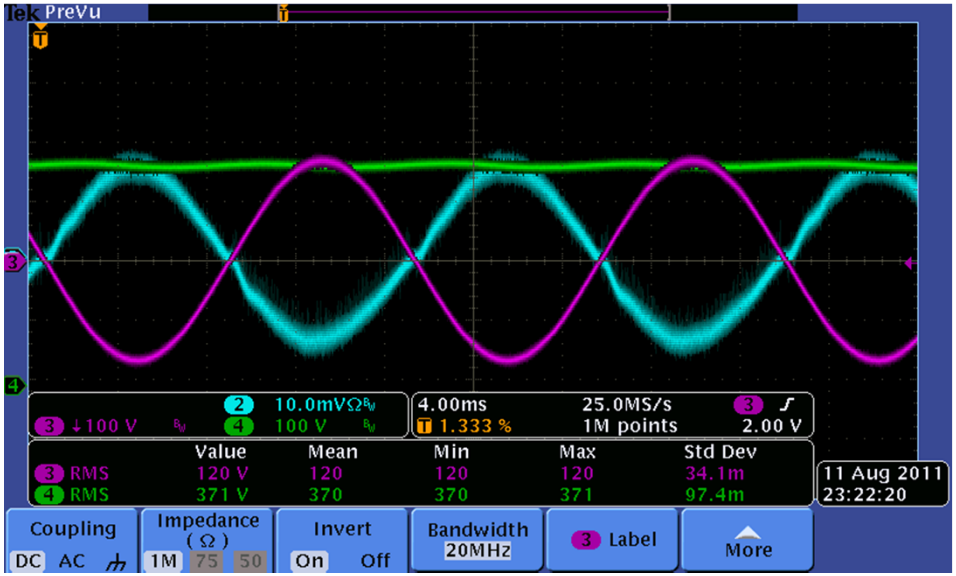
100W output (BUS, current, grid voltage)

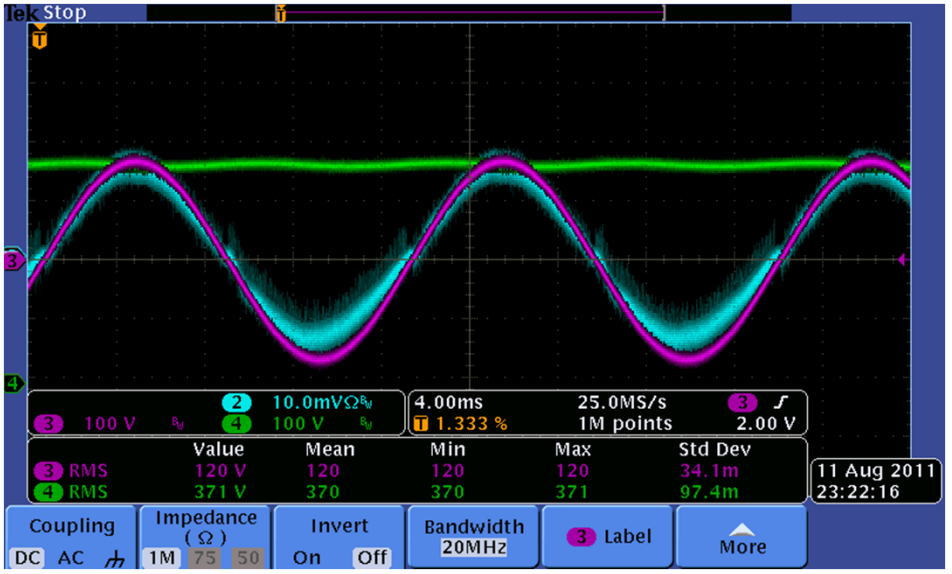


100W output (BUS, current, inverse grid voltage)

Waveforms – Normal Operation

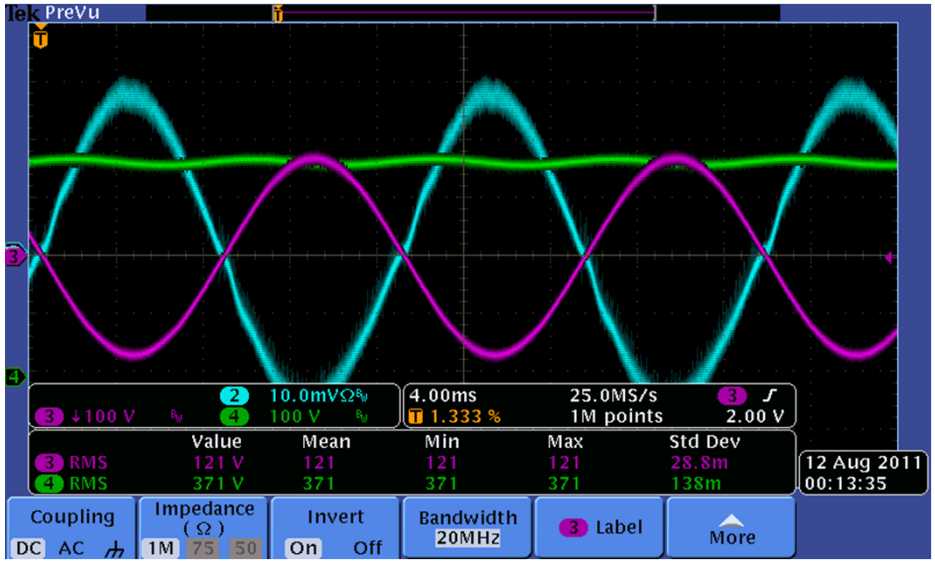
120VAC/60Hz, 250W
CH2: Output Current(Blue)
CH3: Grid Voltage(Red)
CH4: Bus voltage

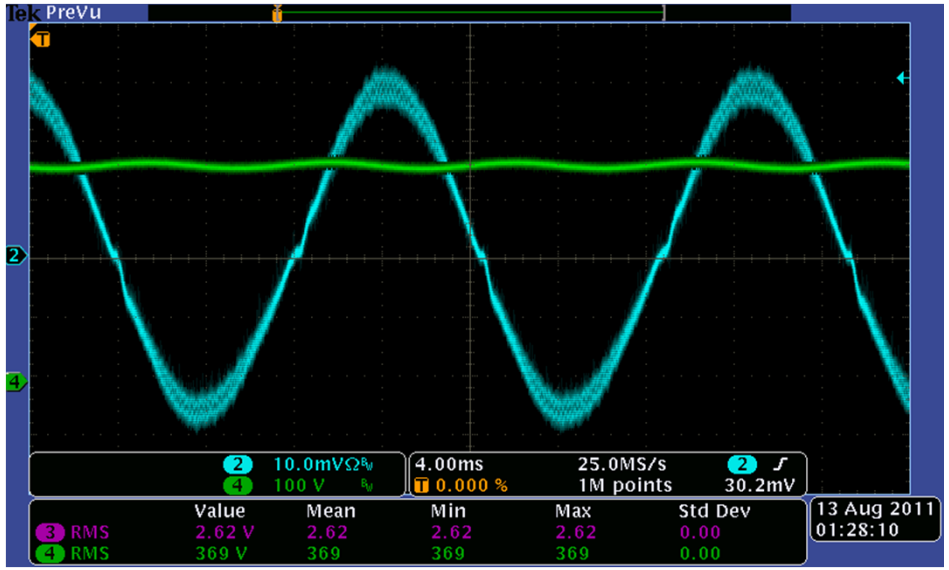




Waveforms – Normal Operation

120VAC/60Hz, 500W
CH2: Output Current(Blue)
CH3: Grid Voltage(Red)
CH4: Bus voltage

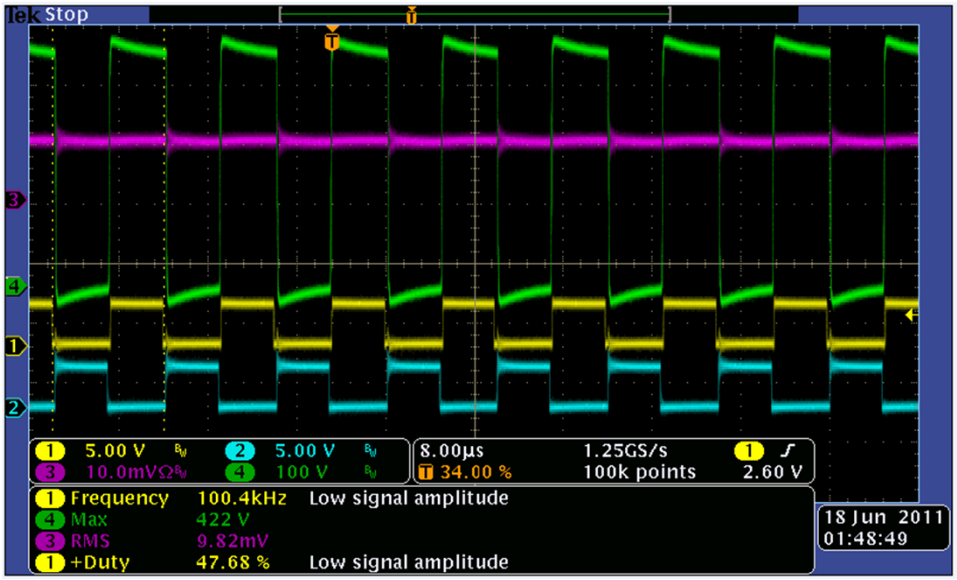




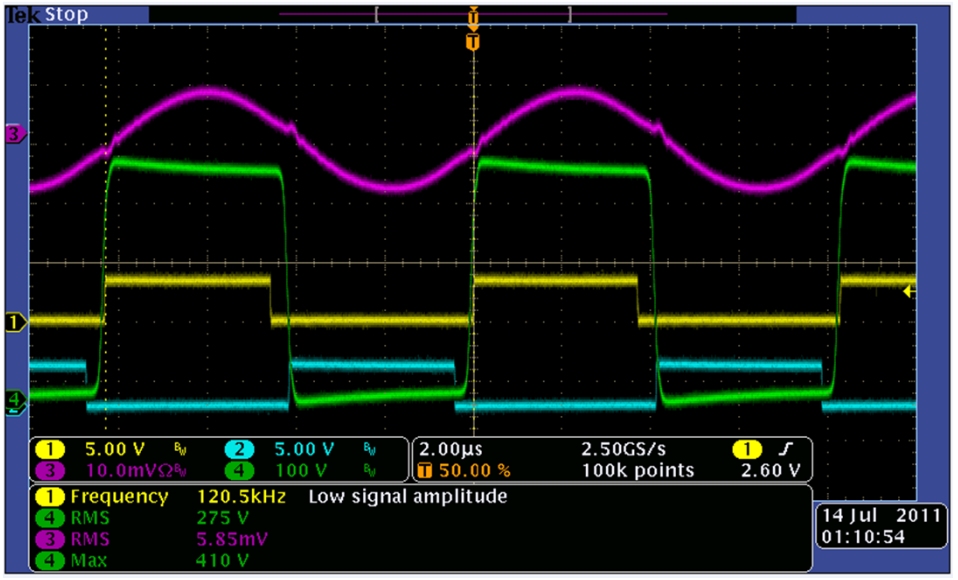
The Fe-Si core 2.5mH 500W waveform

MPPT DC/DC Waveforms

MPPT DC-DC Boost, Vin=200V, Vout=400V, Pout=500W
CH1& CH2: Boost PWM
CH3: Boost Input Current (2A/div)
CH4: Boost MOSFET Drain-Source Volt



MPPT DC-DC LLC, Vin=402V, Vout=400V, Pout=500W
CH1& CH2: LLC PWM(Ch1-upper MOSFET PWM, Ch2-lower MOSFET PWM)
CH3: LLC Resonant Inductor Current (5A/div)
CH4: LLC Switch Node Voltage (Lower MOSFET Drain-Source Volt)



C2000 Benefits

- High Processing Power
  - Fastest 32bit DSP CPU
  - Industry unique CLA
  - Industry unique VCU for PLC
  - Fastest (12bit) ADC, Priority Based ADC Triggering
  - Fast Interrupt Response
  - Highest PWM Resolution (for High PWM Frequency)
  - On-chip Analog Comparators for fast and reliable OVP, UVP, OCP, even on high-end devices (unique)
- High Resolution and Accuracy
  - 32bit CPU Word Length
  - 12bit ADC Resolution
  - Highest PWM Resolution
- Safety and Reliability
  - Trip Zone (for OTP, OVP, UVP, OCP, etc.
  - On-chip Analog Comparators
  - Unique Triple Clock Failure Detection and Protection
  - AEC Q100 Version
- Power Friendly Peripherals
  - Flexible and Powerful PWMs, up to 18 channels (unique)
  - Most flexible ADC Triggering and Sequencing
  - On-Chip Analog Comparators
- Easy-To-Use Tools and Dev Supports
  - CCS
  - Industry unique and most friendly ControlSuite
  - Solar Inverter Dev/Eval Kits (closest to real app)
  - Power Supply Dev/Eval Kits (closest to real app)
  - Third Parties
  - Training Workshops

Thank You