PR410
TMS320x281x Design 1
TPS767D3XX with precise SVS trip points

FEATURES:

- Meets the sequencing requirements (Option 2) of the TMS320F281x processor. Can be simplified to power the TMS320C281x and TMS320R281x.
- Dual-channel TPS767D318 low-dropout (LDO) linear regulator in thermally enhanced PowerPAD^{TM} package saves cost and space.
- TPS3803-01 adjustable supervisory (SVS) IC is used to provide:
  - more precise monitoring of the V_{DD} = 3.3 V I/O rail than the internal SVS's of the TPS767D3XX can provide.
  - sequencing of first the I/O rail then the core rail.
- TPS3808G01 adjustable SVS IC is used to provide:
  - more precise monitoring of the I/O rail than the internal SVS's of the TPS767D3XX can provide
  - open drain /RESET with programmable delay set with a capacitor on the CT pin
- The Q1 versions of the TPS3803-01 and TPS767D3XX operate up to T_A = 125 C and are automotive qualified. The TPS3808G01 operates up to T_A = 125 C. A Q1 version of the TPS3808G01 that is automotive qualified will be available in early 2005.
- Linear regulators start-up fast, allowing large in-rush currents for charging bulk capacitors at start-up. The current draw on the input power supply is minimized by sequencing first the I/O rail then the core rail.

IMPORTANT WEB LINKS:

- Link to the TI power management home page at http://power.ti.com then select the TI DSP Solutions link for more information and other reference designs.
- Link to datasheets at http://focus.ti.com/lit/ds/symlink/tps767d301-q1.pdf, http://focus.ti.com/lit/ds/symlink/tps3803-01-q1.pdf and http://focus.ti.com/lit/ds/symlink/tps3808g01.pdf .
- Link to application note SLVA118 http://focus.ti.com/lit/an/slva118/slva118.pdf to explore the thermal considerations in using linear regulators.

IMPLEMENTATION NOTES:

- **Component selection:**
  - 0.5% tolerance or better resistors are required to provide the precise SVS trip points listed on the schematic
  - If different capacitors are used for C4 and C5 than recommended per the BOM, they must meet the ESR requirements per the datasheet.

- **Power Dissipation/Thermal Issues:**
  - The maximum output current per channel of the dual regulator is dependent on the device's power dissipation. The following equation can be used to compute actual power dissipation and/or maximum output current per channel:

    $P_{Dact} = (V_{IN} - V_{DD\text{-}3.3V}) * I_{Vdd\text{-}3.3V} + (V_{IN} - V_{DD\text{-}CORE})*I_{Vdd\text{-}core}$

    For example, the IC can only dissipate 1.25W at $T_A = 85^o$ C and no airflow.
  - The maximum power dissipation of which the package is capable is

    $$P_{Dmax} = (T_{Jmax} - T_A)/R_{\Theta JA}$$

    where T_{Jmax} is the maximum junction temperature of the device and $R_{\Theta JA}$ is the thermal resistance for a given board type and set of ambient conditions.
  - Refer to the application section of the datasheet for thermal resistances at different ambient temperatures, airflows and ground plane heatsink area.
- **Modifications**
  - **/RESET delay:** Adjustable with capacitor C8.
  - **For C281x and R281x DSPs:** Since sequencing is not required for the TMS320C281x or the TMS320R281x, transistor Q1 and resistors R1 and R2 can be omitted and both /EN1 and /EN2 can be tied together, thereby allowing both regulators to be enabled at the same time and removing power rail sequencing. However, sequencing is still recommended since it helps to prevent the input power supply from being pulled down at start-up due to in-rush currents for charging each rail's bulk capacitors.
- **Waveforms:**

  Waveforms were generated while powering an ezDSP TMS320F2812 evaluation board and with the 1.8-V rail pulling 200 mA and the 3.3-V rail pulling 175 mA steady state.

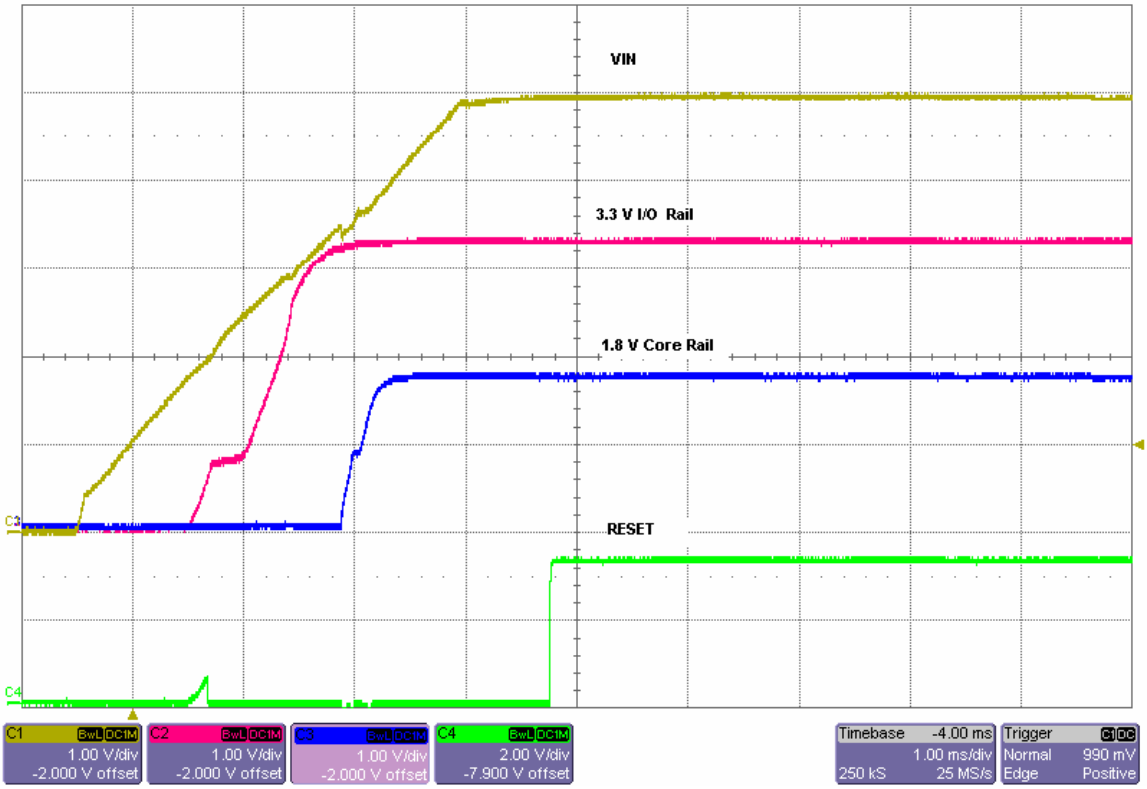

Figure 1 - Power up with V_{IN} = 5.0 V, /EN grounded

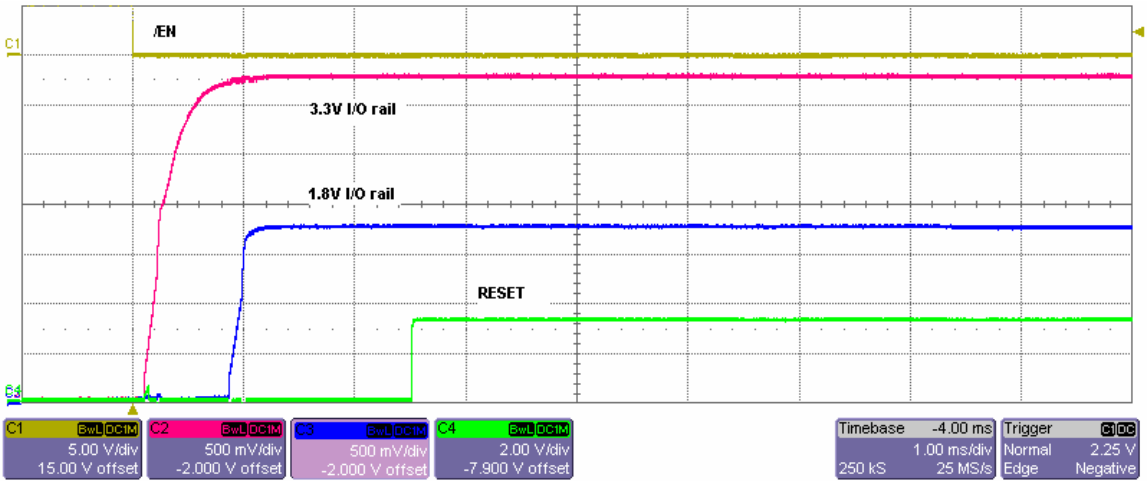

Figure 2 - Power up from enable when V_{IN} = 5.0 V

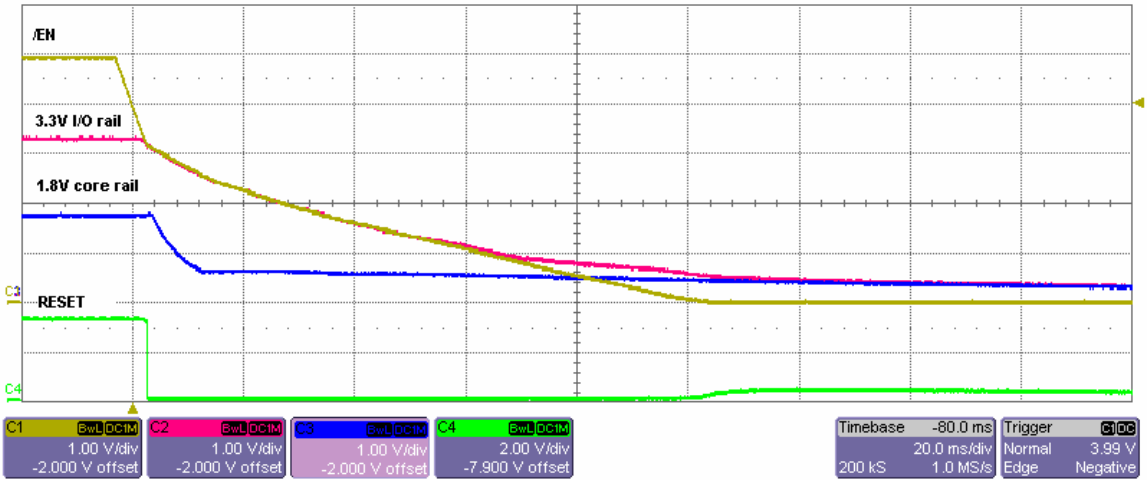

Figure 3 - Power down with V_{IN} = 5.0 V, /EN grounded

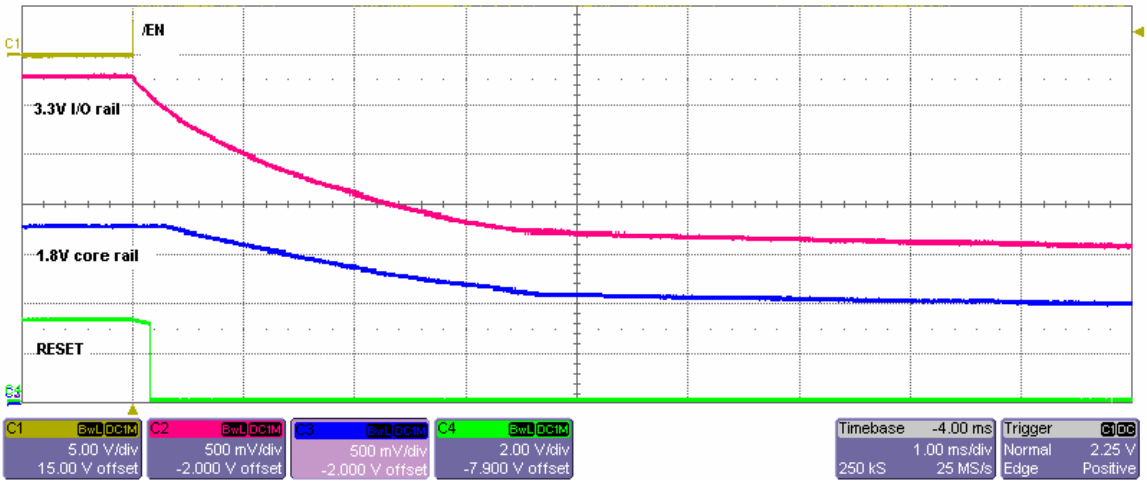

Figure 4 - Power down from enable when V_{IN} = 5.0 V

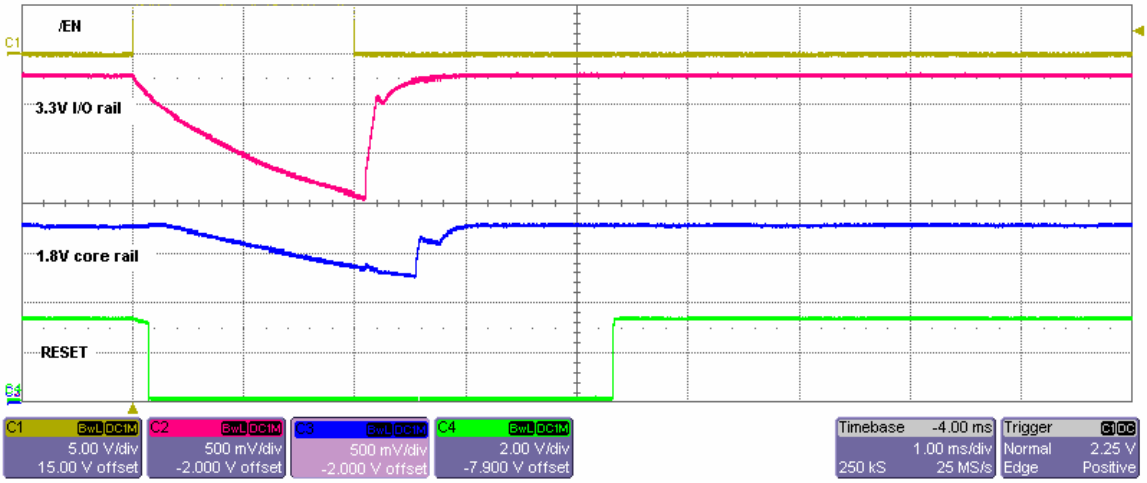

Figure 5 - RESET and recovery after V_{DD} = 3.3V fails

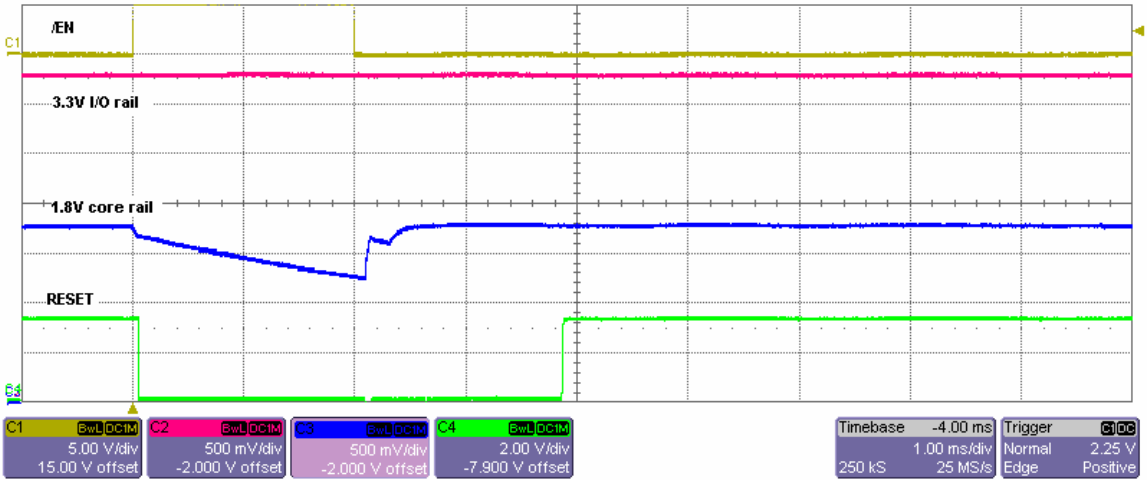

Figure 6 - RESET and recovery after V_{DD} = 1.8V fails

QUESTIONS?

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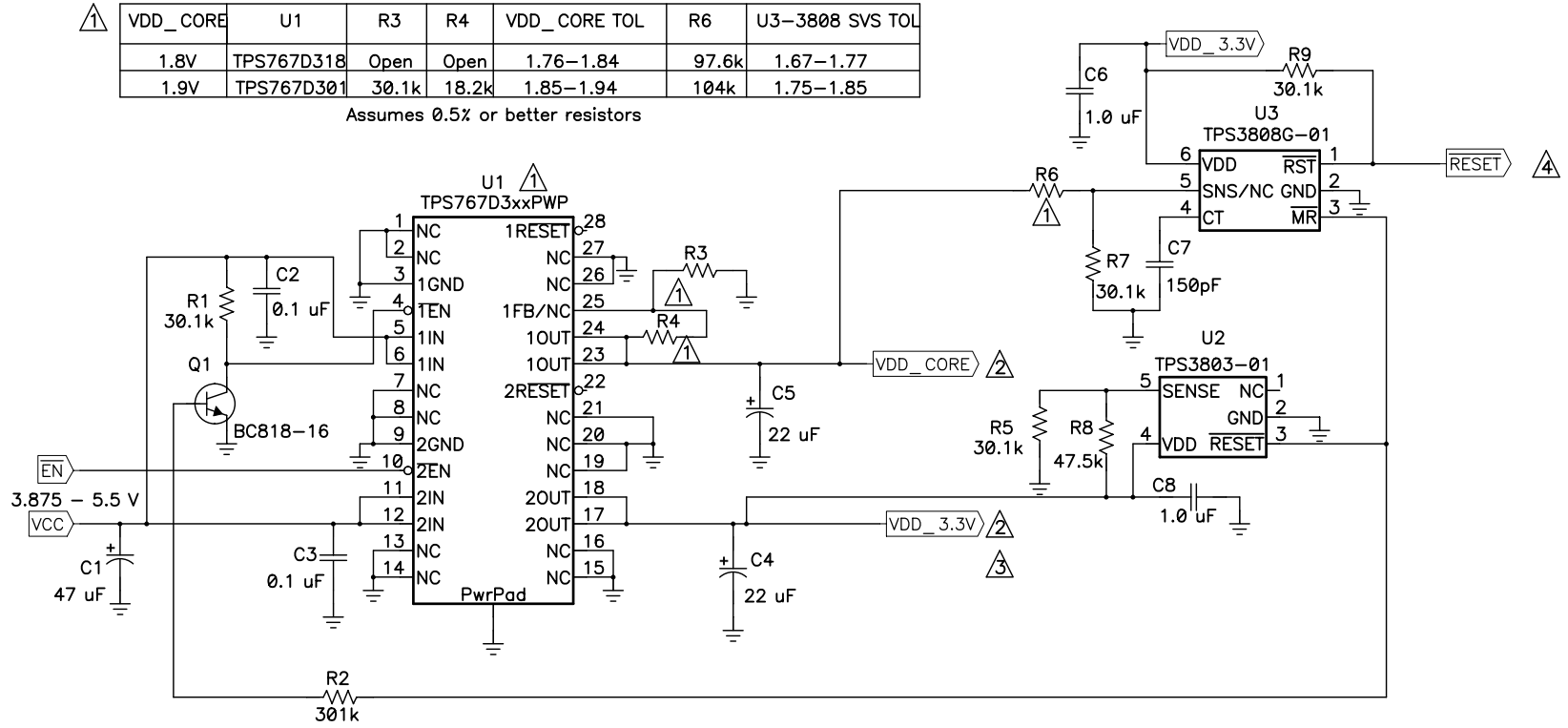

VDD_CORE	U1	R3	R4	VDD_CORE TOL	R6	U3–3808 SVS TOL
1.8V	TPS767D318	Open	Open	1.76–1.84	97.6k	1.67–1.77
1.9V	TPS767D301	30.1k	18.2k	1.85–1.94	104k	1.75–1.85

Assumes 0.5% or better resistors

2 Package power dissipation (Pd) determines maximum current.
Pd is a function of Vin and ambient temperature.

VDD_3.3V TOL	R8	U2–3803 SVS
3.234–3.366	47.5k	3.09–3.23

Assumes 0.5% or better resistors

4 /RESET on the TPS3808 has an open drain output and requires an external pullup resistor (R9 on this design).

Title	TPS767D3XX with precise SVS trip points	
Size B	Number PR410	Rev
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Date: 1/11/2005

PR410 BOM

COUNT						
001	002	RefDes	Description	Size	Part Number	MFR
1	1	C1	Capacitor, Tantalum, 47-uF, 6.3-V, 1.4-milliohm, 20%	B Case	293D476X6R3B2	Vishay
2	2	C2, C3	Capacitor, Ceramic, 0.1-uF, 25-V, X7R, 10%	0603	C1608X7R1E104KT	TDK
2	2	C4, C5	Capacitor, Tantalum, 22-uF, 6.3-V, 570-milliohm, 20%	B Case	595D226X96R3B2	Vishay
2	2	C6, C8	Capacitor, Ceramic, 1.0-uF, 16-V, X5R, 10%	0603	C1608X5R1C105KT	TDK
1	1	C7	Capacitor, Ceramic, 150-pF, 50-V, X7R, 10%	0603	C1608X7R1H151KT	TDK
1	1	Q1	Bipolar, NPN, 25-V, 500-mA, 0.3-W	SOT23	BC818-16	Vishay
4	4	R1, R5, R7, R9	Resistor, Chip, 30.1k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R2	Resistor, Chip, 301k-Ohms, 1/16-W, 1%	0603	Std	Std
0			Resistor, Chip, xx-Ohms, 1/16-W, 1%			
	1	R3	Resistor, Chip, 30.1k-Ohms, 1/16-W, 1%	0603	Std	Std
0			Resistor, Chip, xx-Ohms, 1/16-W, 1%			
	1	R4	Resistor, Chip, 18.2k-Ohms, 1/16-W, yy%	0603	Std	Std
1			Resistor, Chip, 97.6k-Ohms, 1/16-W, 1%	0603	Std	Std
	1	R6	Resistor, Chip, 104k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R8	Resistor, Chip, 47.5k-Ohms, 1/16-W, 1%	0603	Std	Std
1			IC, Dual 1-A Low-Dropout Regulator	PWP28	TPS767D318PWP	TI
	1	U1	IC, Dual 1-A Low-Dropout Regulator	PWP28	TPS767D301PWP	TI
1	1	U2	IC, Voltage Supervisor, 3.3-Volts,	SOP-5 (DCK)	TPS3803H33DCK	TI
1	1	U3	IC, Low Quiescent Current Programmable, Adj-V, Delay Time 1ms to10s	SOT23-6	TPS3808G-01	TI

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PR411
TMS320x281x Design 4
TPS767D3XX

FEATURES:

- Meets the sequencing requirements (Option 2) of the TMS320F281x processor. Can be simplified to power the TMS320C281x and TMS320R281x.
- /RESET delay fixed at 200 ms minimum.
- Dual-channel TPS767D3XX low-dropout (LDO) linear regulator in thermally enhanced PowerPAD^{TM} package saves cost and space.
- The Q1 version of the TPS767D3XX operates up to T_A = 125 C and is automotive qualified.
- Linear regulators start-up fast, allowing large in-rush currents for charging bulk capacitors at start-up. The current draw on the input power supply is minimized by sequencing first the I/O rail then the core rail.

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- Link to datasheets at http://focus.ti.com/lit/ds/symlink/tps767d301-q1.pdf,
- Link to application note SLVA118 http://focus.ti.com/lit/an/slva118/slva118.pdf to explore the thermal considerations in using linear regulators.

IMPLEMENTATION NOTES:

- **Component selection:**
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  - The maximum output current per channel of the dual regulator is dependent on the device's power dissipation. The following equation can be used to compute actual power dissipation and/or maximum output current per channel:

    $$P_{Dact} = (V_{IN} - V_{DD\text{-}3.3V}) * I_{Vdd\text{-}3.3V} + (V_{IN} - V_{DD\text{-}CORE})*I_{Vdd\text{-}core}$$

    For example, the IC can only dissipate 1.25Wat $T_A = 85^o$ C and no airflow.
  - The maximum power dissipation of which the package is capable is

    $$P_{Dmax} = (T_{Jmax} - T_A)/R_{\Theta JA}$$

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- **Modifications**
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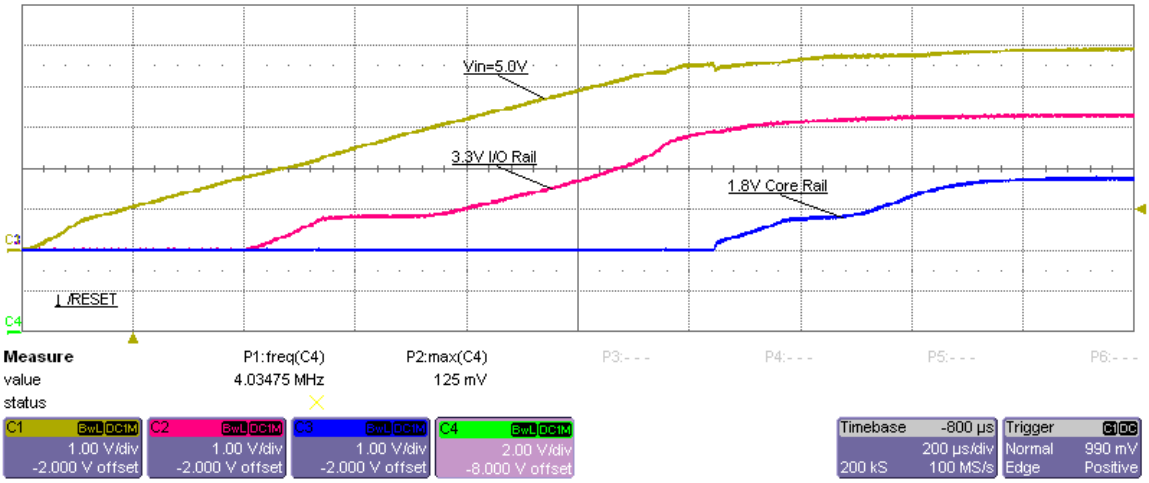

Figure 1 - Power up with V_{IN} = 5.0 V, /EN grounded

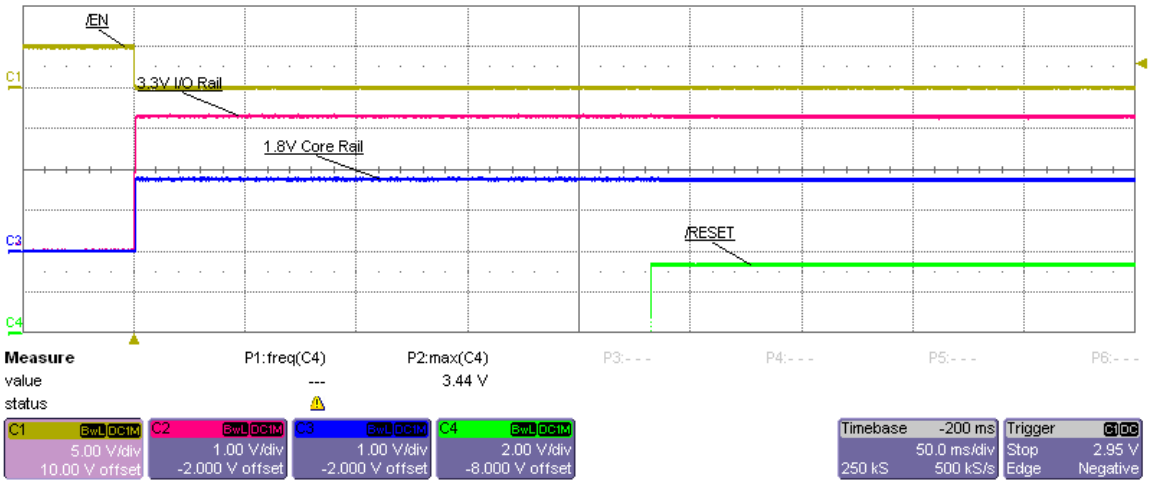

Figure 2 - Power up from enable when V_{IN} = 5.0 V

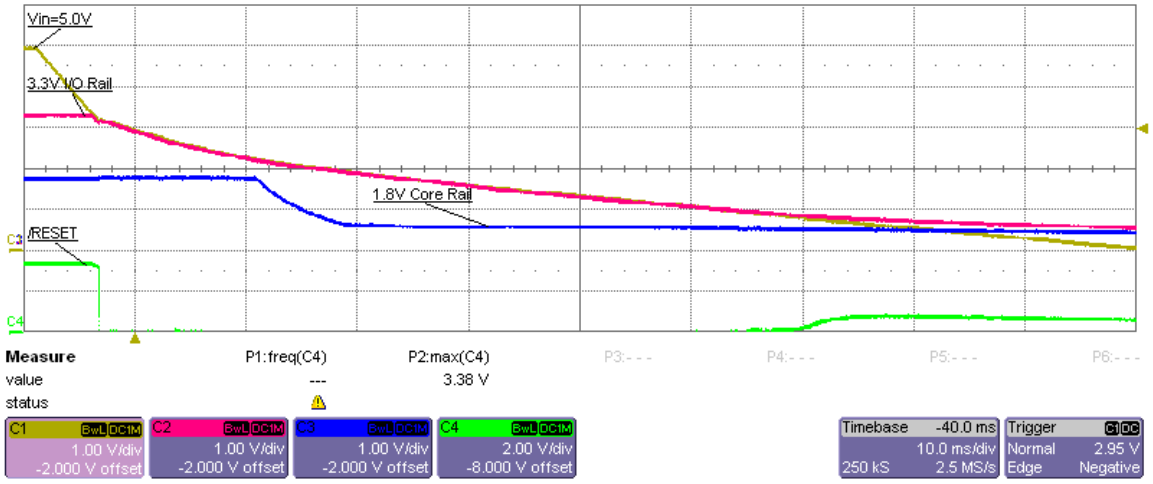

Figure 3 - Power down with V_{IN} = 5.0 V, /EN grounded

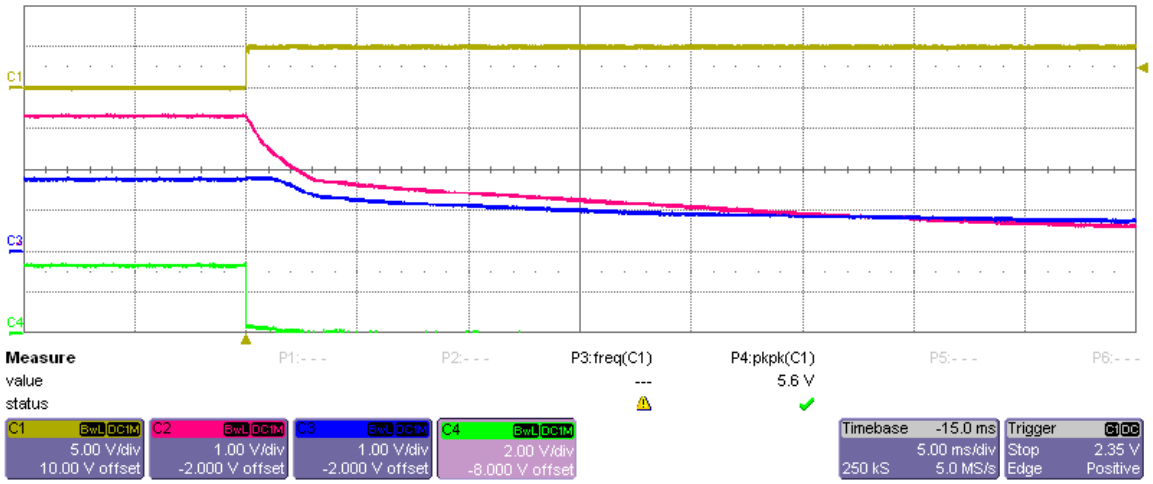

Figure 4 - Power down from enable when V_{IN} = 5.0 V

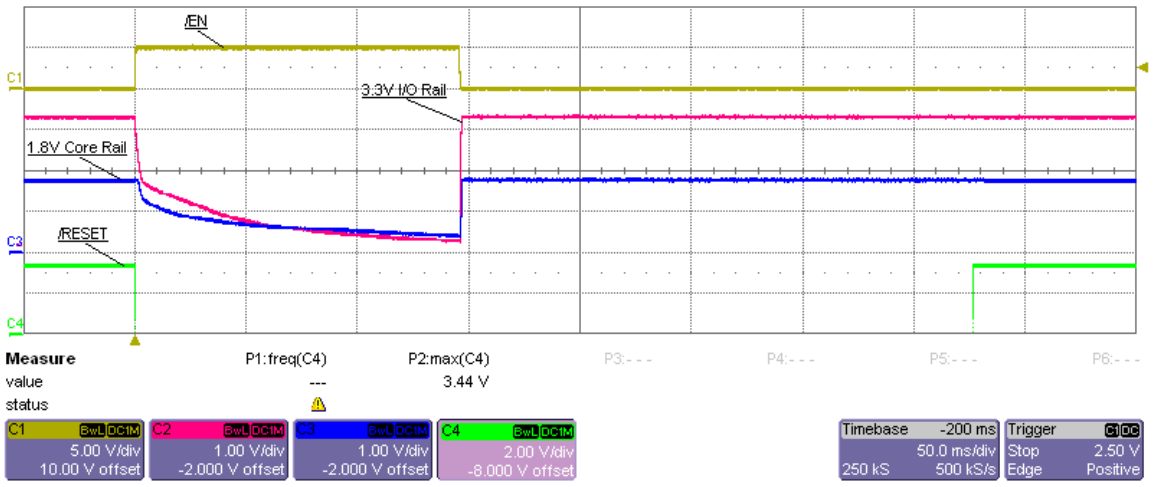

Figure 5 - RESET and recovery after V_{DD} = 3.3V fails

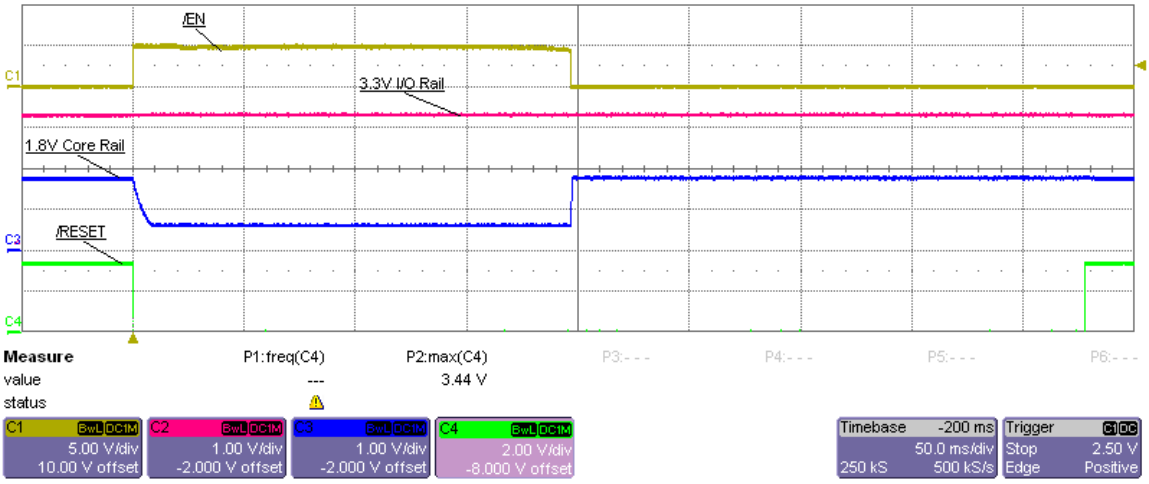

Figure 6 - RESET and recovery after V_{DD} = 1.8V fails

QUESTIONS?

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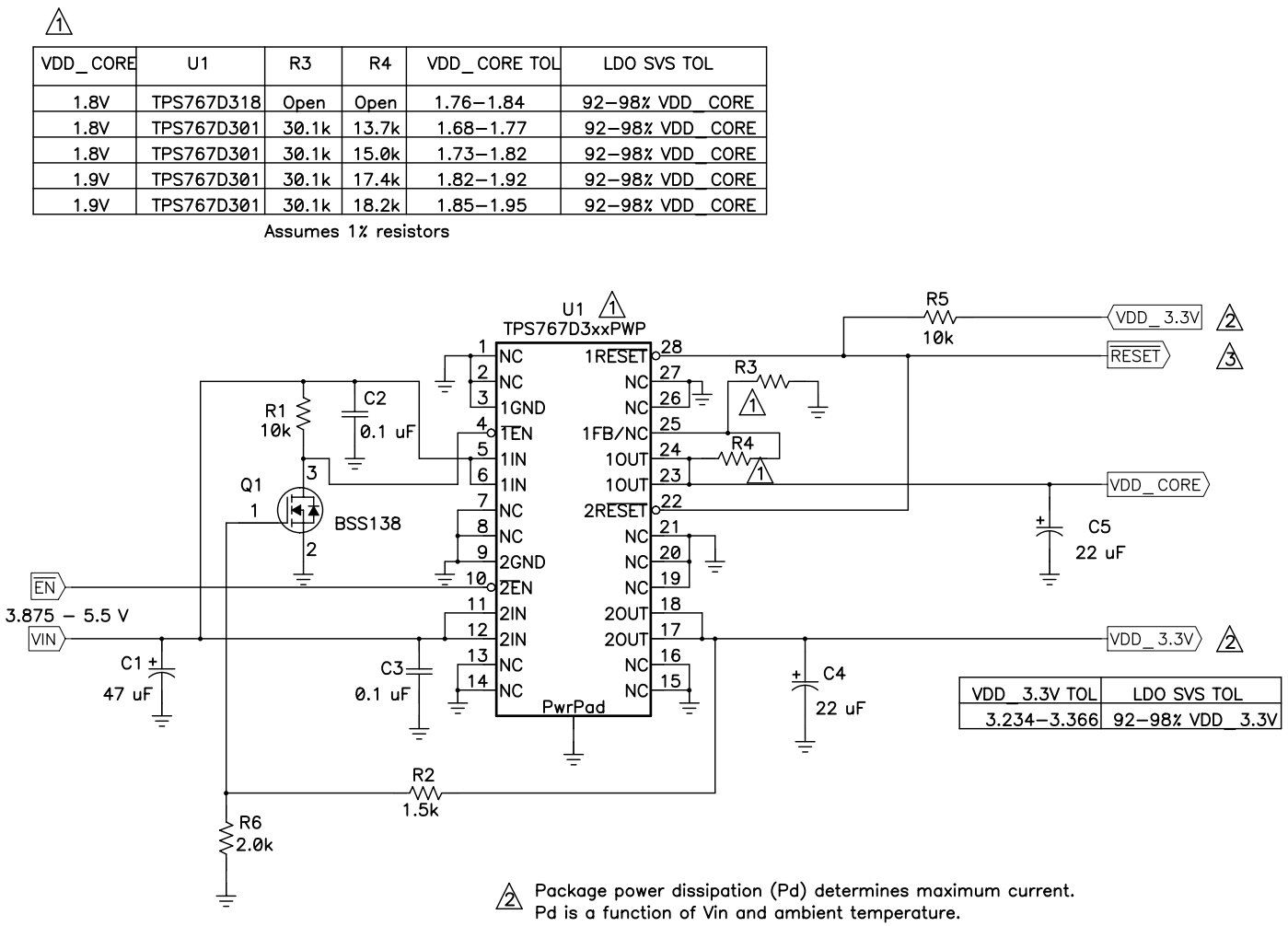
1
VDD_CORE
U1
TPS767D318
R3
Open
R4
Open
VDD_CORE TOL
1.76–1.84
LDO SVS TOL
92–98% VDD_CORE
U1
TPS767D301
30.1k
13.7k
1.68–1.77
92–98% VDD_CORE
U1
TPS767D301
30.1k
15.0k
1.73–1.82
92–98% VDD_CORE
1.9V
TPS767D301
30.1k
17.4k
1.82–1.92
92–98% VDD_CORE
1.9V
TPS767D301
30.1k
18.2k
1.85–1.95
92–98% VDD_CORE
Assumes 1% resistors
U1
TPS767D3xxPWP
1 NC
2 NC
3 1GND
4 TEN
5 1IN
6 1IN
7 NC
8 NC
9 2GND
10 2EN
11 2IN
12 2IN
13 NC
14 NC
28 1RESET
27 NC
26 NC
25 1FB/NC
24 1OUT
23 1OUT
22 2RESET
21 NC
20 NC
19 NC
18 2OUT
17 2OUT
16 NC
15 NC
PwrPad
R1
10k
C2
0.1 uF
Q1
BSS138
R5
10k
R3
R4
C5
22 uF
EN
3.875 – 5.5 V
VIN
C1
47 uF
C3
0.1 uF
C4
22 uF
R2
1.5k
R6
2.0k
VDD_3.3V
RESET
VDD_CORE
VDD_3.3V
VDD_3.3V TOL
LDO SVS TOL
3.234–3.366
92–98% VDD_3.3V
2
Package power dissipation (Pd) determines maximum current.
Pd is a function of Vin and ambient temperature.
3
/RESET on the TPS767xx has a 200ms delay and an open drain
output which requires an external pullup resistor (R5 on this design).
Title
TMS320x281x Design 4 TPS767D3XX
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PR411 BOM

COUNT									
-001	-002	-003	-004	-005	RefDes	Description	Size	Part Number	MFR
1	1	1	1	1	C1	Capacitor, Tantalum, 47-uF, 6.3-V, 1.4-milliohm, 20%	B Case	293D476X6R3B2	Vishay
2	2	2	2	2	C2, C3	Capacitor, Ceramic, 0.1-uF, 25-V, X7R, 10%	0603	C1608X7R1E104KT	TDK
2	2	2	2	2	C4, C5	Capacitor, Tantalum, 22-uF, 6.3-V, 570-milliohm, 20%	B Case	595D226X96R3B2	Vishay
1	1	1	1	1	Q1	MOSFET, N-ch, 50-V, 0.2-A, 5 Ohms	SOT23	BSS138	Fairchild
2	2	2	2	2	R1, R5	Resistor, Chip, 10k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	1	1	1	R2	Resistor, Chip, 1.5k-Ohms, 1/16-W, 1%	0603	Std	Std
0					R3	Resistor, Chip, xx-Ohms, 1/16-W, yy%	0603		
	1	1	1	1		Resistor, Chip, 30.1k-Ohms, 1/16-W, yy%	0603	Std	Std
0					R4	Resistor, Chip, xx-Ohms, 1/16-W, yy%	0603		
	1					Resistor, Chip, 13.7k-Ohms, 1/16-W, 1%	0603	Std	Std
		1				Resistor, Chip, 15.0k-Ohms, 1/16-W, 1%	0603	Std	Std
			1			Resistor, Chip, 17.4k-Ohms, 1/16-W, 1%	0603	Std	Std
				1		Resistor, Chip, 18.2k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	1	1	1	R6	Resistor, Chip, 2.0k-Ohms, 1/16-W, 1%	0603	Std	Std
1					U1	IC, Dual 1-A Low-Dropout Regulator	PWP28	TPS767D318PWP	TI
	1	1	1	1		IC, Dual 1-A Low-Dropout Regulator	PWP28	TPS767D301PWP	TI

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PR412
TMS320x281x Design 1
TPS736XX with optional TPS2051B switch from V_{IN} = 3.3V

FEATURES:

- Meets the sequencing requirements (Option 2) of the TMS320F281x processor. Can be simplified to power the TMS320C281x and TMS320R281x.
- Optional TPS2051B switch provides control of the timing between I/O rail up and core rail up
- Single-channel TPS736xx low-dropout (LDO) linear regulator, with inherent soft start, provides the core rail with high accuracy
- TPS3803-01 adjustable supervisory (SVS) IC is used to:
  - monitor the V_{DD} = 3.3 V I/O rail
  - sequence first the I/O rail then the core rail.
- TPS3808G01 adjustable SVS IC is used to:
  - monitor of the I/O rail
  - provide open drain /RESET with programmable delay set with a capacitor on the CT pin.
- The Q1 versions of the TPS3803-01 operates up to T_A = 125 C and is automotive qualified. The TPS3808G01 operates up to T_A = 125 C. Q1 versions of the TPS3808G01 and TPS736xxDCQ that are automotive qualified will be available in early 2005.
- The current draw on the input power supply is minimized by sequencing first the I/O rail then the core rail.

IMPORTANT WEB LINKS:

- Link to the TI power management home page at http://power.ti.com then select the TI DSP Solutions link for more information and other reference designs.
- Link to datasheets at http://focus.ti.com/lit/ds/symlink/tps73601.pdf, http://focus.ti.com/lit/ds/symlink/tps3803-01-q1.pdf and http://focus.ti.com/lit/ds/symlink/tps3808g01.pdf .
- Link to application note SLVA118 http://focus.ti.com/lit/an/slva118/slva118.pdf to explore the thermal considerations in using linear regulators.

IMPLEMENTATION NOTES:

- **Component selection:**
  - If different capacitors are used for C4 and C5 than recommended per the BOM, they must meet the ESR requirements per the datasheet.
- **Power Dissipation/Thermal Issues:**

- The maximum output current of the regulator is dependent on the device's power dissipation. The following equation can be used to compute actual power dissipation and/or maximum output current for the linear regulator:

  $P_{Dact} = (V_{IN} - V_{DD\text{-}CORE})*I_{Vdd\text{-}core}$

  For example, the IC can only dissipate 1.25Wat $T_A = 85^o$ C and no airflow.
- The maximum power dissipation of which the package is capable is

  $$P_{Dmax} = (T_{Jmax} - T_A)/R_{\Theta JA}$$

  where T_{Jmax} is the maximum junction temperature of the device and $R_{\Theta JA}$ is the thermal resistance for a given board type and set of ambient conditions.
- Refer to the application section of the datasheet for thermal resistances at different ambient temperatures, airflows and ground plane heatsink area.

- **Modifications**
  - **/RESET delay:** Adjustable with capacitor C8.
  - **For C281x and R281x DSPs:** Since sequencing is not required for the TMS320C281x or the TMS320R281x, power switch U1 can be omitted. However, the controlled sequencing and soft-start that the power switch provides is still recommended since both help to prevent the input power supply from being pulled down at start-up due to in-rush currents for charging each rail's bulk capacitors.
- **Waveforms:**

  Waveforms were generated while powering an ezDSP TMS320F2812 evaluation board and with the 1.8-V rail pulling 200 mA and the 3.3-V rail pulling 175 mA steady state.

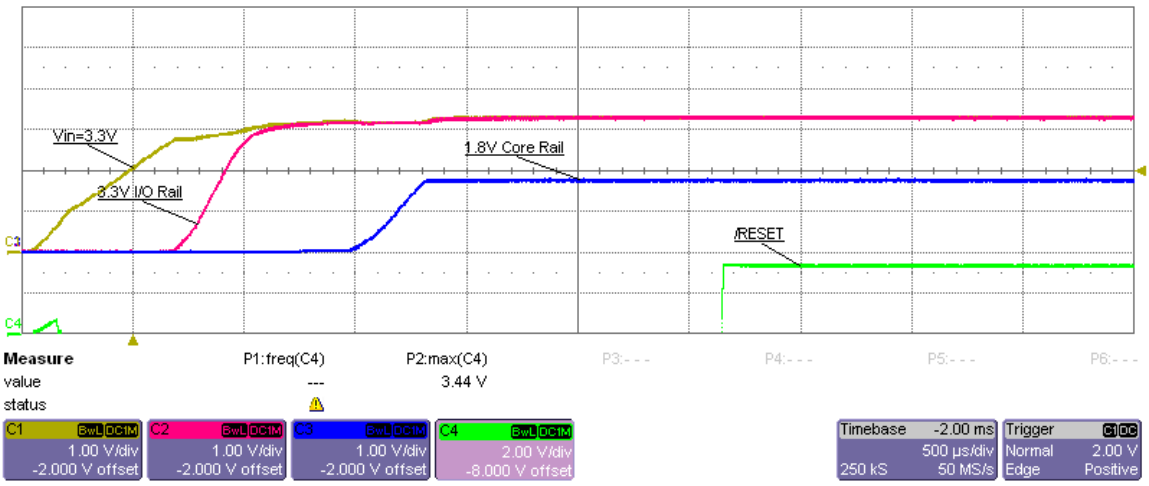

Figure 1 - Power up with V_{IN} = 5.0 V, /EN grounded

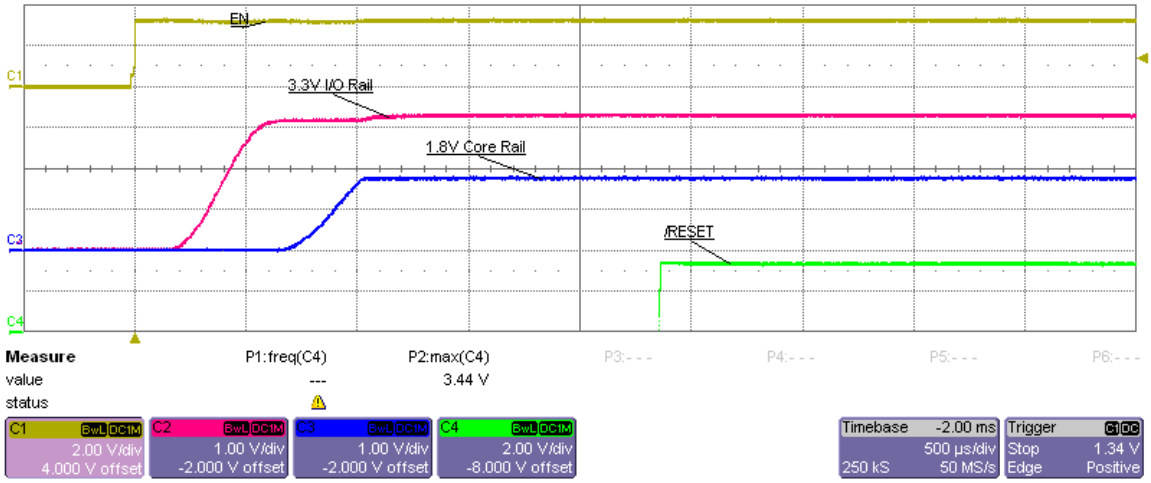

Figure 2 - Power up from enable when V_{IN} = 5.0 V

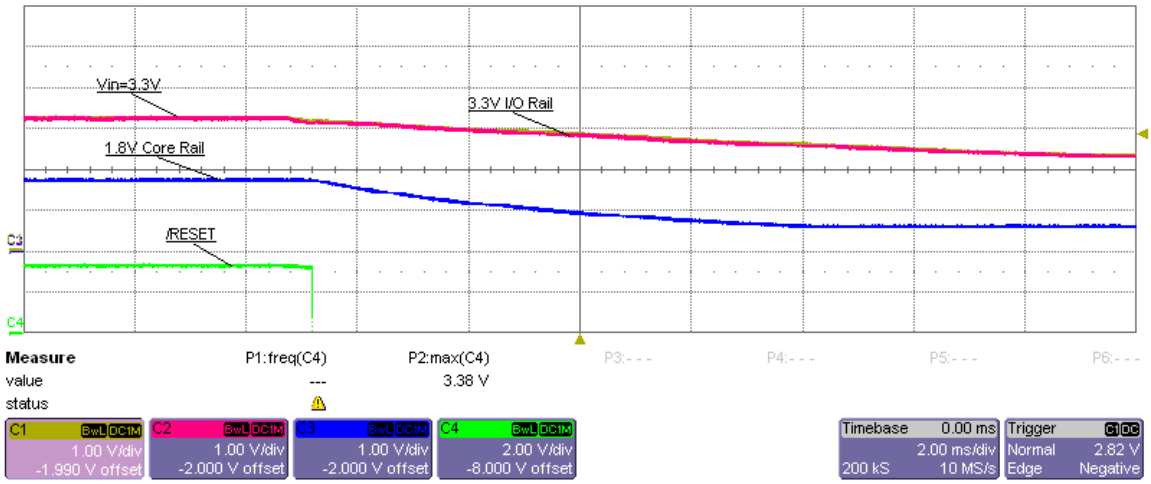

Figure 3 - Power down with V_{IN} = 5.0 V, /EN grounded

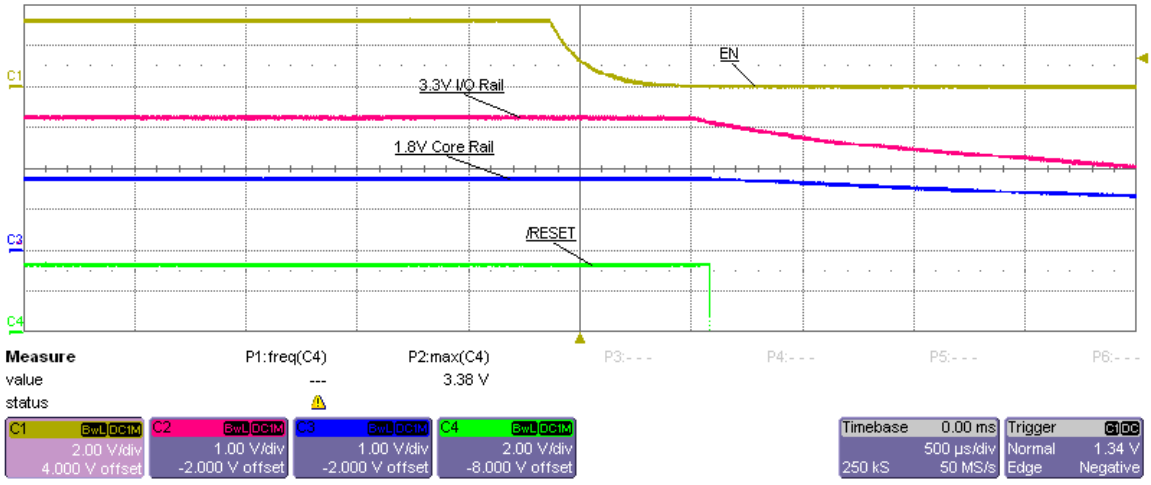

Figure 4 - Power down from enable when V_{IN} = 5.0 V

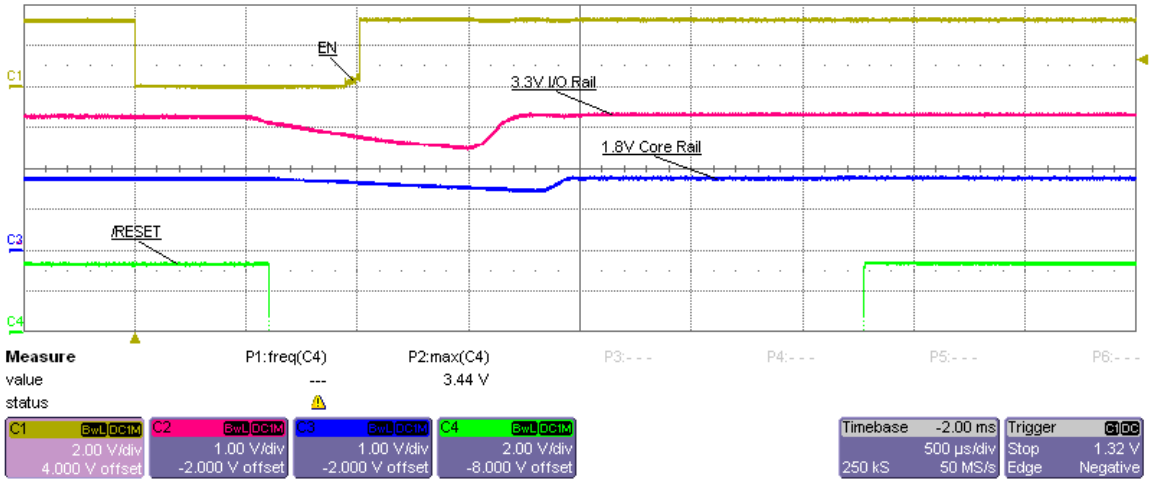

Figure 5 - RESET and recovery after V_{DD} = 3.3V fails

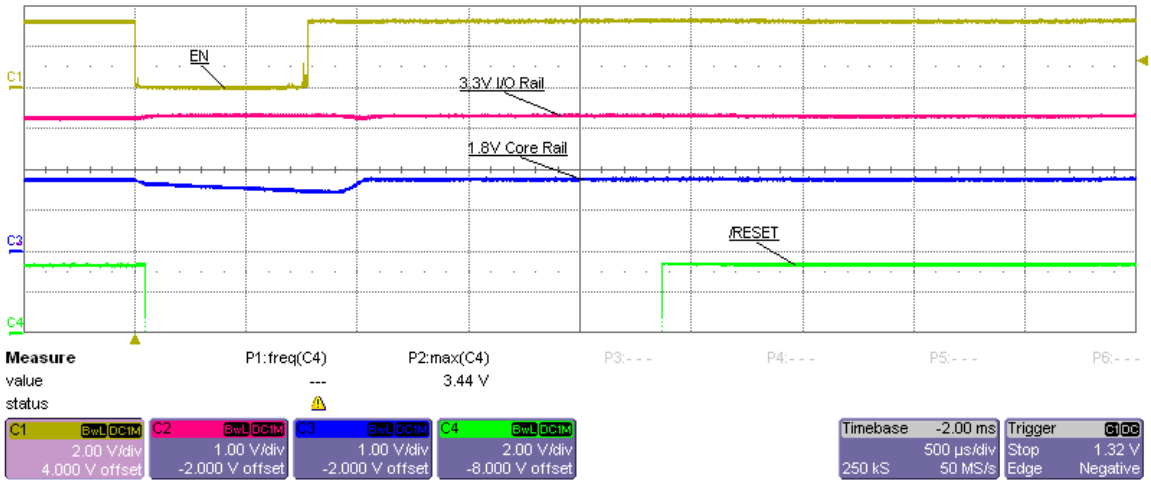

Figure 6 - RESET and recovery after V_{DD} = 1.8V fails

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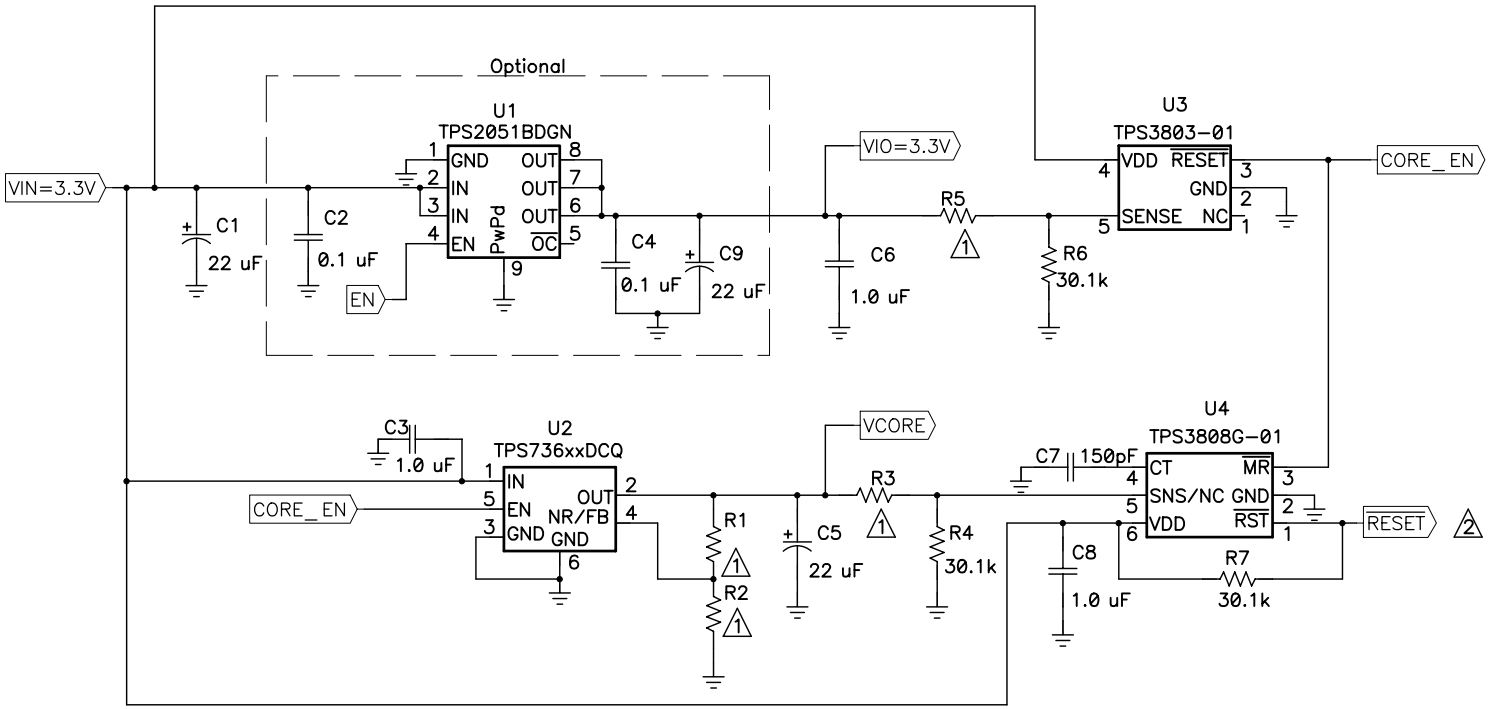

1	VDD_CORE	U2	R1	R2	VDD_CORE TOL	R3	U4–3808 SVS TOL	R5	U3–3803 SVS TOL
	1.8V	TPS73618	Open	Open	1.78–1.82	97.6k	1.67–1.77	47.5k	3.09–3.23
	1.9V	TPS73601	31.6k	54.9k	1.86–1.93	104k	1.75–1.85		

2 /RESET on the TPS3808 has an open drain output and requires an external pullup resistor (R7 on this design).

Title	TMS320x281x DSP Attach Design 3 – for Vin=3.3V	
Size: B	Number: PR412	Rev:
Date: 1/04/05		Drawn by:
Filename: pr412.sch		Sheet: of

Filename: PR412_bom.xls

Date: 1/11/2005

PR412 BOM

COUNT						
-001	-002	RefDes	DESCRIPTION	SIZE	Part Number	MFR
3	3	C1, C5, C9	Capacitor, Tantalum, 22-uF, 6.3-V, 570-milliohm, 20%	B Case	595D226X96R3B2	Vishay
2	2	C2, C4	Capacitor, Ceramic, 0.1-uF, 50-V, X7R, 10%	0603	C1608X7R1H104K	TDK
3	3	C3, C6, C8	Capacitor, Ceramic, 1.0-uF, 16-V, X7R, 10%	0603	C1608X7R1C105K	TDK
1	1	C7	Capacitor, Ceramic, 150-pF, 50-V, C0G, 5%	0603	C1608C0G1H151J	TDK
0	0	R1	Resistor, Chip, xx-Ohms, 1/16-W, 1%	0603		
0	1		Resistor, Chip, 31.6k-Ohms, 1/16-W, 1%	0603	Std	Std
0	0	R2	Resistor, Chip, xx-Ohms, 1/16-W, 1%	0603		
0	1		Resistor, Chip, 54.9k-Ohms, 1/16-W, 1%	0603	Std	Std
1	0	R3	Resistor, Chip, 97.6k-Ohms, 1/16-W, 1%	0603	Std	Std
0	1		Resistor, Chip, 104k-Ohms, 1/16-W, 1%	0603	Std	Std
3	3	R4, R6, R7	Resistor, Chip, 30.1k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R5	Resistor, Chip, 47.5k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	U1	IC,Current-Limited Power -Distribution Switches, 2.7-5.5V, 500mA	DGN-8	TPS2051BDGN	TI
1	0	U2	IC, Cap-Free NMOS, 400mA LDO Regulator With Reverse Current Protection	SOT223-6	TPS73618DCQ	TI
0	1		IC, Cap-Free NMOS, 400mA LDO Regulator With Reverse Current Protection	SOT223-6	TPS73601DCQ	TI
1	1	U3	IC, Voltage Supervisor, 3.3-Volts,	SOP-5 (DCK)	TPS3803-01DCK	TI
1	1	U4	IC, Low Quiescent Current Programmable, Adj-V, Delay Time 1ms to10s	SOT23-6	TPS3808G-01	TI

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PR413
TMS320x281x Design 2
TPS70202 Low Cost Design

FEATURES:

- Meets the sequencing requirements (Option 2) of the TMS320F281x processor. Can be simplified to power the TMS320C281x and TMS320R281x.
- Dual-channel TPS70202 500mA/200mA low-dropout (LDO) linear regulator in thermally enhanced PowerPAD^{TM} package saves cost and space.
- Linear regulators start-up fast, allowing large in-rush currents for charging bulk capacitors at start-up. The current draw on the input power supply is minimized by sequencing first the I/O rail then the core rail.

IMPORTANT WEB LINKS:

- Link to the TI power management home page at http://power.ti.com then select the TI DSP Solutions link for more information and other reference designs.
- Link to datasheets at http://focus.ti.com/lit/ds/symlink/tps70202.pdf
- Link to application note SLVA118 http://focus.ti.com/lit/an/slva118/slva118.pdf to explore the thermal considerations in using linear regulators.

IMPLEMENTATION NOTES:

- **Component selection:**
  - If different capacitors are used for C4 and C5 than recommended per the BOM, they must meet the ESR requirements per the datasheet.
- **Power Dissipation/Thermal Issues:**
  - The maximum output current per channel of the dual regulator is dependent on the device's power dissipation. The following equation can be used to compute actual power dissipation and/or maximum output current per channel:

    $$P_{Dact} = (V_{IN} - V_{DD\text{-}3.3V}) * I_{Vdd\text{-}3.3V} + (V_{IN} - V_{DD\text{-}CORE})*I_{Vdd\text{-}core}$$

    For example, the IC can only dissipate 1.1W at $T_A = 85^o$ C and no airflow.
  - The maximum power dissipation of which the package is capable is

    $$P_{Dmax} = (T_{Jmax} - T_A)/R_{\Theta JA}$$

    where T_{Jmax} is the maximum junction temperature of the device and $R_{\Theta JA}$ is the thermal resistance for a given board type and set of ambient conditions.
  - Refer to the application section of the datasheet for thermal resistances at different ambient temperatures, airflows and ground plane heatsink area.
- **Modifications for C281x and R281x:**
  - Since sequencing is not required for the TMS320C281x or the TMS320R281x, transistor Q1 and resistors R1 and R7 can be omitted, PG1 and PG2 can be tied to MR and both /EN1 and /EN2 can be tied

together, thereby allowing both regulators to be enabled at the same time and removing power rail sequencing. However, sequencing is still recommended since it helps to prevent the input power supply from being pulled down at start-up due to in-rush currents for charging each rail's bulk capacitors.

- **Waveforms:**
  Waveforms were generated while powering an ezDSP TMS320F2812 evaluation board loaded with the 1.8-V rail pulling 200 mA and the 3.3-V rail pulling 175 mA steady state.

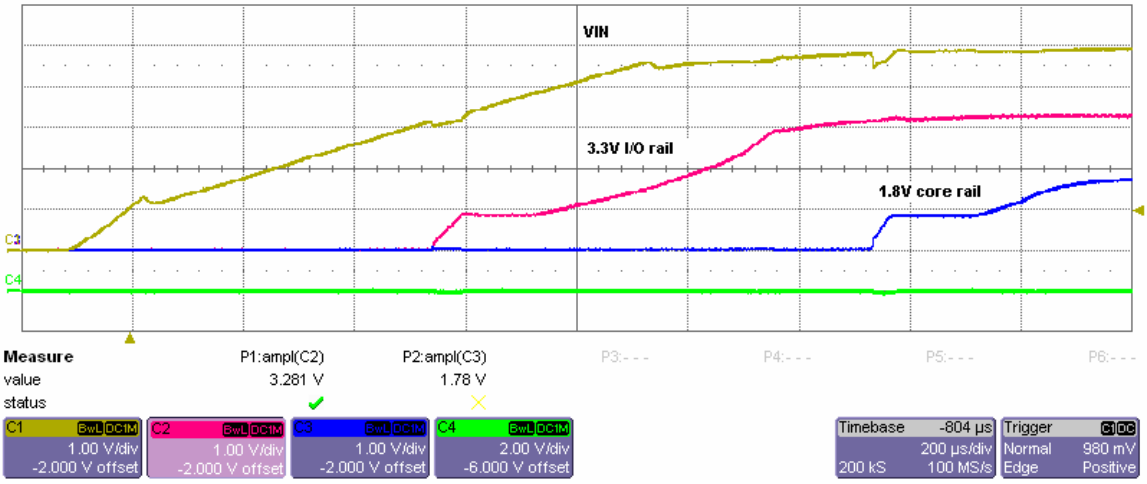

Figure 1 - Power up with V_{IN} = 5.0 V, /EN grounded

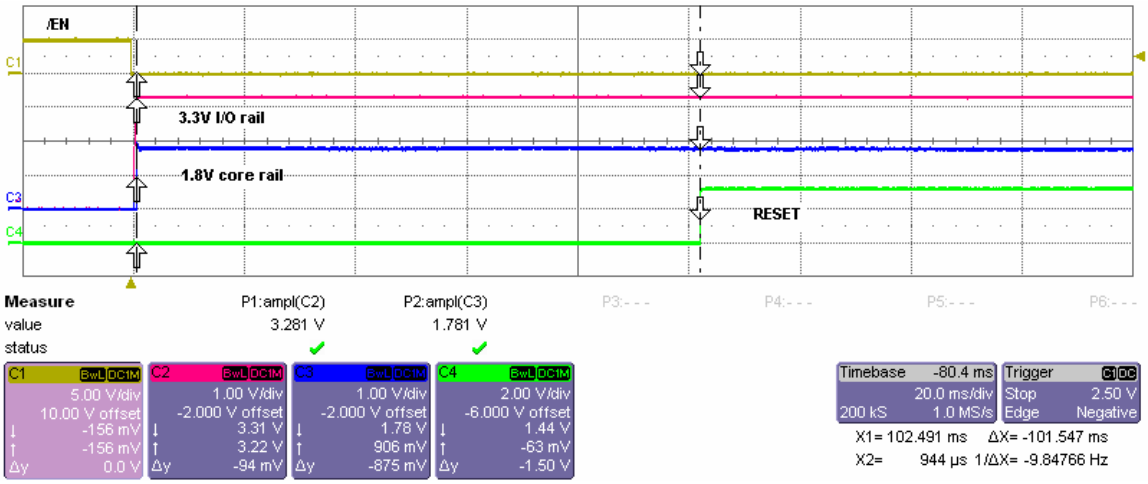

Figure 2 - Power up from enable when V_{IN} = 5.0 V

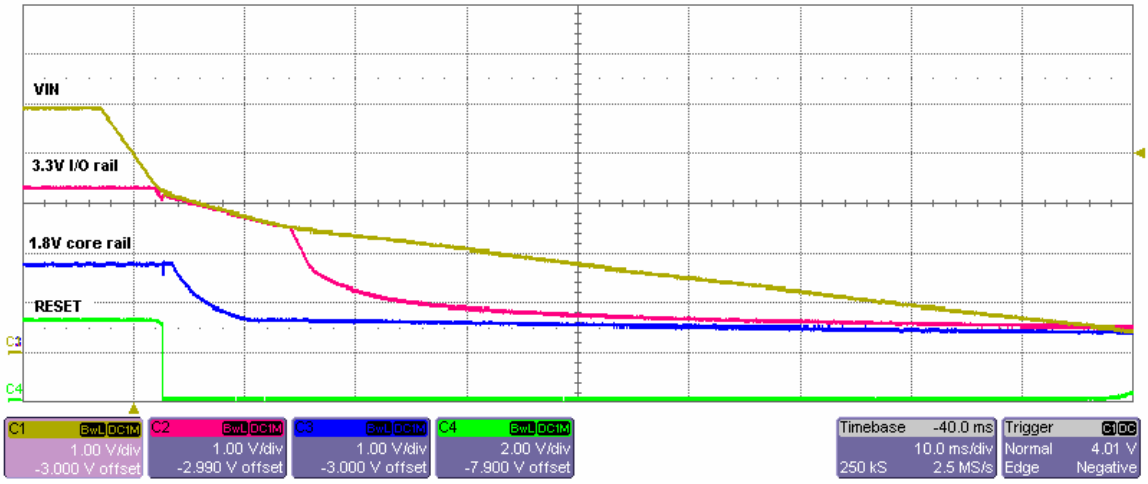

Figure 3 - Power down with V_{IN} = 5.0 V, /EN grounded

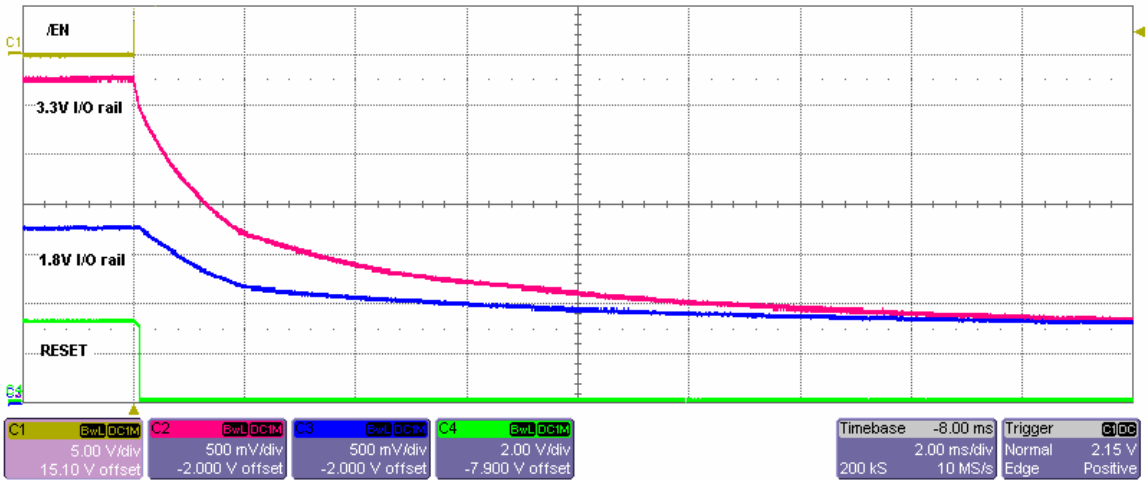

Figure 4 - Power down from enable when V_{IN} = 5.0 V

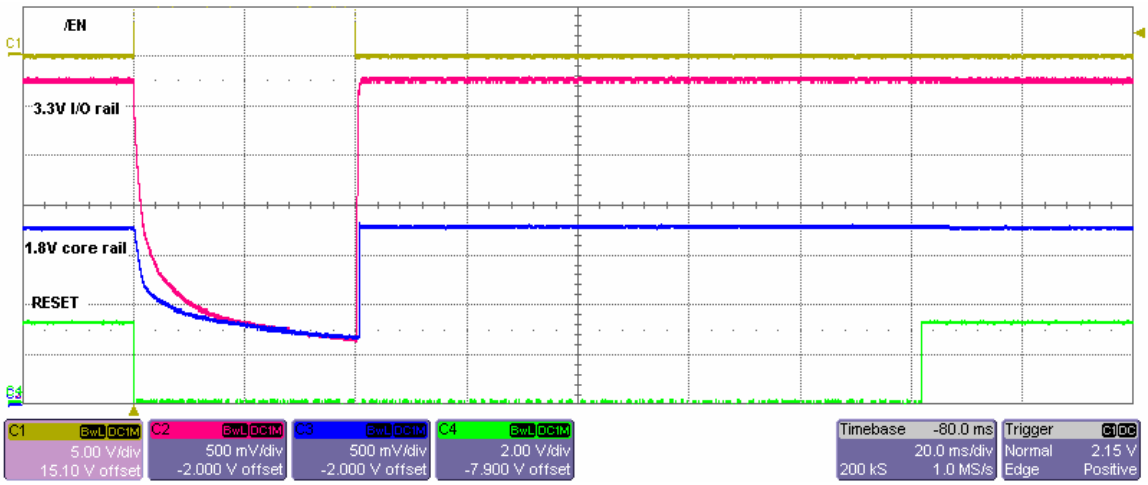

Figure 5 - RESET and recovery after V_{DD} = 3.3V fails

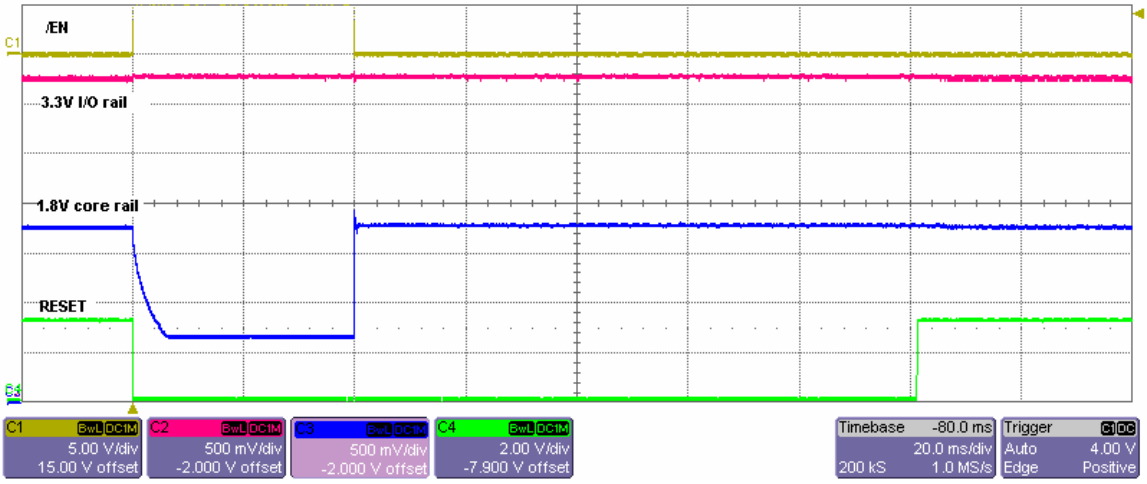

Figure 6 - RESET and recovery after V_{DD} = 1.8V fails

QUESTIONS?

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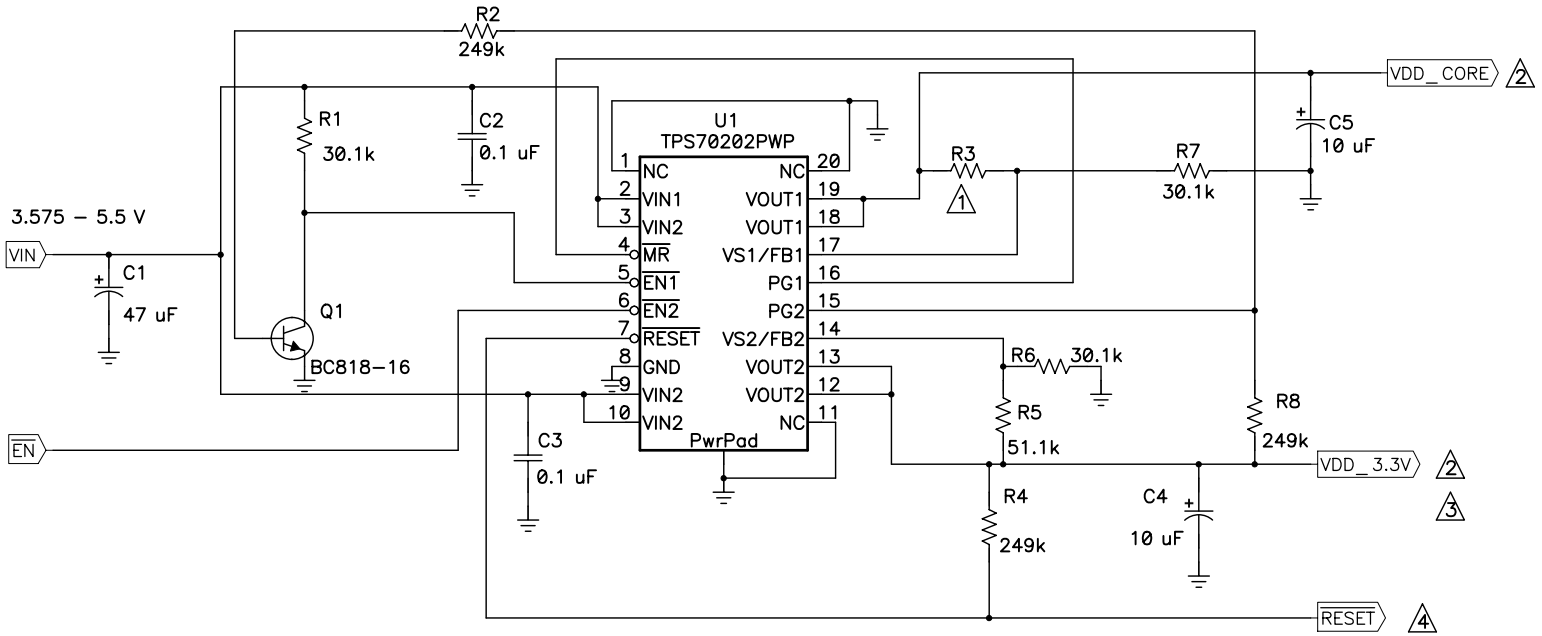

1

VDD_CORE	R3	VDD_CORE TOL	LDO SVS TOL
1.8V	14.3k	1.76–1.85	92%–98% VDD_CORE
1.9V	16.5k	1.84–1.95	92%–98% VDD_CORE

Assumes 1% resistors

2 Package power dissipation (Pd) determines maximum current.
Pd is a function of Vin and ambient temperature.

3

VDD_3.3V TOL	LDO SVS TOL
3.22–3.38	92%–98% VDD_3.3V

4 /RESET on the TPS70202 has a 120 ms delay and an open drain output which requires an external pullup resistor (R4 on this design).

Title	TMS320x281x DSP Attach Design 2 Low Cost	
Size: B	Number: PR413	Rev:
Date: 1/04/05		Drawn by:
Filename: pr413.sch		Sheet: of

Filename: PR413_bom.xls

Date: 12/16/2004

PR413 BOM

COUNT		RefDes	Description	Size	Part Number	Mfr
1	1	C1	Capacitor, Tantalum, 47-uF, 6.3-V, 1.4-ohm, 20%	3528(B)	293D476X6R3B2	Vishay
2	2	C2, C3	Capacitor, Ceramic, 0.1-uF, 25-V, X7R, 10%	0603	C1608X7R1E104KT	TDK
2	2	C4, C5	Capacitor, Tantalum, 10-uF, 6.3-V, 2.9-ohm, 20%	3528(B)	293D106X6R3B2	Vishay
1	1	Q1	Bipolar, NPN, 25-V, 500-mA, 310-mW	SOT23	BC818-16	Vishay
3	3	R1, R6, R7	Resistor, Chip, 30.1k-Ohms, 1/16-W, 1%	0603	Std	Std
3	3	R2, R4, R8	Resistor, Chip, 249k-Ohms, 1/16-W, 1%	0603	Std	Std
1		R3	Resistor, Chip, 14.3k-Ohms, 1/16-W, 1%	0603	Std	Std
	1		Resistor, Chip, 16.5k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R5	Resistor, Chip, 51.1k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	U1	IC, Dual-output LDO Regulator w/SVS	PWP20	TPS70202PWP	TI

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