Purpose

This document describes the characterization measurements made on the ADS5500 EVM. These measurements are summarized on a sheet of paper included with the EVM.

Test Setup

The test setup used to characterize the EVM is shown in Figure 1.

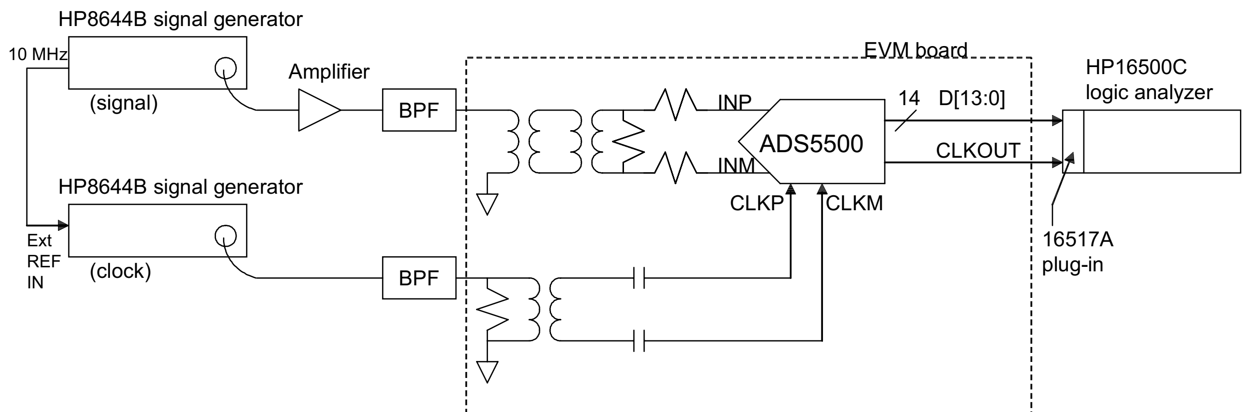

Figure 1. Characterization Test Setup

The signal to be sampled and the sampling clock are both generated with HP8644B signal generators that are frequency locked together (connecting the “10 MHZ” output on the back of one generator to the “EXT REF IN” input of the other generator or connecting both to an external 10 MHz reference). Both of these signals are passed through band-pass filters to reduce the harmonics and jitter generated by the test instrumentation. The characteristics of the filters are shown in Table 1. As would be expected, the narrower the filter bandwidths, the better the performance that will be observed.

Filter	Center Frequency	Lower 3dB Freq.	Upper 3dB Freq.
Signal filter	100 MHz	98.5 MHz	101.5 MHz
Clock filter	125.02 MHz	>123 MHz	<127 MHz

Table 1. Characteristics of Bandpass Filters.

The “signal” HP8644B’s output is passed through a wideband amplifier (e.g., THS900x) to provide sufficient amplitude to the input of the ADC. The amplifier has about 15dB gain with 50-ohm input and output impedances.

The signals are passed through transformers to the signal (INP and INM) and clock (CLKP and CLKM) inputs of the ADS5500 ADC. The 14-bit output data (D0 through D13) and clock (CLKOUT) are captured using an HP16500C logic analyzer mainframe with 16517A plug-in card. The captured data is relayed to a computer via GPIB for spectral analysis.

Let f_s be the sample rate of the ADC (125 MHz) – this is the rate of the clock frequency generated by the “clock” HP8644B in Figure 1. Then the Nyquist, or folding frequency, is half of this:

$$f_N = \frac{f_s}{2}.$$

Let the input sine wave (generated by the “signal” HP8644B in Figure 1) frequency be f_{in}. This sine wave is sampled by the ADC, which introduces harmonic distortion and noise. Harmonic distortion occurs at multiples of the input sine wave frequency. However, because the ADC is a sampling system, these harmonics are aliased into the frequency band from DC to Nyquist.

Location of the Input Frequency Harmonics

The location of the aliased signals can be pictured as shown in Figure 2. Each harmonic is aliased to a frequency corresponding to the distance of that frequency component from the nearest multiple of the sampling frequency, f_s.

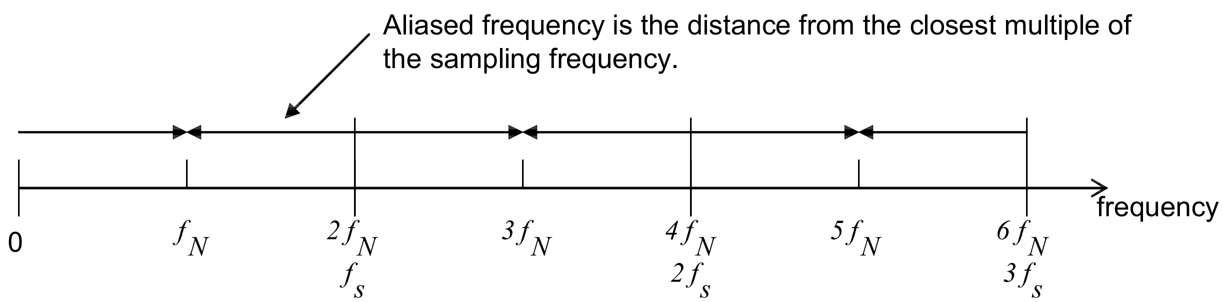

Figure 2. Location of frequency aliases

The harmonics of the input frequency, f_{in}, are $N \bullet f_{in}, N = 1,2,3,\ldots$. An algorithm to find the aliased frequency of the *N*th harmonic, based on finding the distance from the nearest multiple of the sampling frequency, is described as follows.

1. Calculate $n = int\left(\frac{Nf_{in}}{f_N}\right)$
2. If *n* is odd, then $f_{alias} = \left(\frac{n+1}{2}\right)(2f_N) - Nf_{in} = (n+1)f_N - Nf_{in}$.
3. If *n* is even, then $f_{alias} = Nf_{in} - \left(\frac{n}{2}\right)(2f_N) = Nf_{in} - nf_N$

For example, here’s a table showing the aliases for the first several harmonics of a 70 MHz input signal sampled at 125 MHz. That is, f_{in}=70 MHz and f_N=125 MHz / 2=62.5MHz.

N	$N \bullet f_{in}$ (MHz)	$n = int(Nf_{in}/f_N)$	even/odd	f_{alias} (MHz)
1	70	int(70/62.5)=1	odd	55
2	140	int(140/62.5)=2	even	15
3	210	int(210/62.5)=3	odd	40
4	280	int(280/62.5)=4	even	30
5	350	int(350/62.5)=5	odd	25

Definitions of Measured Parameters

When a signal of frequency f_{in} is put into an ADC converter sampling at a frequency f_s, the result when viewed in the frequency domain (by taking an FFT of the output of the ADC) consists of the fundamental frequency (the desired signal), harmonics of the fundamental frequency (aliased as described above), and noise due to quantization and other noise sources in the ADC. There are a number of figures of quality defined to describe how well the ADC reproduces the fundamental frequency while minimizing harmonic distortion and noise. This section of this document describes those figures of quality. Averaging multiple FFT's can reduce the variation in the measured figures of quality. An example plot and computation is shown for the figures of quality later.

The figures of quality are measured using a sine wave of a certain amplitude. If a sine wave that encompasses the entire input range of the ADC (a "full-scale" amplitude sine wave) is defined as 0 dBFS (decibels full scale), then the test signal is defined as a sine wave in relationship to this (for example, -1 dBFS, which would be a sine wave with 89% of the full-scale amplitude).

Spurious Free Dynamic Range (SFDR)

When looking at the spectrum of the reconstructed waveform from the ADC, the largest spike will be at the fundamental frequency or alias frequency if greater than the Nyquist frequency. There will also be several spikes due to harmonic distortion or noise. The Spurious Free Dynamic Range (SFDR) is the difference, expressed in decibels (dBc), between the RMS amplitude of the fundamental frequency and the next largest frequency spike.

Total Harmonic Distortion

Total Harmonic Distortion (THD) measures the distortion provided in the reconstructed ADC signal due to harmonics of the fundamental frequency being generated by the ADC. THD does not include noise sources in the ADC, and so separates distortion in the ADC from noise generation.

THD is defined as the ratio, expressed in decibels (dBc), between the RMS value of the fundamental frequency component and the RMS sum of the first several (possibly aliased) harmonics of the input frequency. Typically, the first 9 harmonics are used for the calculation. The example below illustrates the computation in detail.

SNR

The Signal-to-Noise ratio (SNR) is the complementary measurement to the THD. Here, a ratio is taken between the RMS sum of all the noise from DC (not including DC) to Nyquist that is not a (possibly aliased) harmonic of the fundamental and the power of an assumed sine wave of an amplitude that encompasses the full-scale input range of the ADC. That is, the RMS sum is taken over all the frequency bins that are not used in the THD calculation above, and therefore typically harmonics above the first nine are treated as noise. If one assumes that the noise is independent of the signal, then the SNR is appropriately expressed in terms of dBFS – decibels with respect to the power of a sine wave encompassing the full-scale of the ADC. Our measurements are expressed in dBFS.

SNRD

Sometimes called SINAD, this measurement expresses the signal-to-noise ratio of the converter considering both harmonic distortion and noise. SNRD (signal to noise+distortion ratio) is calculated by taking the RMS sum of all components except the fundamental summed from DC (not including DC) to Nyquist divided by the power of an assumed full-scale sine wave input. The noise ratio is expressed as decibels with respect to the power of an assumed sine wave that encompasses the full-scale input range of the ADC (dBFS).

Equivalent Number of Bits (ENOB)

Using either the SNR or SNRD, the equivalent number of bits of an ideal ADC can be calculated, assuming only quantization noise exists. Usually the SNRD is used. Assume that the ADC is being driven by a full-scale amplitude sine wave. Then the number of equivalent number of bits in an "ideal" ADC is limited only by its quantization noise:

$$SNRD = \frac{RMS\ value\ of\ the\ input\ sinewave}{RMS\ value\ of\ quantization\ noise}$$

Let the input range of the ADC be 0 to *A* volts. A full-scale sine wave has an RMS value of $\frac{A}{2\sqrt{2}}$. If the ADC has *N* bits, then the quantization voltage is $q = A \bullet 2^{-N}$. The quantization RMS noise is the quantization voltage divided by the square root of 12. (This is the RMS value of a uniform distribution of width *q* – see the Appendix.) So:

$$SNRD = \frac{\left(\frac{A}{2\sqrt{2}}\right)}{\left(\frac{A2^{-N}}{\sqrt{12}}\right)}$$

$$20\log_{10}(SNRD) = 20\log_{10}\left(\frac{\sqrt{12}}{2\sqrt{2}}\right) - 20\log_{10}\left(2^{-N}\right)$$

$$SNRD_{dB} = 1.76dB + 6.02N$$

Since *N* is the equivalent number of bits, then

$$ENOB = \frac{SNRD_{dB} - 1.76dB}{6.02}.$$

Selection of Sampling and Input Frequencies

This section describes the selection of the sampling and input frequencies for the ADC characterization. There are two requirements on these frequencies. The first is that the two frequencies be chosen so that there is no "leakage" in the FFT's spectral components. Secondly, the two frequencies are chosen so that input waveform is sampled at different phases each cycle, so that more information is added to the FFT every cycle.

Implicit in an FFT is the assumption that the signal being sampled is replicated infinitely in time before and after the sequence being sampled. "Leakage" results if there are discontinuities between the beginning and end of the sequence being sampled. In order to prevent leakage in the FFT, it is necessary to sample the input frequency so that the record time covers an integral number of periods of the input waveform. That is, the waveform has to be continuous when the record is duplicated forward and backward in time. The number of cycles of the input sine wave in the record is given by $N_{cyc} = N_{samp}\frac{f_s}{f_{in}}$. We want this N_{cyc} to be an integer to prevent leakage. Selecting the number of cycles to be an integer is called "coherent sampling." Coherent sampling meets the first requirement of preventing FFT leakage.

To meet the second requirement that the input waveform be sampled at different phases during each cycle of the input waveform, $N_{cyc} \div N_{samp}$ is chosen to be an irreducible fraction – that is, N_{cyc} and N_{samp} are chosen to be relatively prime. Because N_{samp} is typically chosen to be a power of two so that a radix-2 FFT can be used, it suffices to choose N_{cyc} to be an odd number.

Example. Let f_s=125.02MHz and f_{in}=66.6MHz. If N_{samp}=8192 (=2^{13}), then N_{cyc}=(8192/125.02)•66.6=4364.00 with the values given. So, these two values will give a good frequency transform with no leakage. But 4364 is not relatively prime to 8192 – they both are divisible by two. However, 4363 is relatively prime to 8192 (in fact, 4363 is a prime number, so it would work with any number of samples, not just a power of 2), so by choosing f_{in}=(125.02/8192)•4363=66.5847 MHz, then the input and sampling frequencies will be coherent, and the FFT will have the maximum amount of information in it.

An Example Computation

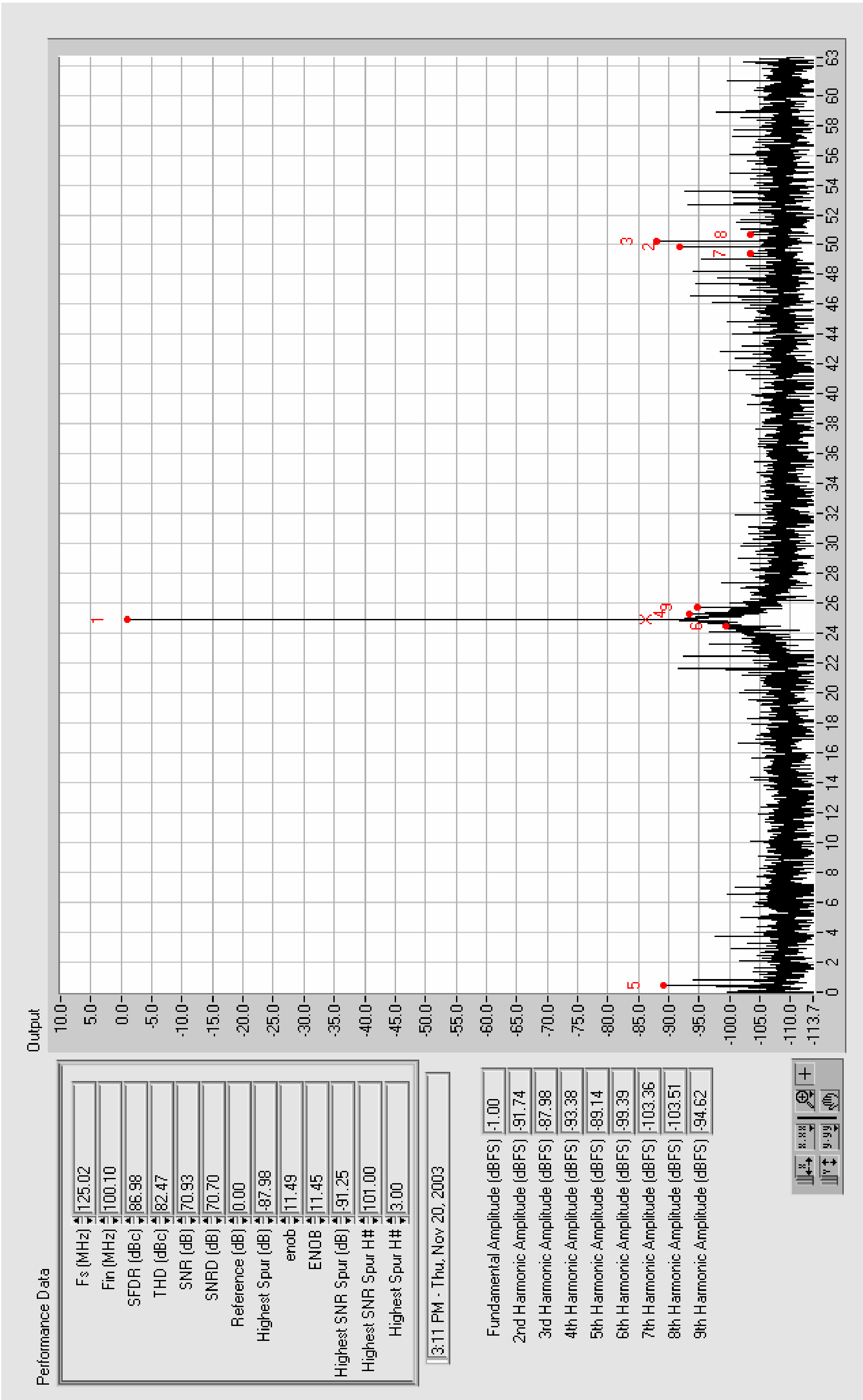

Figure 3. An example measurement of an ADC being run with a 100.09841 MHz input sine wave and 125.02 MHz clock

The spectrum shown in Figure 3 was obtained by taking an FFT of the output of an ADC when supplied with a 100.09841 MHz input signal and clocked with a 125.02 MHz clock using 8192 samples. Since (8192/125.02)•100.09841=6559.00, the chosen frequencies have met the constraints described above. The numerals above some of the spectral lines in Figure 3 are the harmonic numbers of those frequencies. Using the formulas derived to find the aliased frequencies of the harmonics of the input, the following table is constructed.

N	$N \bullet f_{in}$ (MHz)	$n = int\left(\frac{Nf_{in}}{f_N}\right)$	even/odd	f_{alias} (MHz)	Amplitude (dBFS)
1	100.0984	int(100.10/62.51)=1	odd	24.92	-1.00
2	200.1968	int(200.20/62.51)=3	odd	49.84	-91.74
3	300.2952	int(300.30/62.51)=4	even	50.26	-87.98
4	400.3936	int(400.39/62.51)=6	even	25.33	-93.38
5	500.4920	int(500.49/62.51)=8	even	0.41	-89.14
6	600.5905	int(600.59/62.51)=9	odd	24.51	-99.39
7	700.6888	int(700.69/62.51)=11	odd	49.43	-103.36
8	800.7873	int(800.79/62.51)=12	even	50.67	-103.51
9	900.8857	int(900.89/62.51)=14	even	25.75	-94.62

SFDR

The spurious free dynamic range is the difference between the fundamental amplitude in dB and the highest noise spike. The noise spike is the 3rd harmonic and is listed as “highest spur.”

SFDR=(-1.00dB) - (-87.98 dB)

SFDR=86.98dB

THD

The total harmonic distortion is the ratio of the RMS voltage of the fundamental divided by the RMS sum of the harmonic voltages. Using the relationship that volts=$10^{(dB/20)}$, dB=$20\log_{10}$(volts), and summing harmonic powers in the denominator, the calculation proceeds:

$$THD_{dB} = 20log_{10}\left(\frac{10^{-1.00/20}}{\sqrt{10^{-91.74/10} + 10^{-87.98/10} + 10^{-93.38/10} + \cdots + 10^{-94.62/10}}}\right) = 82.47 \text{ dB.}$$

The harmonic number of the largest harmonic spike (considering the first 9 harmonics) is shown as the “Highest Spur H#” (highest harmonic spur number) in the summary table. Here, the highest harmonic spike is the 3rd harmonic.

SNR

The SNR is defined as the RMS sum of all the frequencies that are not harmonics from DC (not including DC) to Nyquist divided by the power of an assumed sine wave using the entire full-scale voltage range of the ADC. For the data shown, the SNR is 70.93dBFS.

The highest noise spike that is not a first through ninth harmonic is marked with an “X.” In case the highest spike is a higher harmonic, its harmonic number is calculated as the “Highest SNR Spur H#” (highest SNR spur harmonic number). In this case, it is the 101st harmonic frequency, indicating that this spur is actually not due to harmonic distortion. Since the “X” is on the side of the fundamental, it’s probable that the fundamental has widened due to jitter and the test software has classified this as a spur.

SNRD

The SNRD is defined as the sum of the power of all the frequencies from DC to Nyquist, not including DC, divided by the power of an assumed sine wave using the full-scale voltage range of the ADC. This value should be worse than the SNR, since it includes both SNR and THD in it. For the data shown, the SNRD is 70.70 dBFS.

enob

This is the equivalent number of bits using the SNR (not SNRD) value:

$$enob = \frac{SNR_{dB} - 1.76dB}{6.02} = \frac{70.93dB - 1.76dB}{6.02} = 11.49\ bits$$

ENOB

This is the equivalent number of bits using the SNRD (signal to noise ratio including distortion):

$$ENOB = \frac{SNRD_{dB} - 1.76dB}{6.02} = \frac{70.70dB - 1.76dB}{6.02} = 11.45\ bits$$

Appendix. RMS Value of Quantization Noise

This appendix develops the RMS noise due to quantization in an ADC.

As the *N*-bit ADC samples an input waveform, it is likely that the sampled voltage is not exactly at one of the 2^N quantization levels. So, at every sample, some noise is introduced because of the difference between the sampled voltage and the quantization levels.

Assuming that the input waveform and clock frequency waveform are uncorrelated, it is reasonable to assume that the error between the quantized voltage levels and the sampled voltage is uniformly distributed between –*q*/2 and +*q*/2, where the voltage between quantization levels is called *q*. See Figure A-1. In order to describe the noise statistically, we need to determine the rms value of the noise.

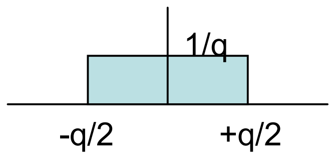

Figure A-1. Uniform distribution of quantization noise

The RMS value of the zero-mean distribution *f(x)* defined by the figure is:

$$RMS = \sqrt{\int_{-q/2}^{q/2} x^2 f(x)dx} = \sqrt{\frac{1}{3}\left(\frac{q^3}{8} + \frac{q^3}{8}\right)\frac{1}{q}} = \frac{q}{\sqrt{12}}.$$

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