High Speed 111:
Analog to Digital Converter
Basic Customer Training

Overview of Topics

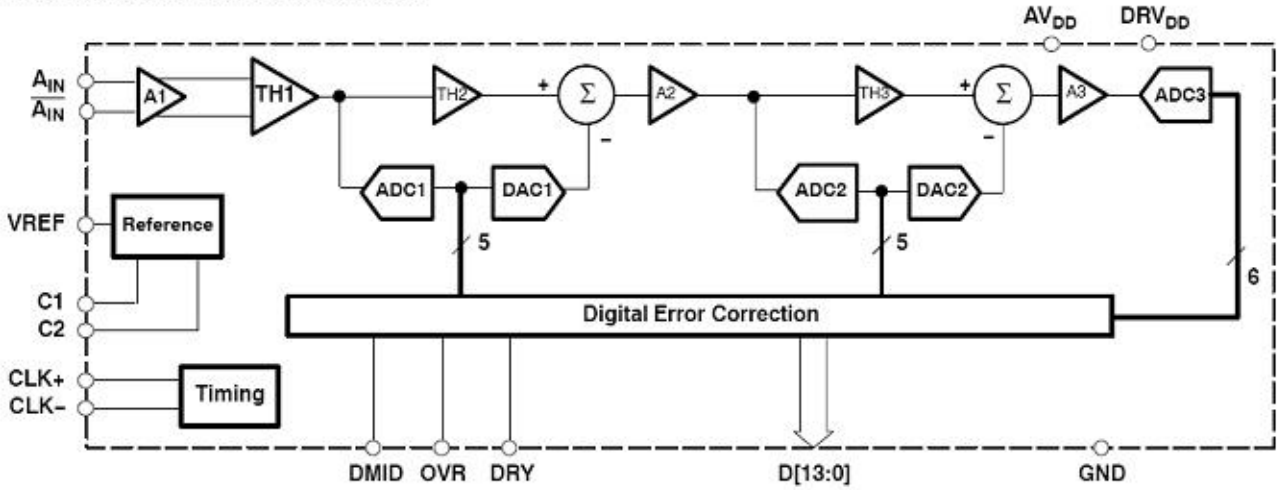
- What is a High Speed ADC?
  - Pipeline ADC
- ADC Parameters
  - SNR, SFDR, SINAD, THD, ENOB
  - Input Bandwidth
  - Clock Rate
  - dBc vs dBFS
- Sampling
  - Nyquist Zones
  - Aliasing
- Digital Outputs

What is a High Speed ADC?

Pipeline ADC – Example ADS5424

- Notice that there are 3 sub-ADCs
  - Sub-ADC1 = 5 bits
  - Sub-ADC2 = 5 bits
  - Sub-ADC3 = 6 bits
  - = 16 bits for a 14-bit ADC ?
- ADS5424 is an 105MSPS 14 bit ADC
  - The extra bits are used for internal error correction, only 14 bits come out
  - The Clock Latency is 3 cycles – it takes three periods of the clock for the converted signal to come out in digital format

FUNCTIONAL BLOCK DIAGRAM



ADC Parameters

ADC Parameters

- SNR, SFDR, SINAD, THD, ENOB
- Input Bandwidth
- Performance vs Bandwidth
- Clock Rate
- dBc or dBFS

SNR/SFDR/SINAD/THD/ENOB

- These are all measures of a converter's ability – related to the frequency domain
  - SNR = Signal-to-Noise Ratio
  - SFDR = Spurious-Free Dynamic Range
  - SINAD = Signal-to-Noise and Distortion Ratio
    - Sometimes written as SNDR
  - THD = Total Harmonic Distortion
  - ENOB = Effective Number Of Bits

SNR, THD, SFDR

- SNR is the ratio between the power measured in a single tone and the rms sum of the noise (minus harmonics at least 2-6, sometimes more)
- THD is the ratio between the power measured in a single tone and the sum of the power in harmonics (usually at least the 1st five harmonics, sometimes more)
- SFDR is the ratio between the power measured in a single tone and the highest spur measured (whether harmonic or not)
- Notice – SNR, though a measure of noise, contains LOTs of harmonics – any not counted in THD

SINAD and ENOB

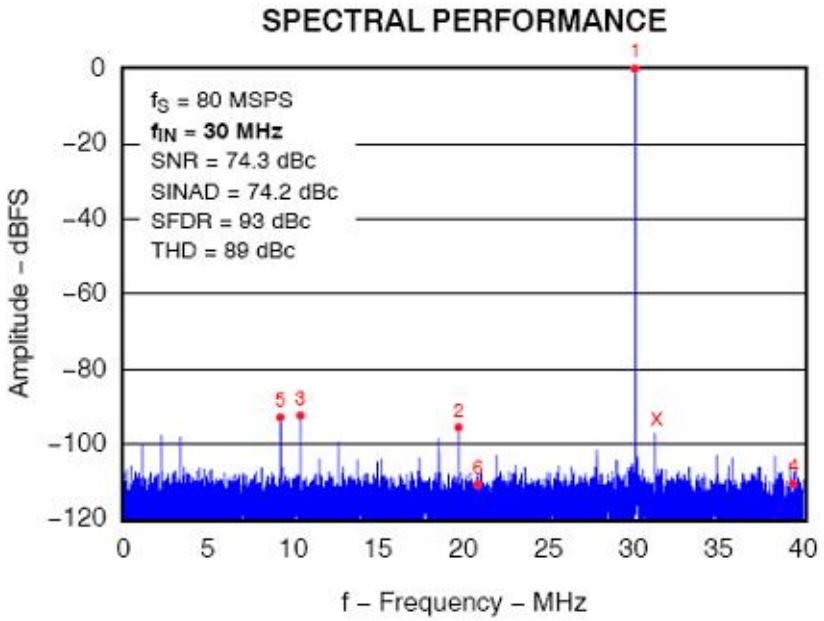
- SINAD is the ratio between the power measured in a single tone and the rms sum of the noise and the distortion
- It can be calculated directly by the summation of THD and SNR because that is what it is.
- ENOB is an overall measure of how perfect the ADC is, and SINAD tells us how perfect the ADC is, so ENOB is calculated from SINAD

- ENOB = (SINAD – 1.76)/6.02

Example ENOB calculation

- SINAD is 74.2dBc
- ENOB =
  - (74.2 – 1.76)/6.02
  - = 12.03bits
  - From a 14-bit ADC
  - It is typical as the bits > 10 for there to be a noticeable difference between bits (14) and effective bits (12.03)

ADS5423 80MSPS 14bit ADC



This particular plot notes the locations of harmonics 2-6.
Notice they also alias into the Nyquist band (0-40MHz) at 80MSPS.

Input Bandwidth

- The ADS5463 (12b/500M ADC) has a 2+GHz Input Bandwidth
- This only means that as the input frequency is swept from 0-~2.3GHz, the signal will not lose more than 3dB of power, it says nothing about the performance of the ADC at 2GHz
- Usually the performance of the ADC has degraded long before its Input Bandwidth is reached
- This is also referred to as FPBW
  - Full Power Bandwidth

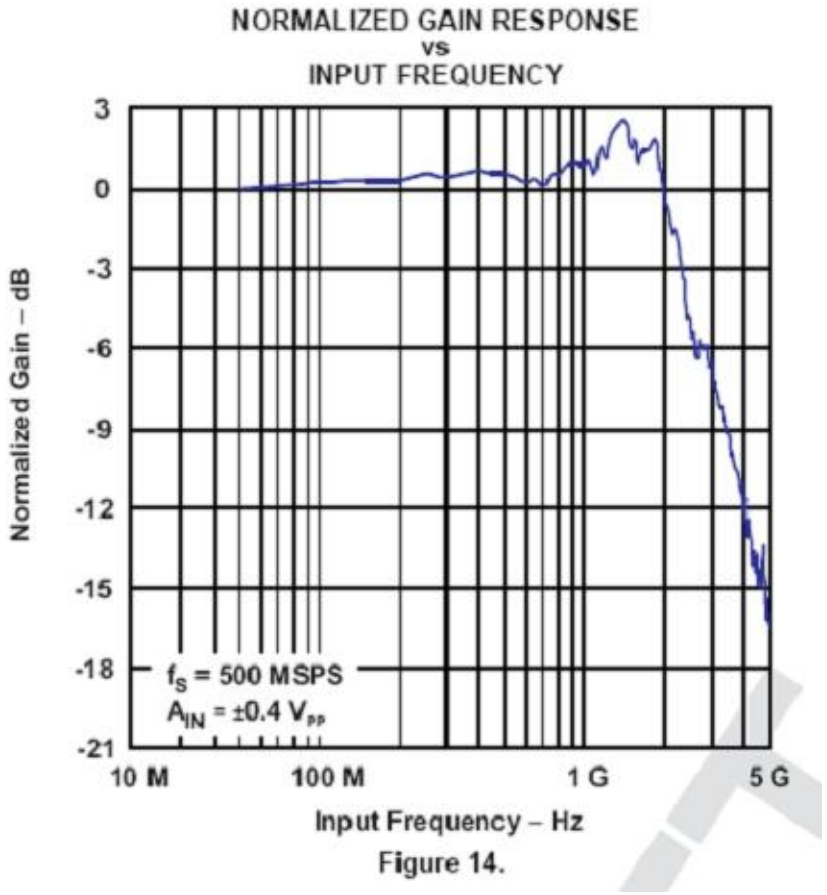
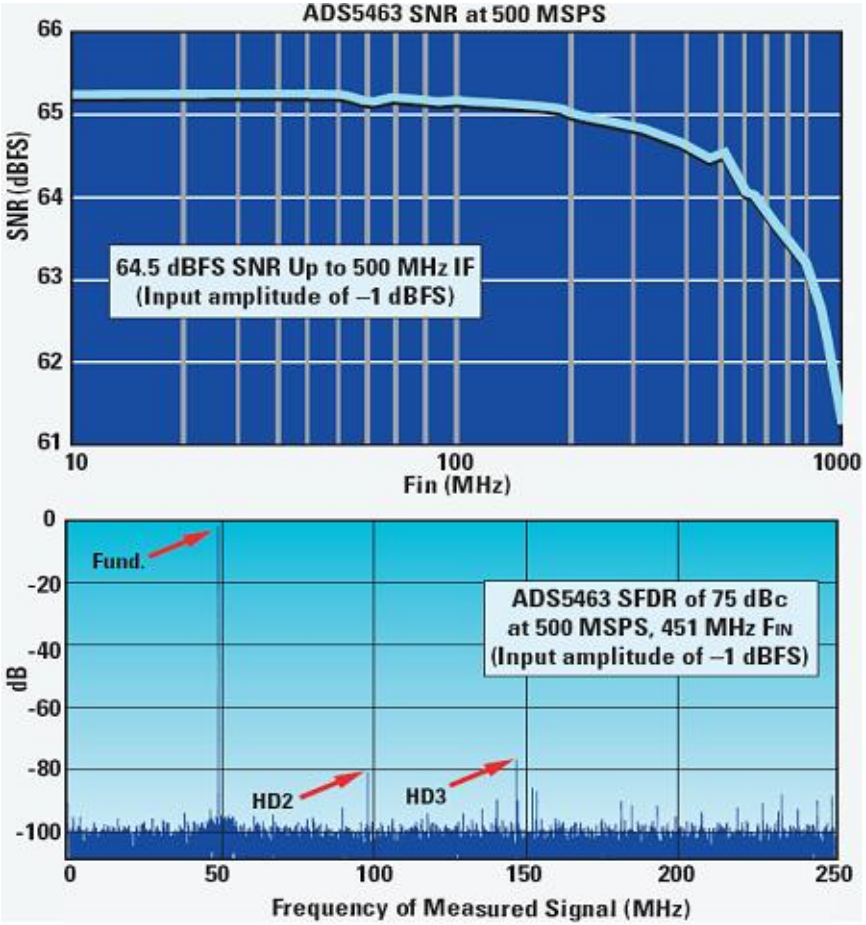


Figure 14.

Note: this plot does not yet appear like this in the datasheet, but it will

Performance vs Input Bandwidth

- Performance Bandwidth is a subjective term we use to indicate approximately where the ADC stops being as good as advertised
- Even though the ADS5463 has a 2+GHz Input Bandwidth, the SNR is down about 3dB at ~950MHz, so from an SNR perspective, the 'performance bandwidth' is about 1GHz (again, subjectively speaking)
- If SFDR is your key parameter of interest, you may have a different opinion than the result that was based on the SNR – also very subjective
- You can use the ADC with almost any input frequency you want, so long as you can live with the loss in power if you exceed the FPBW and the loss in performance as the input frequency increases



Clock Rates

- ADC Clock rates are *usually* specified as xSPS (such as MSPS – Mega Samples Per Second) instead of MHz to *attempt* to make it clear that you are talking about the clock frequency and not the analog input frequency
- But, xSPS is still xHz (usually)
- 100MSPS = 100MHz clock
- 1GSPS = 1GHz clock
- 100kSPS = 100 kHz clock

- It is possible that the clock frequency and the sample rate are not in fact the same, but they usually are

dBc vs dBFS

- dBc – measurement made relative to the carrier power
- dBFS – measurement made relative to the converter's Full Scale
  - The converter's full scale is 0dBFS, but it is VERY common for recommended full scale to be -1dBFS
  - This is due to the fact that you usually want to allow a little bit of conversion headroom in case there is noise or a slight DC shift in the analog signal…otherwise…you clip.

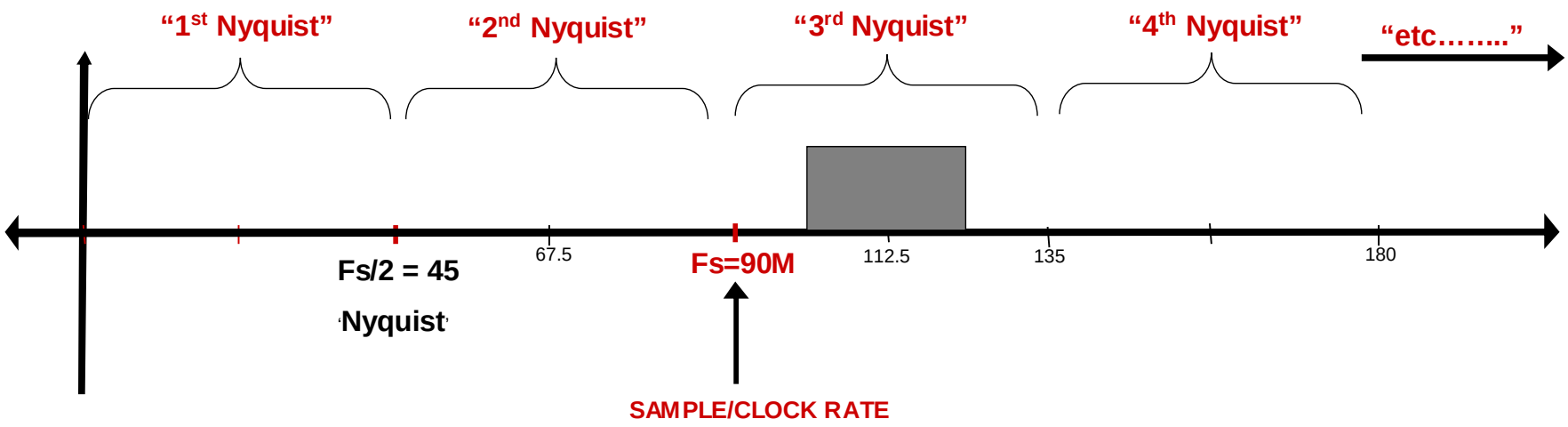
- Know the difference between dBc and dBFS!

Sampling and Nyquist

What did Harry Say about Sampling?

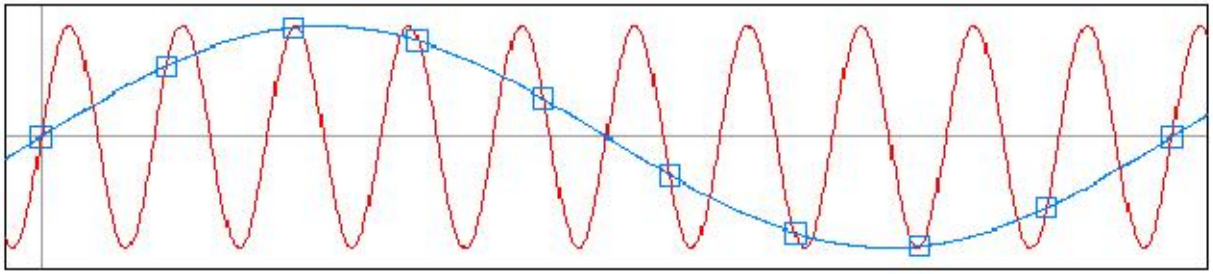
- The **Nyquist Frequency**, named after Harry Nyquist or the Nyquist–Shannon sampling theorem, is half the sampling frequency of a discrete signal processing system.
- The **Nyquist Rate** is the minimum sampling rate required to avoid aliasing when sampling a continuous signal. In other words, the Nyquist rate is the minimum sampling rate required to allow *unambiguous* reconstruction of a band-limited continuous signal from its samples. If the input signal is real and band-limited, the Nyquist rate is simply twice the highest frequency contained within the signal.

Nyquist Zones



What is Aliasing?

- Aliasing - two different sinusoids give the same digital samples
  - If F_s is the Sampling Frequency (clock rate)
  - a high frequency $F_{red} = 10/9 * F_s$
  - and a low frequency at $F_{blue} = 1/9 * F_s = F_{red} – F_s$
  - Both look like $1/9 * F_s$ to the ADC
  - Thus one might say,
    - "the frequency at F_{red} is aliased down, or *under-sampled*, to be at frequency F_{blue} at the ADC digital outputs in the spectral domain"
    - Or better yet, "the ADC can't tell the difference"



example: Wikipedia.org

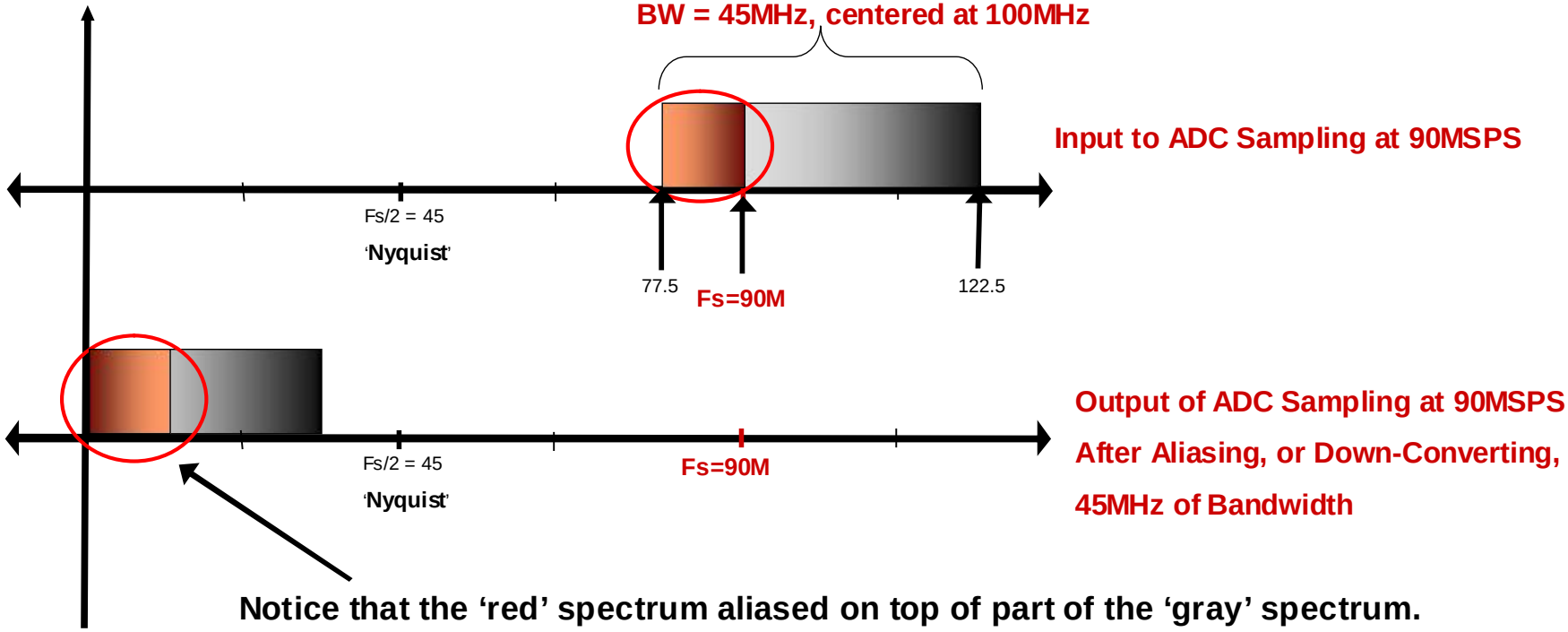
Under-sampling (Aliasing)

- We just down-converted a signal from a high frequency to a lower frequency – that sounds useful
  - This is called Under-sampling
- This usually requires an analog frequency mixer
- What is not always clear in the definition of the Nyquist Rate is that it refers to the **bandwidth** of the signal, not the frequency
  - In the example given, the bandwidth of each signal is practically zero – these are discrete tones at 1/9 and 10/9 of Fs
  - But signals with no bandwidth contain little information and are therefore not usually very useful for communication systems
  - So let's look at aliasing with some bandwidth involved….

Bad Aliasing

- Harry Nyquist did say something about aliasing that sounded bad
- Let me explain by example:
- Let Fs = 90MSPS
- Half of 90M = 45MHz
- So according to Nyquist, you can sample up to 45MHz of bandwidth using a sample rate of 90MSPS
- However (here is where aliasing could be bad) – if you try to put a signal 45MHz wide at 100MHz, and sample at 90MSPS, the ADC will get confused
- Frequency to be sampled occupies 77.5MHz – 122.5MHz
- It will ‘fold’ or ‘alias’ the frequency content from 90M to 122.5MHz down to 0 to 32.5MHz
- It will alias the frequency content from 77.5M to 90MHz to 0 to 12.5MHz

Bad Aliasing (graphically speaking)



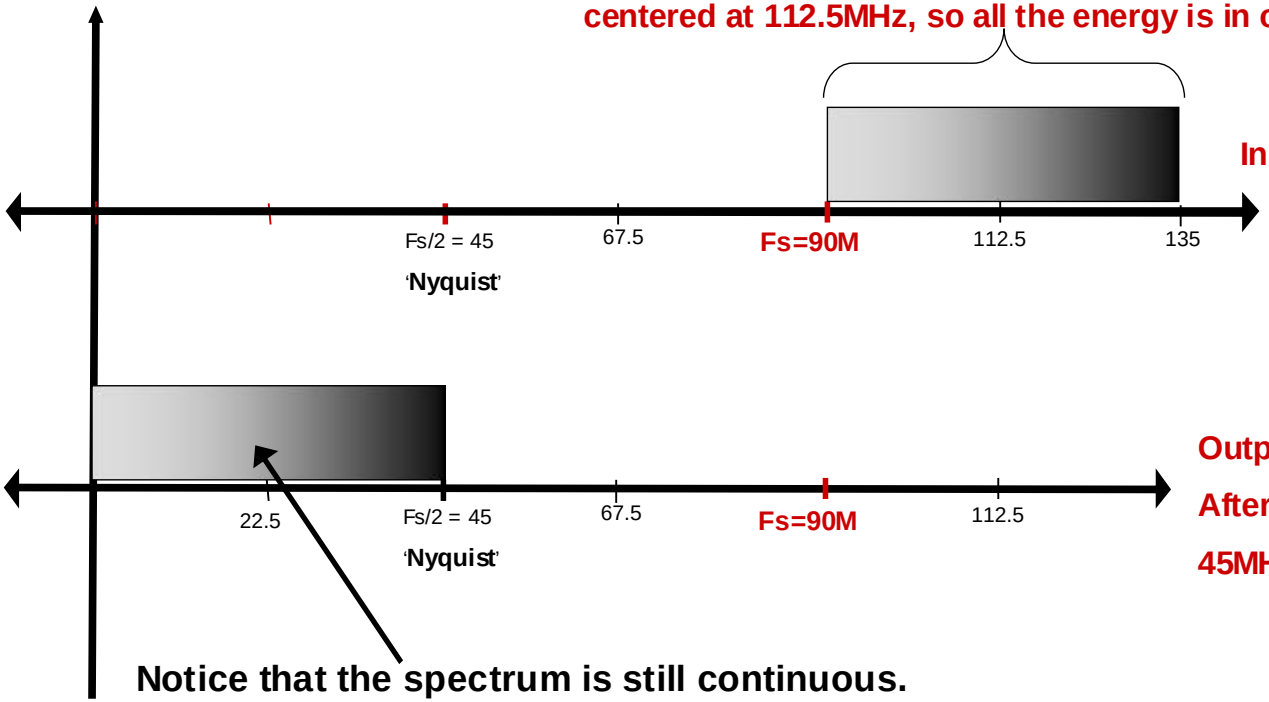
Notice that the 'red' spectrum aliased on top of part of the 'gray' spectrum.

Notice also that the red horizontally inverted, while the gray did not

This would not be okay – a digital down-converter (DDC) would not be able to recover the information.

Good Aliasing

As drawn here, this is 1 modulated carrier with a BW = 45MHz, centered at 112.5MHz, so all the energy is in one 'Nyquist Zone'



Input to ADC Sampling at 90MSPS

Output of ADC Sampling at 90MSPS

After Aliasing, or Down-Converting, 45MHz of Bandwidth

Notice that the spectrum is still continuous.

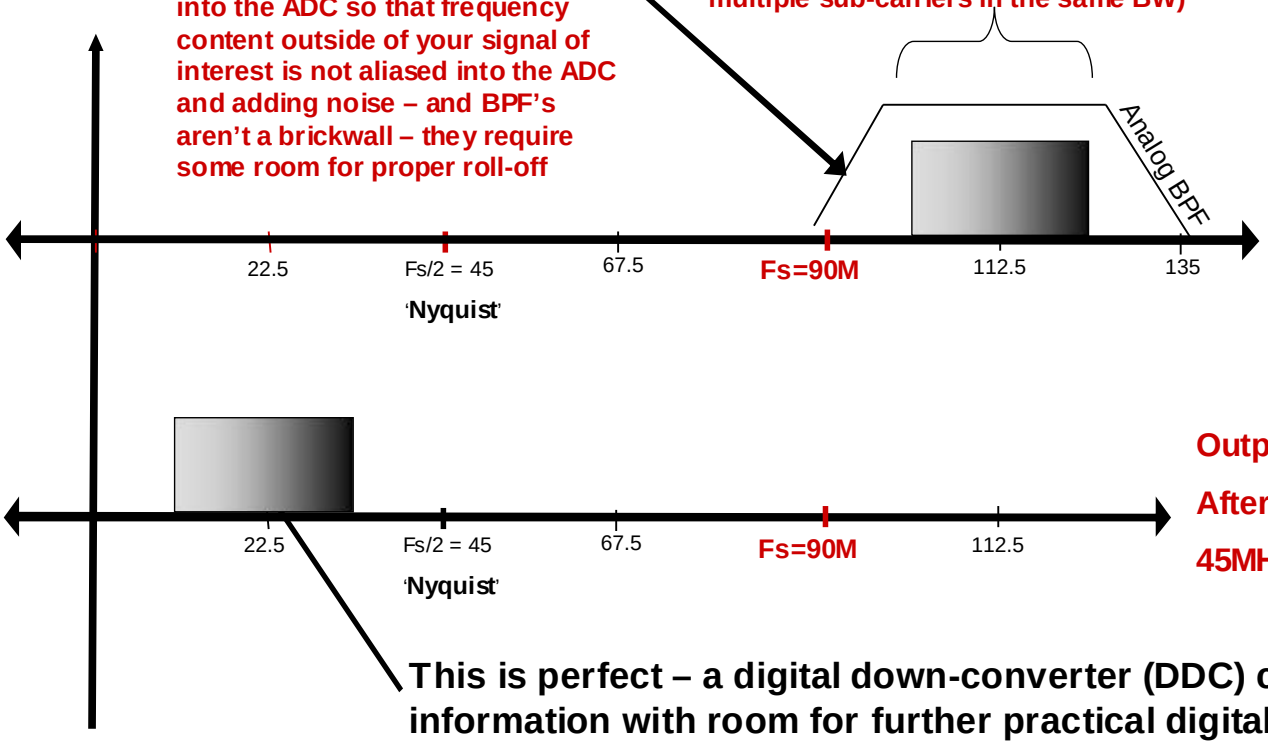
Notice that the color is not horizontally inverted – this is because we used an 'odd' nyquist zone (the 3rd). If we had used an 'even' zone, the color would reverse – it is spectrally inverted. This is not a bad thing, but might need to be known in order to process the band.

Many radio designs take full advantage of 'good aliasing' to eliminate an entire analog frequency down-conversion stage – saving board space, power, and money

Practical Aliasing Example

In the real world, you need to band-pass filter the signal before going into the ADC so that frequency content outside of your signal of interest is not aliased into the ADC and adding noise – and BPF's aren't a brickwall – they require some room for proper roll-off

As drawn here, this is 1 modulated carrier with a BW = 22.5MHz (Fs / 4), centered at 112.5MHz (it could be multiple sub-carriers in the same BW)



Input to ADC Sampling at 90MSPS

Output of ADC Sampling at 90MSPS

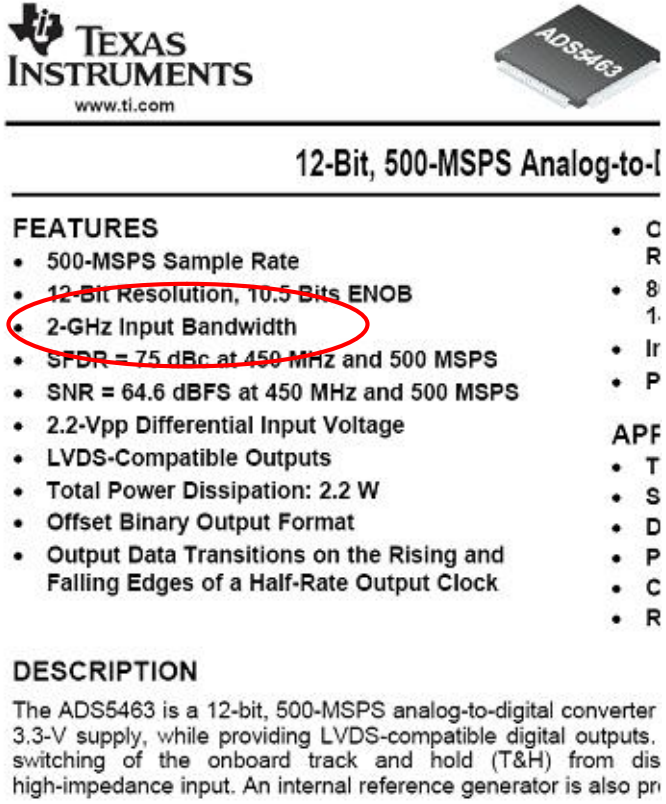
After Aliasing, or Down-Converting, 45MHz of Bandwidth

This is perfect – a digital down-converter (DDC) can recover the information with room for further practical digital filtering and digital frequency mixing – usually to baseband.

Many radio designs take full advantage of 'good aliasing' to eliminate an entire analog frequency down-conversion stage – saving board space, power, and money

Can all ADCs Under-sample?

- Pipeline ADCs are usually designed to have Input Bandwidth that exceeds the intended operating range or 'Performance Bandwidth'
- The ADS5463, with a 2GHz Input Bandwidth, could sample input frequencies up to 2GHz (carrier, not BW) at 500MSPS – but the performance is frequency dependent
- There are ADCs that cannot under-sample, which are sometimes called Nyquist Converters, and are usually high precision and have much slower sample rates



TEXAS INSTRUMENTS
www.ti.com

ADS5463

12-Bit, 500-MSPS Analog-to-

FEATURES

- 500-MSPS Sample Rate
- 12-Bit Resolution, 10.5 Bits ENOB
- 2-GHz Input Bandwidth
- SFDR = 75 dBc at 450 MHz and 500 MSPS
- SNR = 64.6 dBFS at 450 MHz and 500 MSPS
- 2.2-Vpp Differential Input Voltage
- LVDS-Compatible Outputs
- Total Power Dissipation: 2.2 W
- Offset Binary Output Format
- Output Data Transitions on the Rising and Falling Edges of a Half-Rate Output Clock

DESCRIPTION

The ADS5463 is a 12-bit, 500-MSPS analog-to-digital converter 3.3-V supply, while providing LVDS-compatible digital outputs. switching of the onboard track and hold (T&H) from dis high-impedance input. An internal reference generator is also pr

ADC Digital Outputs

CMOS Outputs

- Parallel CMOS (3.3V logic) outputs
  - Pro: Simple to interface to, lower power at slow Fclk
  - Con: Requires lots of IO
  - Con: Large, fast output edges can create “spurs” on board if you are not careful.
  - Example: ADS5500

LVDS Outputs

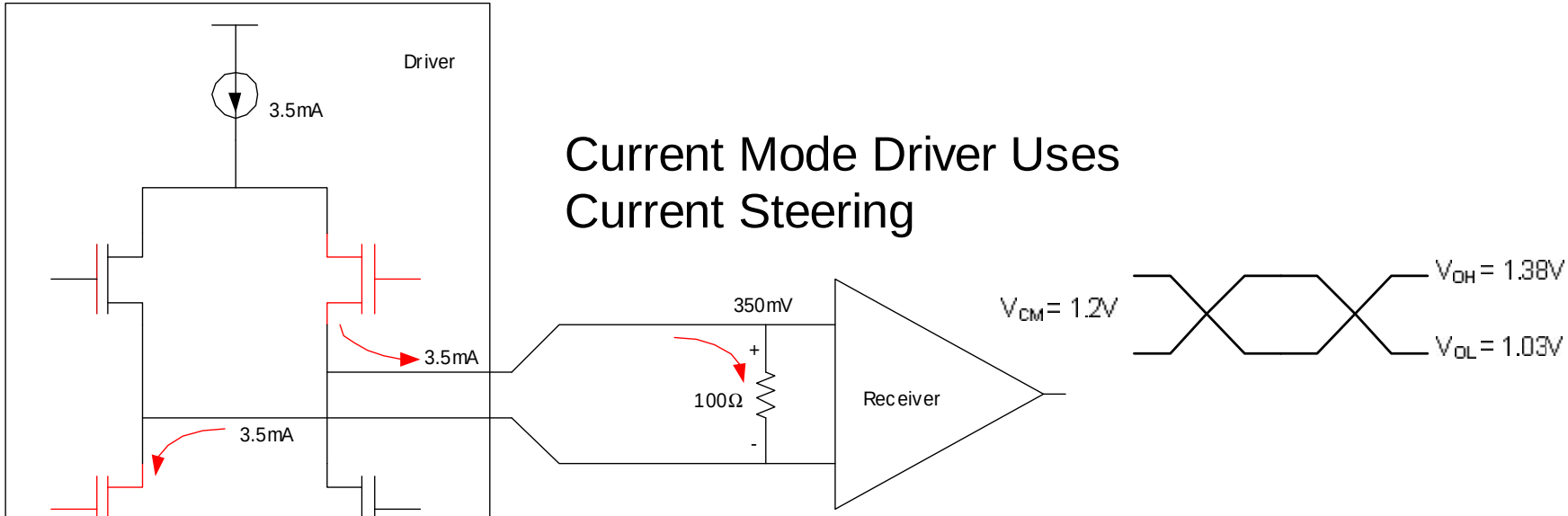
- LVDS (ANSI/TIA/EIA-644)
  - Differential Output Swing 700mVpp (350mVpp on each side)
    - Vcm = 1.2V
    - Common mode noise immunity
  - Current mode output, Iout = 3.5mA
    - 100 ohm termination needed at receiver
    - Class A output has low dI/dt noise
    - Supply independent
  - Lower EMI on board designs.
  - Ex. ADS5547, ADS5463, ADS6445

Parallel LVDS

- LVDS
  - DDR can reduce clocking frequency by a factor of 2
    - When 1 bit is sent per digital output
    - Example ADS5463
    - Sometimes called ‘half rate DDR’
  - DDR clocks data bits on both rising and falling edges
  - Or……
  - DDR cuts the output pin count by 2, allows for smaller packages
    - When 2 bits are sent per digital output
    - Example ADS5547
    - Sometimes called ‘full rate DDR’
  - DDR is supported by FPGAs (Altera, Xilinx)

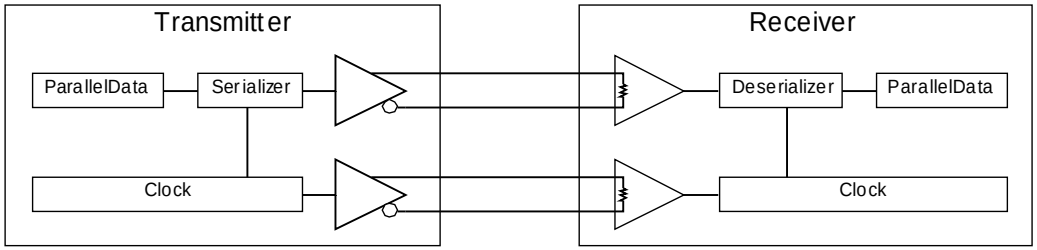
LVDS

Simplified LVDS Diagram



Current Mode Driver Uses
Current Steering

Serialized LVDS Diagram



Output Timing

- To achieve proper board operation between an ADC's outputs and the digital device receiving the data (like an FPGA), a timing analysis will be required
- The output timing parameters of the ADC must be carefully studied along with the setup/hold times of the receiving circuit
- Board design is important – all digital lines should be carefully matched in length and impedance
- Many times the clockout of the ADC is used to capture the data into the digital device
  - The clockout may have to be time delayed in order to achieve proper timing
- This is a detailed topic that we will avoid in this material – but beware of it!
  - It causes many headaches for customers and our apps support team

More Questions?

- Need help selecting a high speed ADC or DAC for your system?
- More questions about using a high speed ADC or DAC?
- Email:

  hs_converter_apps@list.ti.com