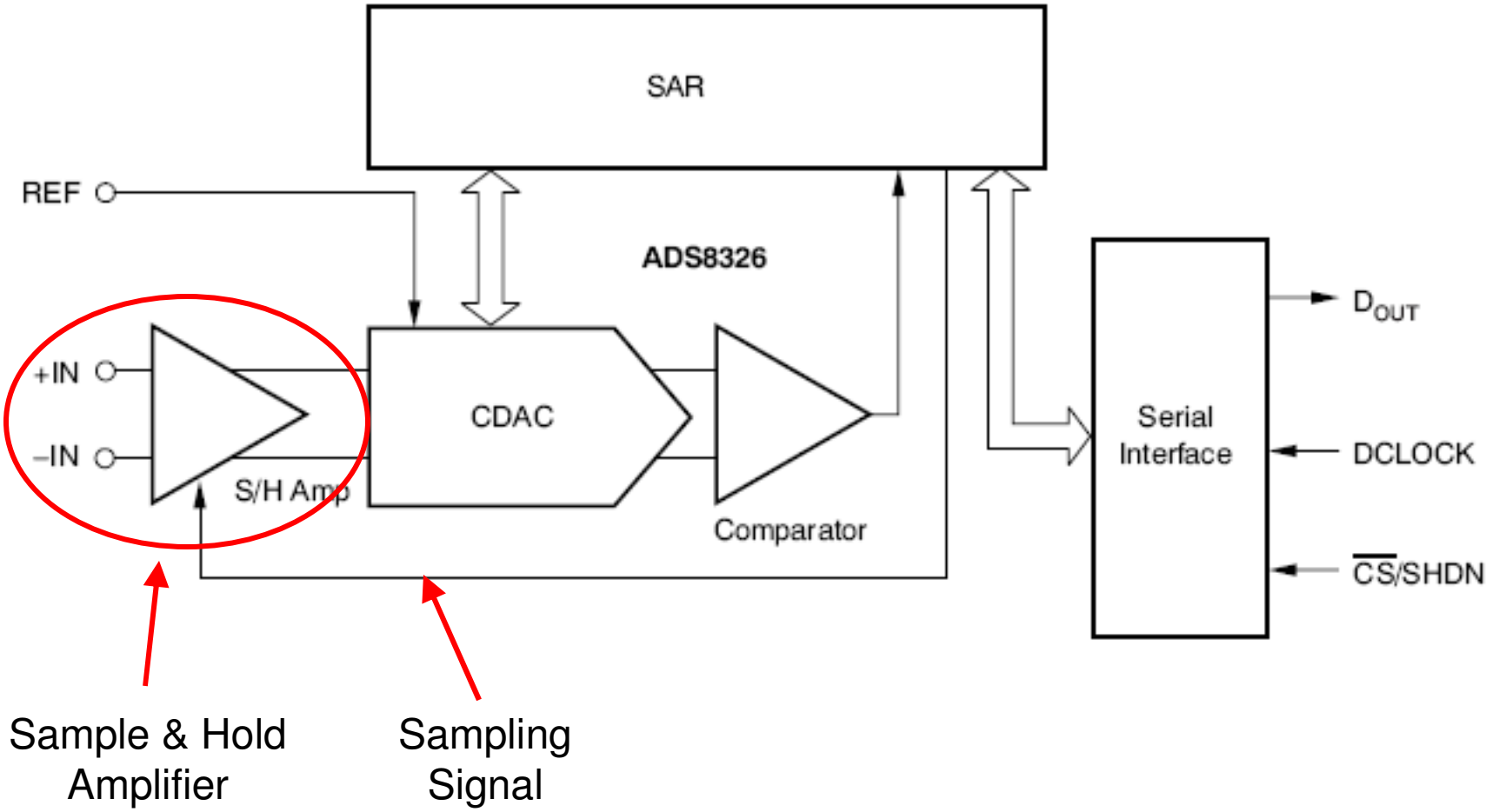
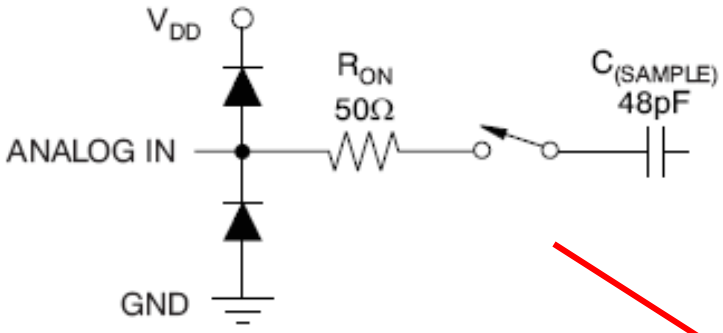
Op Amp Drive for SAR Converter:

Four Steps Design

SAR ADC's Block Diagram

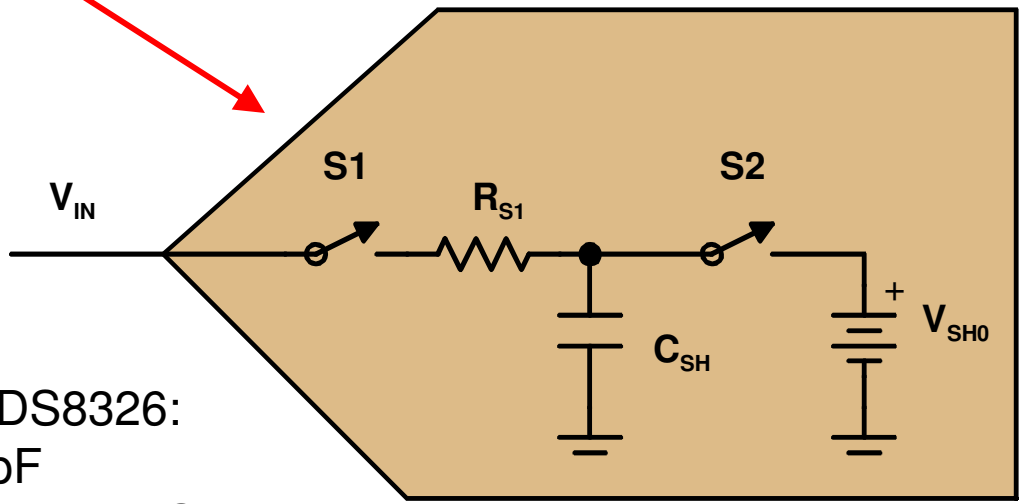


Equivalent Input Circuit



Diode Turn-On Voltage: 0.35V
Equivalent Analog Input Circuit

SAR ADC
Sample & Hold Amplifier



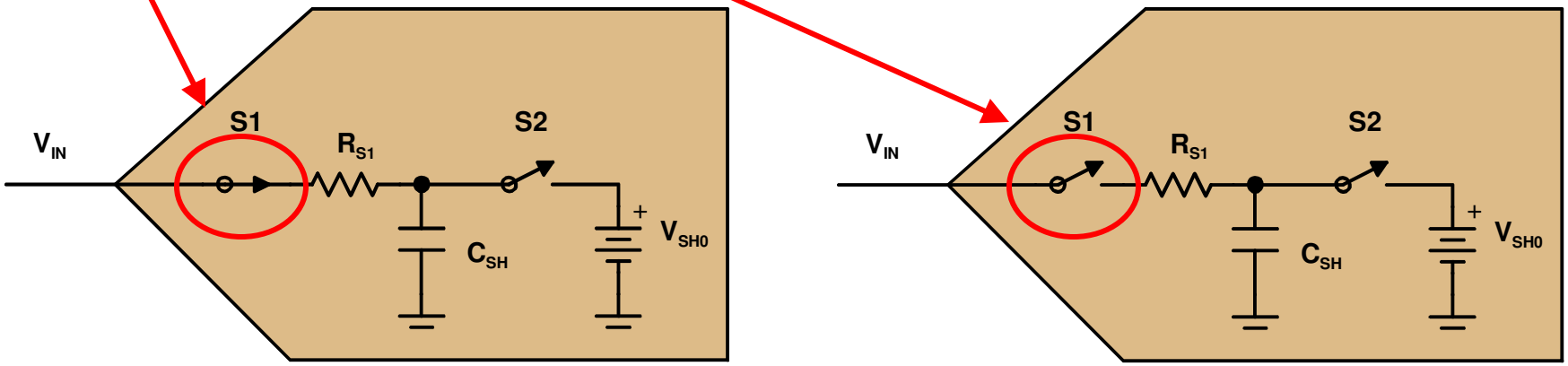
From the Data Sheet for ADS8326:
- Sampling capacitor is 48pF
- Sampling switch resistance is 50 Ω

Sample and Conversion Process

ELECTRICAL CHARACTERISTICS: V_{DD} = +5V

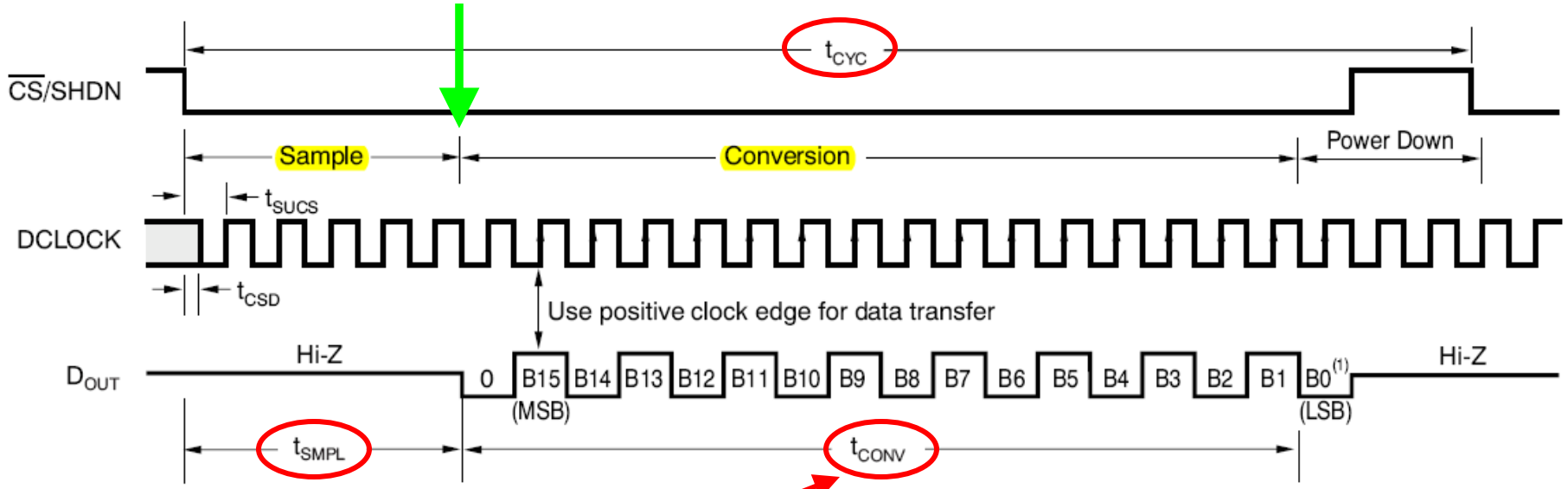
At –40°C to +85°C, V_{REF} = +5V, –IN = GND, f_{SAMPLE} = 250kHz, and f_{DCLOCK} = 24 × f_{SAMPLE}, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS8326I MIN	ADS8326I TYP	ADS8326I MAX	ADS8326IB MIN	ADS8326IB TYP	ADS8326IB MAX	UNIT
SAMPLING DYNAMICS									
Conversion time (16 DCLOCKs)	t_{CONV}	24kHz ≤ f_{DCLOCK} ≤ 6MHz	2.667		666.7	2.667		666.7	µs
Acquisition time (4.5 DCLOCKs)	t_{AQ}	f_{DCLOCK} = 6MHz	0.75			0.75			µs
Throughput rate (22 DCLOCKs)					250			250	kSPS
Clock frequency	f_{DCLOCK}		0.024		6	0.024		6	MHz



Sample and Conversion Timing

TIMING INFORMATION

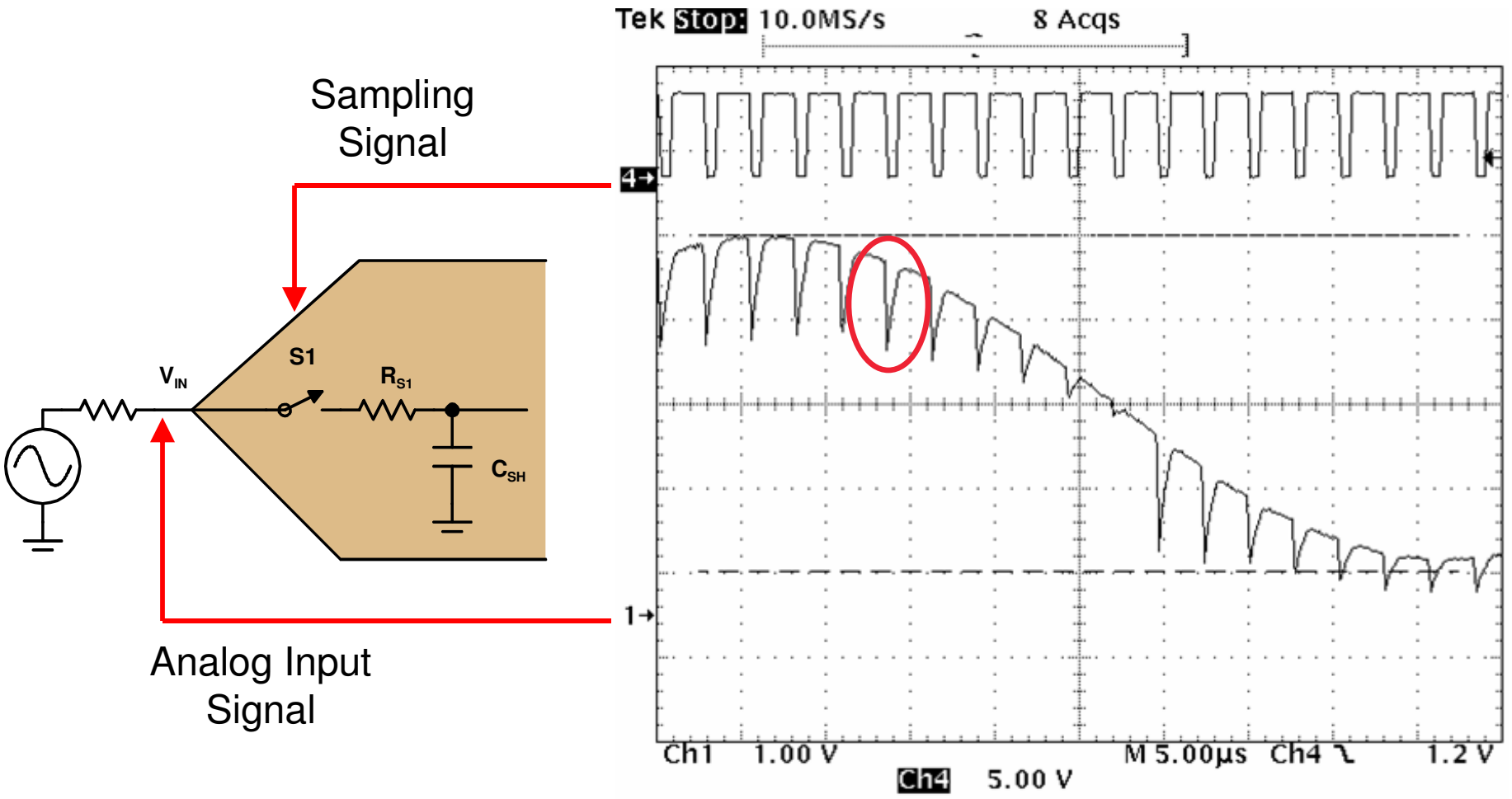


NOTE: (1) A minimum of 22 clock cycles are required for 16-bit conversion; 24 clock cycles are shown.

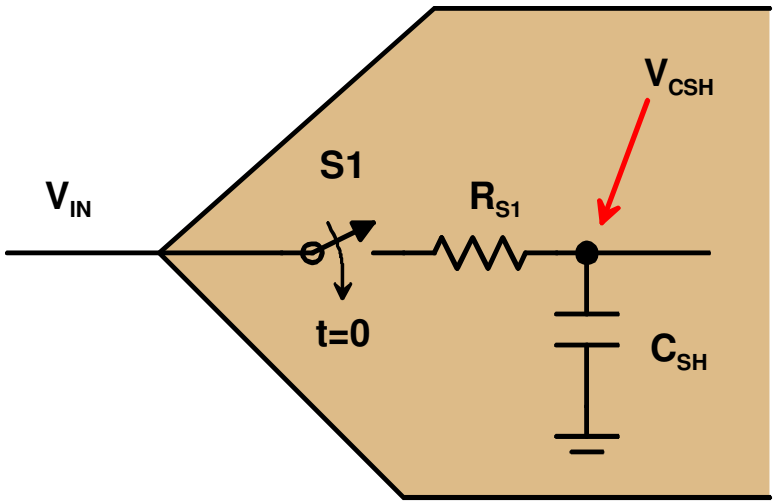
Table 1. Timing Characteristics

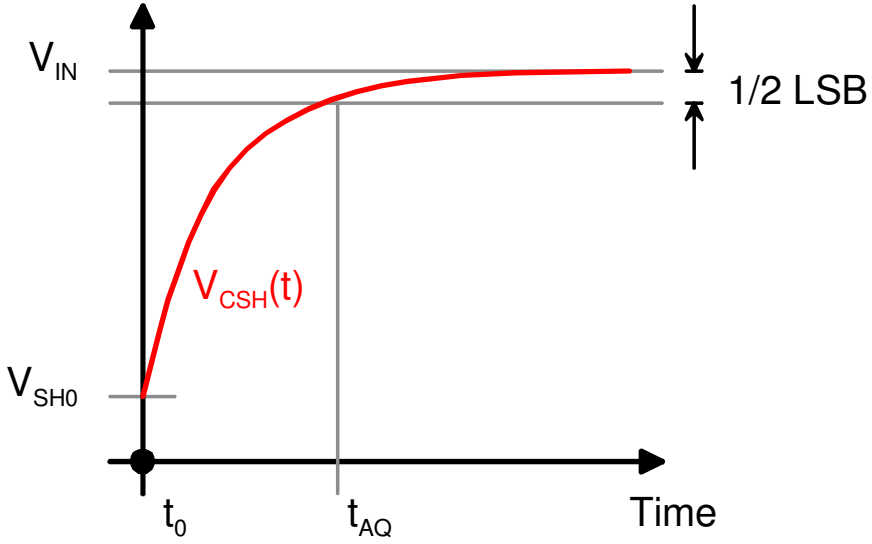
SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{SMPL}	Analog input sample time	4.5		5.0	DCLOCKs
t_{CONV}	Conversion time		16		DCLOCKs
t_{CYC}	Complete cycle time	22			DCLOCKs

Voltage Ripple on The Input of ADC



Voltage Across Sampling Capacitor





$$V_{CSH}(t) = V_{CSH}(t_0) + [V_{IN} - V_{CSH}(t_0)] \times (1 - e^{-\frac{t}{\tau}})$$

$$\tau = R_{S1} \times C_{SH}$$

Settling Time as a Function of Time Constant

$$V_{IN} - V_{CSH}(t_{AQ}) \leq \tfrac{1}{2} LSB$$

$V_{CSH}(t_{AQ})$ is voltage across the C_{SH}, at the end of the sampling period

t_{AQ} is acquisition time, the time from the beginning of the sampling period (t_0) to the end of the sampling period

$$\frac{1}{2} LSB = \frac{FSR}{2^{N+1}}$$

(LSB = Least Significant Bit, FSR is the full-scale range of the N-Bit converter)

$$t_{AQ} \geq k_1 \times \tau$$

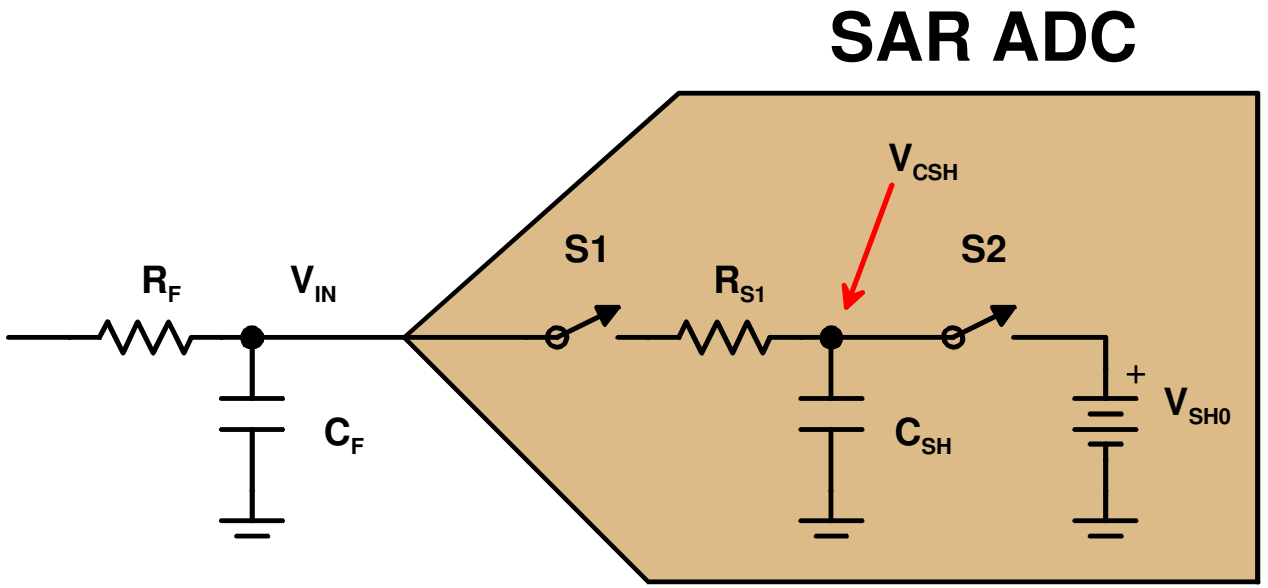
$$k_1 = (N+1) \times \ln(2)$$

Time-Constant-Multiplier (k_1) for SAR ADC

ADC Resolution	k1 time-constant-multiplie 1/2 LSB accuracy, $1/2^{N+1}$
8	6.2
10	7.6
12	9.0
14	10.4
16	11.8
18	13.2
20	14.6

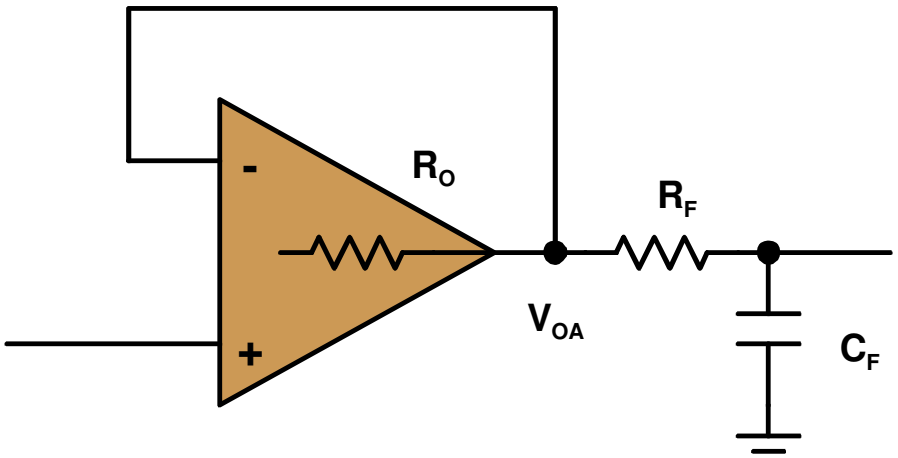
*note – using worst case values: V_{IN} = full-scale voltage or 2^N, V_{SH0} = 0V

SAR ADC With Input RC Filter

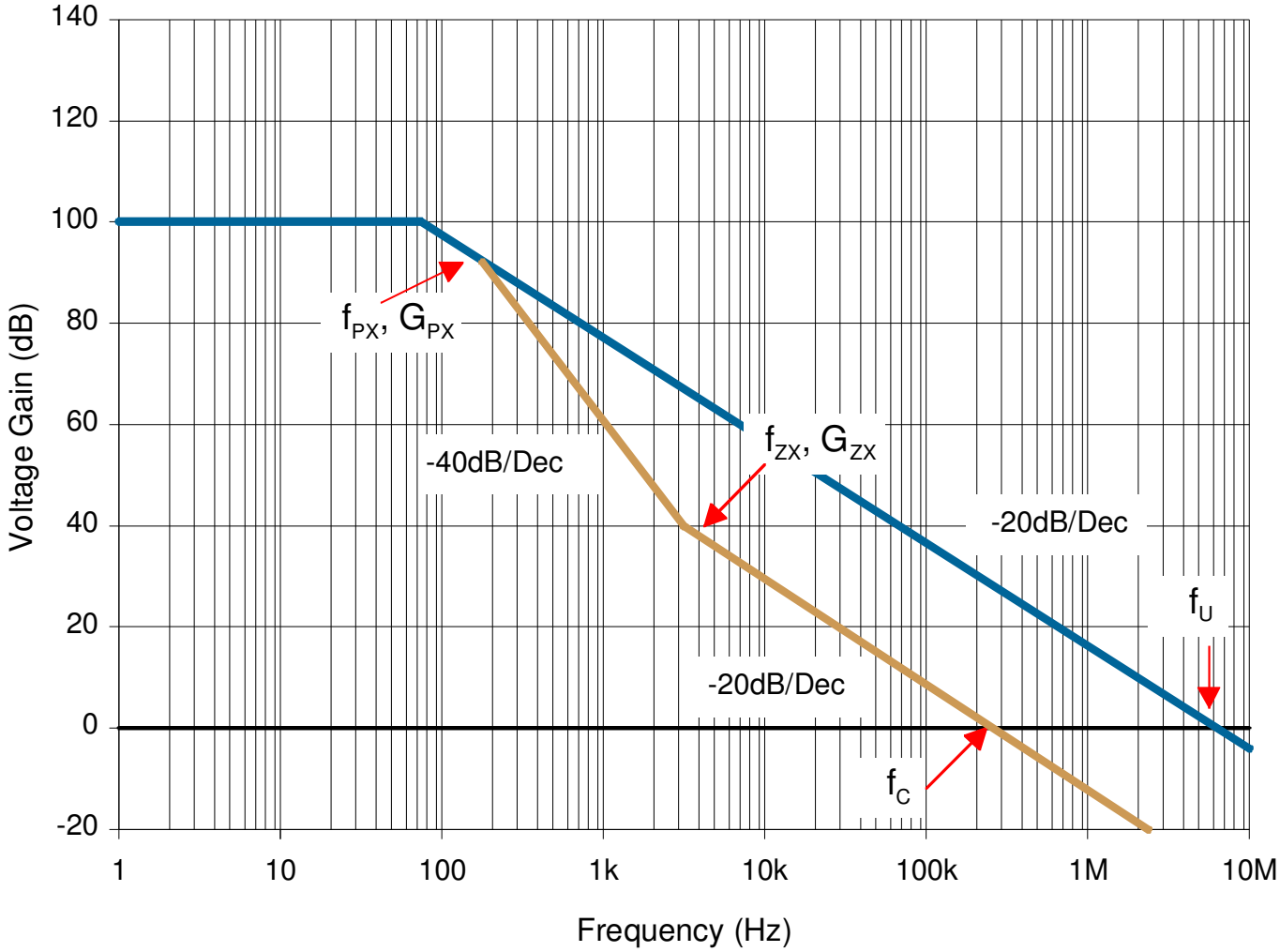


$$R_F \times C_F \leq \frac{t_{AQ}}{(N+1)\cdot \ln(2)}$$

Op Amp Driving RC Filter



Modified Open-Loop Voltage Gain



Added Pole and Zero

Frequency of added pole

$$f_{PX} = \frac{1}{2\pi \cdot (R_O + R_F) \cdot C_F}$$

Frequency of added zero

$$f_{ZX} = \frac{1}{2\pi \cdot R_F \cdot C_F}$$

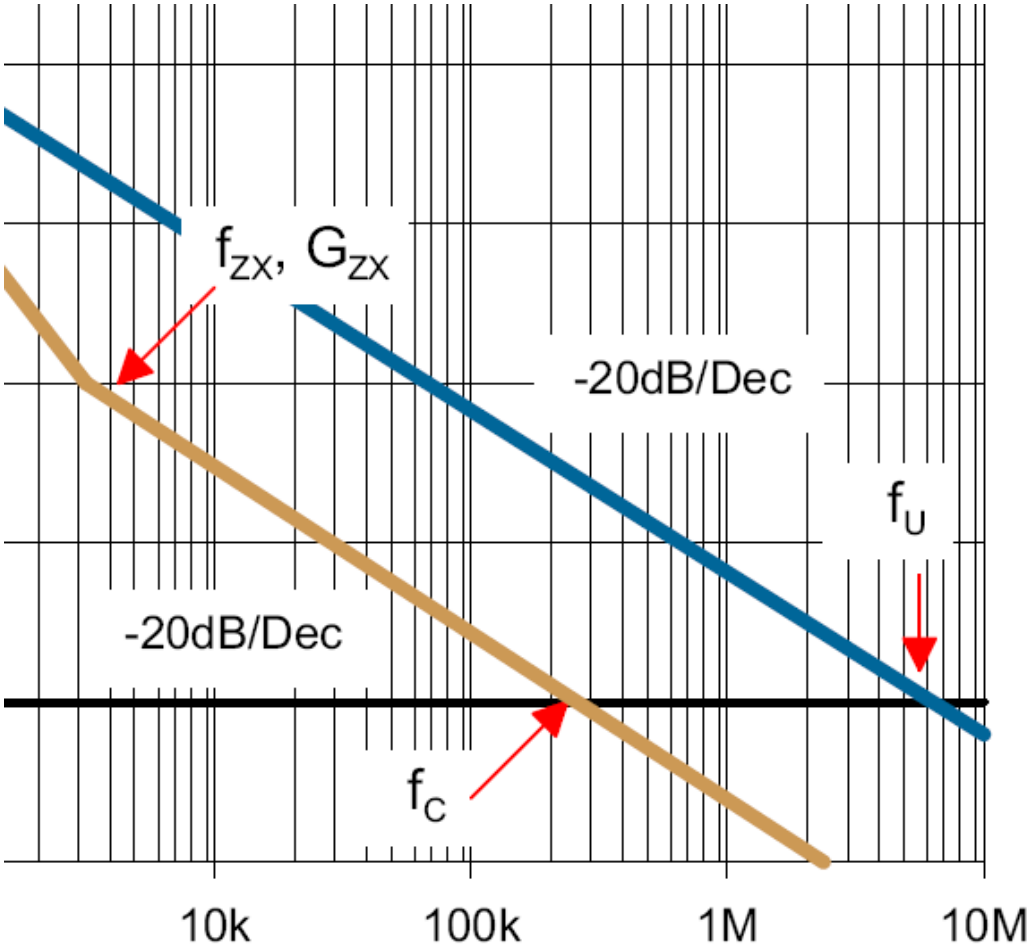
Gain of added pole

$$G_{PX} = -20 \cdot \log\left[\frac{f_{PX}}{f_U}\right]$$

Gain of added zero

$$G_{ZX} = G_{PX} - 40 \cdot \log\left[\frac{f_{ZX}}{f_{PX}}\right]$$

Good Design Guideline



$$f_C \le \tfrac{1}{2} f_U$$

$$f_{ZX} \le \tfrac{1}{2} f_C$$

or

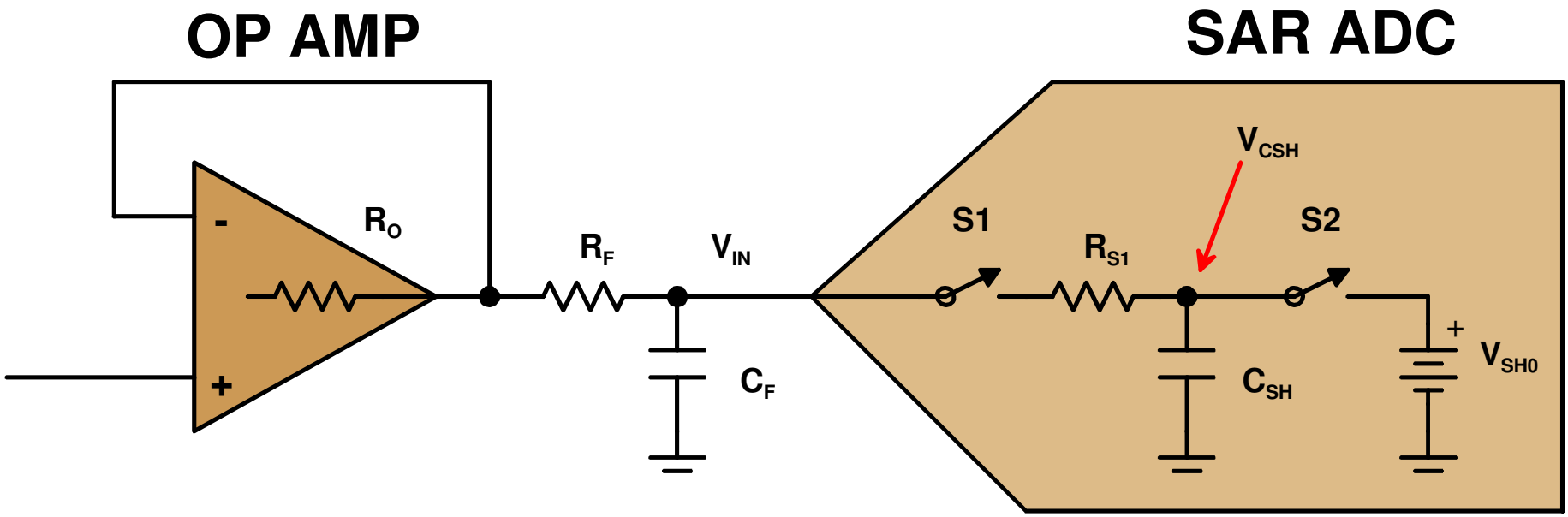
$$f_{ZX} \le \tfrac{1}{4} f_U$$

$$G_{ZX} \ge +6dB$$

$$f_{PX} > \tfrac{1}{10} f_{ZX}$$

$$R_F \ge \frac{R_O}{9}$$

Final Circuit



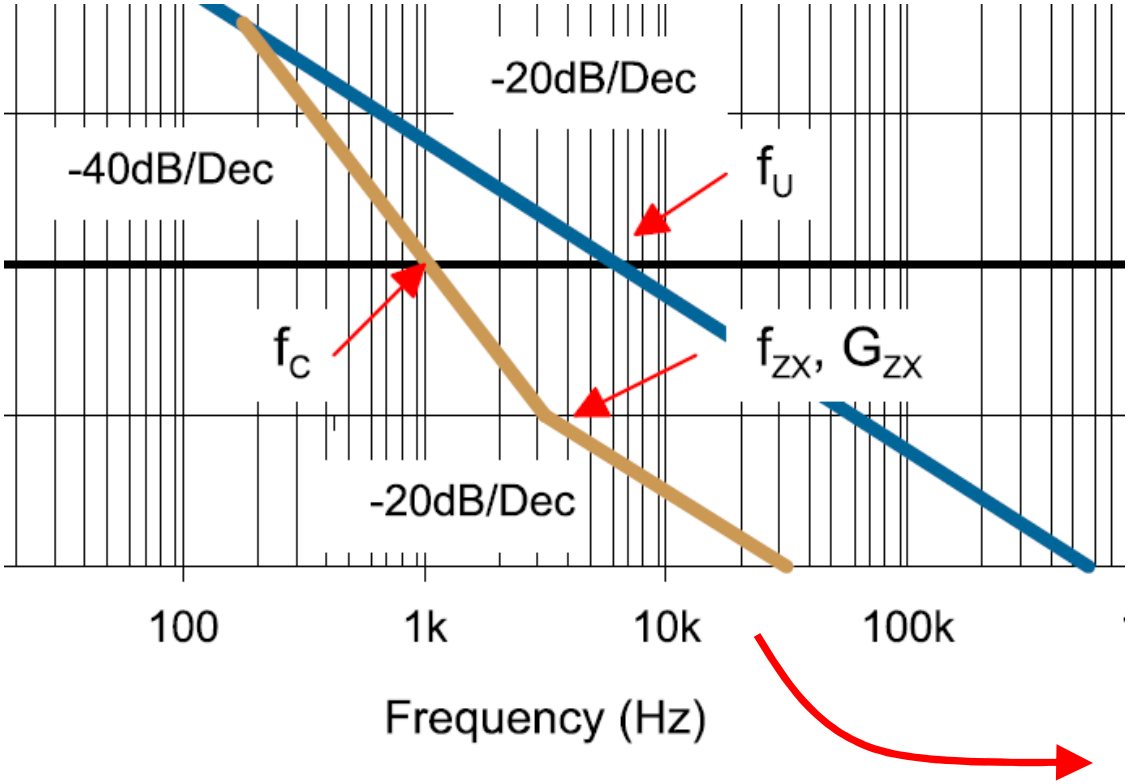
Minimum Acquisition Time and Op Amp's GBW

- Calculate time-constant multiplier $k = (N+1) \cdot \ln(2)$
- Determine minimum time-constant $\tau \leq \frac{t_{AQ}}{k}$
- Calculate frequency of added zero $f_{ZX} = \frac{1}{2\pi \cdot \tau}$
- Find Unity Gain Bandwidth $GBW = 4 \cdot f_{ZX}$

Minimum Acquisition Time for Different Op Amps

		GBW (MHz)	f_Z (MHz)	τ (ns)	12 Bit t_{AQ} (ns)	16 Bit t_{AQ} (ns)
INA155	Medium Speed, Precision INA	0.55	0.14	1,157	5,672	8,881
INA128	High Precision, 120dB CMRR	1.3	0.33	490	2,400	3,757
INA331	High Bandwidth, Single Supply	5.0	1.25	127	624	977
OPA340	CMOS, 0.0007% THD+N	5.5	1.38	116	567	888
OPA363	1.8V, High CMRR, SHDN	7.0	1.75	91	446	698
OPA2613	Dual VFB, Low Noise	12.5	3.13	51	250	391
OPA627	Ultra-Low THD+N, Wide BW	16.0	4.00	40	195	305
OPA381	Precision High-Speed Amp	18.0	4.50	35	173	271
OPA727	CMOS, e-trim™, Low Noise	20.0	5.00	32	156	244
OPA228	Precision, Low Noise, G ≥ 5	33.0	8.25	19	95	148
OPA350	Precision ADC Driver	38.0	9.50	17	82	129
OPAy365	High-Speed, Zero-Crossover	50.0	12.50	13	62	98
OPA2889	Dual, Low Power, VFB	75.0	18.75	8	42	65
OPA211	36V, Bipolar Precision	80.0	20.00	8	39	61
THS4281	Very Low Power RRIO	80.0	20.00	8	39	61
OPA358	CMOS, 3V Operation, SC70	80.0	20.00	8	39	61

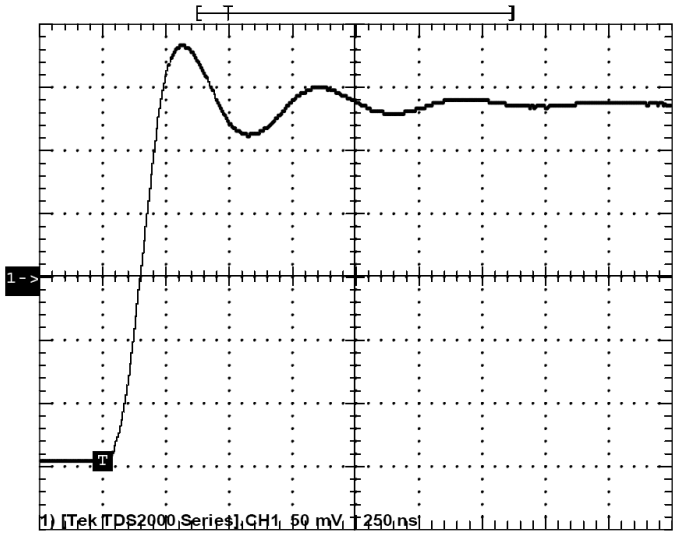
Not Good Design Guideline



$$f_C \le f_{ZX}$$

$$or$$

$$G_{ZX} \le 0dB$$



Stability Problem

After selecting ADC and OpAmp

- Determine CF $20 \cdot C_{SH} \le C_F \le 60 \cdot C_{SH}$
- Calculate R_F $R_F = \frac{1}{2\pi \cdot C_F \cdot f_{ZX}}$
- Verify value R_F $R_F \ge \frac{R_O}{9}$
- Calculate frequency of added pole $f_{PX} = \frac{1}{2\pi \cdot (R_F + R_O) \cdot C_F}$
- Keep added pole and zero less then decade a part $f_{PX} \ge \frac{1}{10} f_{ZX}$

Design by Example

For ADS8326 we have t_{AQ}=750ns, C_{SH}=48pF and N=16.

1

$$k = (N+1)\cdot\ln(2) = (16+1)\cdot\ln(2) = 11.78$$

$$\tau \le \frac{t_{AQ}}{k} = \frac{750ns}{11.78} = 63.65ns$$

$$f_{ZX} = \frac{1}{2\pi\cdot\tau} = \frac{1}{2\pi\cdot 63.65ns} = 2.5MHz$$

2

$$GBW \ge 4\cdot f_{ZX} = 4\cdot 2.5MHz = 10MHz$$

3

$$20\cdot C_{SH} \le C_F \le 60\cdot C_{SH} \Rightarrow 20\cdot 48\,pF \le C_F \le 60\cdot 48\,pF \Rightarrow$$
$$960\,pF \le C_F \le 2.9nF \Rightarrow C_F = 1.2nF$$

4

$$R_F = \frac{1}{2\pi\cdot C_F\cdot f_{ZX}} = \frac{1}{2\pi\cdot 1.2nF\cdot 2.5MHz} = 53\Omega$$

References

1) Green, Tim, “Operational Amplifier Stability, Part 6 of 15: Capacitance-Load Stability: RISO, High Gain & CF, Noise Gain,” Analog Zone, 2005.
2) Miro Oljaca, and Baker Bonnie, “Start with the right op amp when driving SAR ADCs,” EDN, October 16, 2008,
3) Downs, Rick, and Miro Oljaca, “Designing SAR ADC Drive Circuitry, Part I: A Detailed Look at SAR ADC Operation,” Analog Zone, 2005.
4) Downs, Rick, and Miro Oljaca, “Designing SAR ADC Drive Circuitry, Part II: Input Behavior of SAR ADCs,” Analog Zone, 2005.
5) Downs, Rick, and Miro Oljaca, “Designing SAR ADC Drive Circuitry, Part III: Designing The Optimal Input Drive Circuit For SAR ADCs,” Analog Zone, 2007.
6) Baker, Bonnie, and Miro Oljaca, “External components improve SAR-ADC accuracy,” EDN, June 7, 2007,
7) Miroslav Oljaca, “Understand the Limits of Your ADC Input Circuit Before Starting Conversions,” Analog Zone, 2004.