TSW308x Evaluation Module

The TSW308x evaluation module (EVM) provides a basic platform to evaluate the DAC348x in a complete RF transmit signal chain. Along with the DAC348x, the EVM includes a LMK04806B clock jitter cleaner and generator source, which provides the clocks required for the DAC and the external pattern generator. The EVM also includes an onboard TRF3705 I/Q modulator, which provides IF-to-RF upconversion for basic transmitter evaluation. This EVM is ideally suited for mating with the TSW3100 pattern generation board for evaluating WCDMA, LTE, or other high-performance modulation schemes.

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1 Introduction

1.1 Overview

The TSW308x evaluation module (EVM) is a family of circuit boards that allows designers to evaluate the performance of the Texas Instruments DAC348x family of digital-to-analog converters (DAC). The DAC348x family consists of DAC3482, DAC3484, and DAC34H84. The 16-bit, 1.25-GSPS, DAC348x has integrated 2x/4x/8x/16x interpolation filters, 32-bit NCO, on-chip PLL, and exceptional linearity at high IFs. The EVM provides a flexible environment to test the DAC348x under a variety of clock, data-input, and RF-output conditions. For ease of use as a complete RF transmit solution, the TSW308xEVM includes the LMK04806B low-noise, clock generator/jitter cleaner for clocking the DAC348x, as well as a TRF3705, a 300-MHz to 4-GHz quadrature modulator, for up-converting I/Q outputs from the DAC to RF.

EVM Part No.	**TSW3084**	**TSW3085**	**TSW30H84**
DAC Part No.	DAC3484	DAC3482	DAC34H84
Output Channels	4	2	4
Maximum DAC Rate	1.25 GSPS	1.25 GSPS	1.25 GSPS
Digital Interface	16-Bit LVDS Interface	16-Bit LVDS Interface	32-Bit LVDS Interface
Maximum Data Rate per Channel	312.5 MSPS	625 MSPS	625 MSPS

The EVM can be used along with TSW3100 to perform a wide range of test procedures. The TSW3100 generates the test patterns that are fed to the DAC348x through a 1.25-GSPS LVDS port. The LMK04806B also is used to synchronize the TSW3100 board to the TSW308xEVM. The RF signal path includes an amplifier and programmable attenuator.

1.2 EVM Block Diagram

Figure 1 shows the TSW308xEVM block diagram.

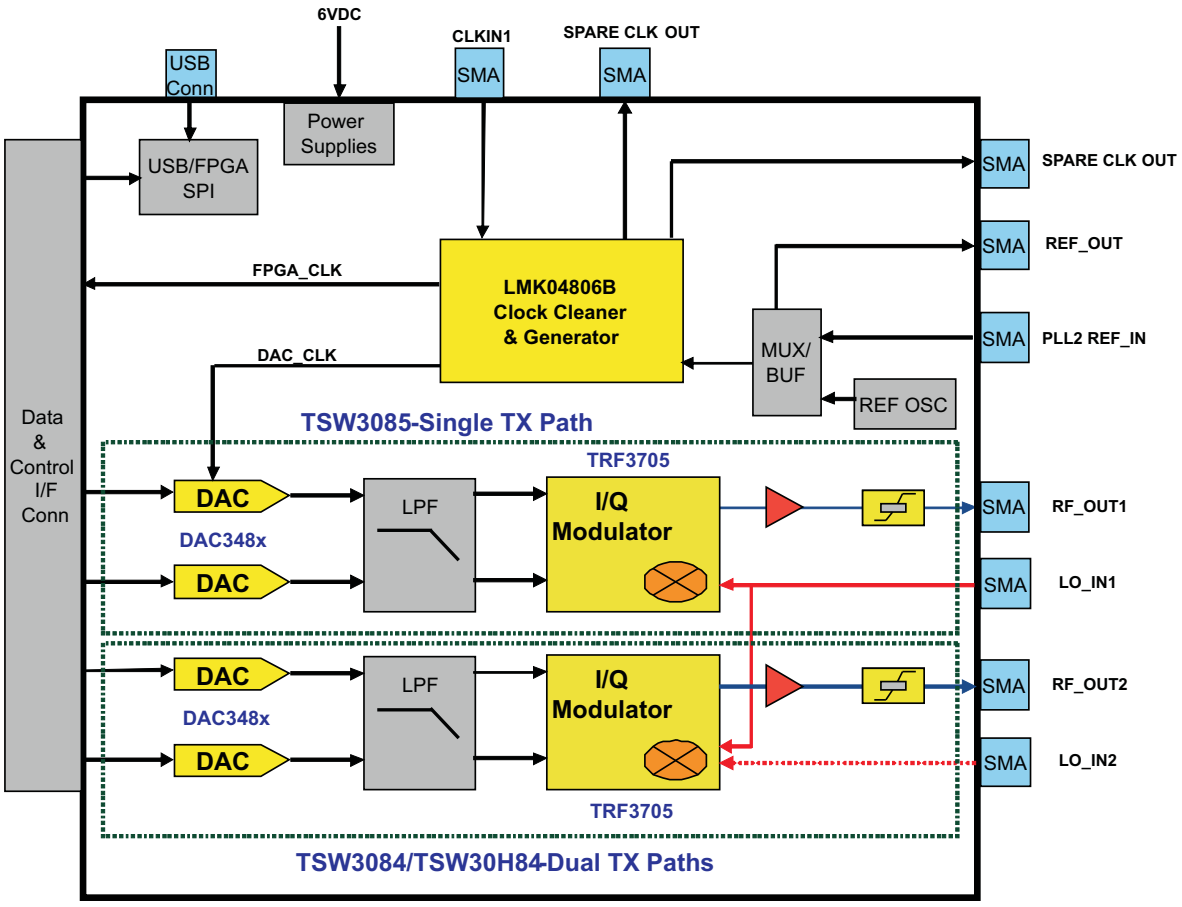


Figure 1. TSW30H84EVM Block Diagram

2 Software Control

2.1 Installation Instructions

Perform the following steps to install the software.

1. Open the folder named TSW308x_Installer_vxpx (xpx represents the latest version).
2. Run Setup.exe.
3. Follow the onscreen instructions.
4. Once installed, navigate to C:\Program Files\Texas Instruments\TSW308x. Start the GUI by clicking on the file named TSW308x.exe.
5. When plugging in the USB cable for the first time, you are prompted to install the USB drivers.
   (a) When a pop-up screen opens, select *Continue Downloading*.
   (b) Follow the onscreen instructions to install the USB drivers.
   (c) If needed, the drivers can be accessed directly in the install directory.

2.2 Software Operation

The software allows programming control of the DAC, the LMK, and the attenuator devices. The front panel provides a tab for full programming of each device. The GUI tabs provide a more convenient and simplified interface to the most-used registers of each device.

Each device has its own custom control interface. At the top level of the GUI are five control tabs. The first four are used to configure the DAC348x and the last for the LMK04806B. The attenuator control window on the right side of the GUI is used to program the attenuator.

2.2.1 Input Tab Control Options

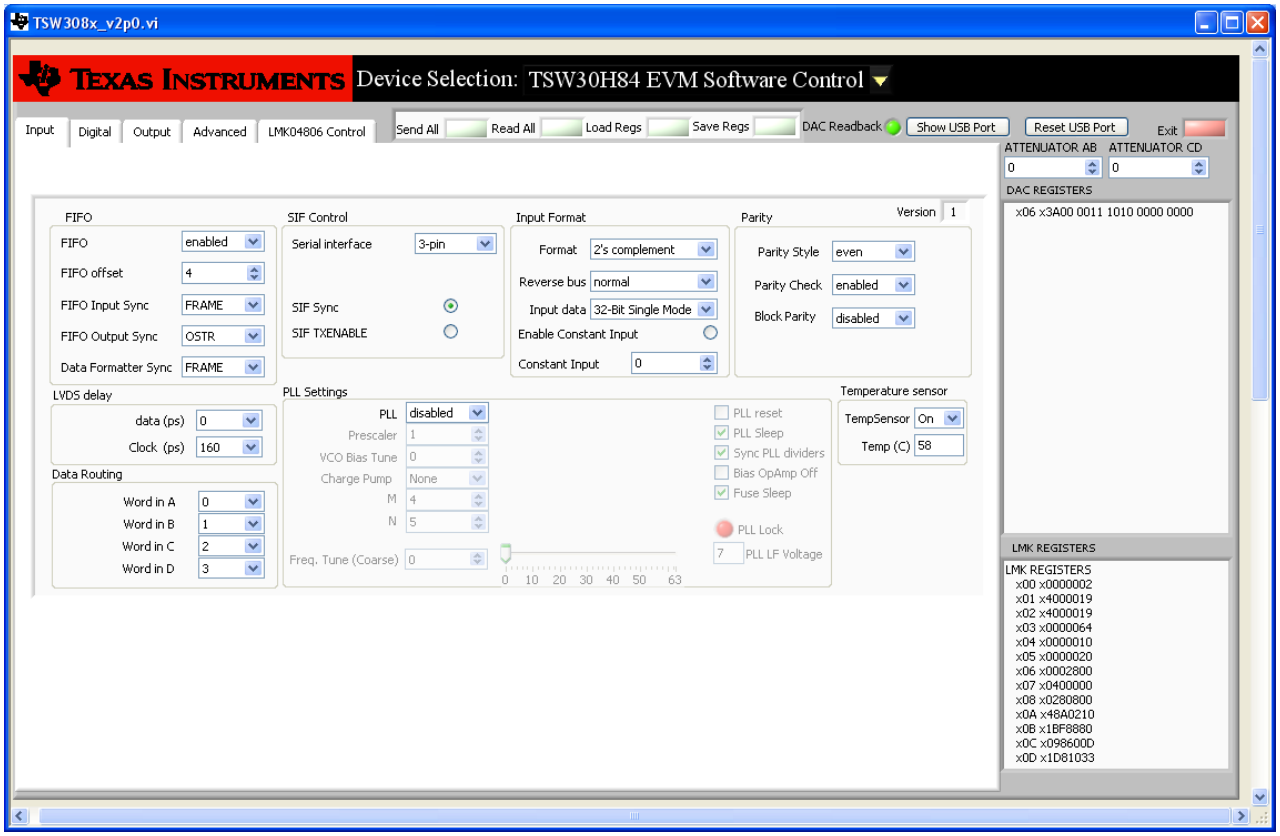


Figure 2. Input Tab Control Options – DAC348x

- FIFO: allows the configuration of the FIFO and FIFO synchronization (sync) sources.
- LVDS delay: provides internal delay of either the LVDS DATA or LVDS DATACLK to help meet the input setup/hold time.
- Data Routing: provides flexible routing of the A, B, C, and D sample input data to the appropriate digital path. **Note:** the DAC3482 does not support this mode.
- SIF Control: provides control of the Serial Interface (3-wire or 4-wire) and Serial Interface Sync (*SIF Sync*).
- Input Format: provides control of the input data format (i.e., 2's complement or offset binary).
- Parity: provides configuration of the parity input.
- PLL Settings: provides configuration of the on-chip PLL circuitry.
- Temperature Sensor: provides temperature monitoring of DAC348x die temperature.

2.2.1.1 FIFO Settings

The DAC348x has 8-samples deep FIFO to relax the timing requirement of a typical transmitter system. The FIFO has an input pointer and an output pointer, and both pointers can accept various input sources as reset triggers of input and output pointer position. One important application for input and output pointer control is the ability to synchronize multiple DACs in the system. For additional information, see the relevant DAC348x data sheet.

- FIFO Offset: The default position of FIFO output pointer after reset by the synchronization source. This setting can be used to change the latency of the DAC348x.
- Data Formatter Sync: Synchronization source for FIFO data formatter. Select between LVDS FRAME or LVDS SYNC signals.
- FIFO Input Sync: Synchronization source for FIFO input pointer. Select among the LVDS FRAME, LVDS SYNC, and/or SPI register SIF-SYNC to reset the FIFO input pointer position.
- FIFO Output Sync: Synchronization source for FIFO output pointer. Select among the LVDS FRAME, LVDS SYNC, SPI register SIF-SYNC, and/or OSTR signal to reset the FIFO output pointer position.
  - For single device application without the need for precise latency control, Single Sync Source Mode may be used. The FIFO output pointer position can be reset with LVDS FRAME, LVDS SYNC, and/or SPI register SIF-SYNC. See the Single Sync Source Mode in the relevant DAC348x data sheet for details.
  - For multiple device synchronization, select the OSTR signal as the FIFO output synchronization source. If the DAC is configured to accept external DAC Clock input, then the OSTR signal is the external LVPECL signal to the OSTRP/N pins. If the DAC is configured to accept the internal on-chip PLL clock, then the OSTR signal is the internally generated PFD frequency. See the Dual Sync Sources Mode in the relevant DAC348x data sheet for details.

2.2.1.2 LVDS Delay Settings

The TSW3100 pattern generator sends out LVDS DATA and DATACLK as edge-aligned signals. The following options can be implemented to meet the minimum setup and hold time of DAC348x data latching:

- Set the on-chip LVDS DATACLOCK delay. Typical setting of 160 ps or more helps meet the timing requirement for most of the TSW3100 + TSW308xEVM setup. This LVDS DATACLOCK delay does not account for additional printed-circuit board (PCB) trace-to-trace delay variation, only the internal DATACLK delay.
- Modify the external LVDS DATACLK PCB trace delay. Additional trace length can be added to the DATACLK P&N PCB trace length.
  - For the TSW3085EVM: At the bottom side, set SJP4, SJP5, SJP6, and SJP7 to the 1-2 position for approximately 400 ps of trace delay.
  - For the TSW3084EVM and TSW30H84EVM: At the top side, set SJP9, SJP10, SJP11, and SJP12 to the 2-3 position for approximately 280 ps of trace delay.

2.2.1.3 PLL Settings

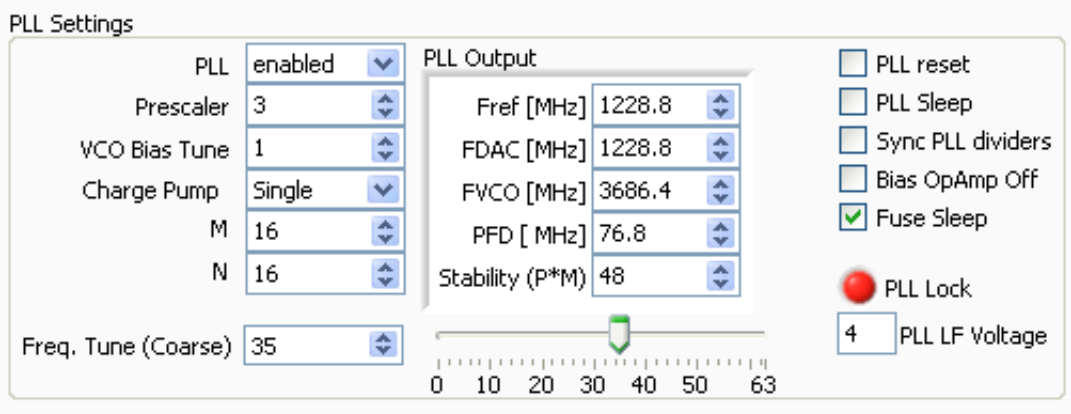


Figure 3. PLL Configuration

Perform the following steps to configure the PLL.

1. Enable PLL.
2. Uncheck *PLL reset* and *PLL sleep*.
3. Set *M* and *N* ratio such that F_{DAC} = (M)/(N) × Fref.
4. Set the *prescaler* such that the F_{DAC} × prescaler is within 3.3 GHz and 4 GHz.
5. Set *VCO Bias Tune* to 1.
6. *Charge Pump* setting
   (a) If stability (P × M) is less than 120, then set to *Single*.
   (b) If stability (P × M) is greater than 120, then set to *Double* or install external loop filter.
7. Adjust the *Freq. Tune (Coarse)* accordingly.

2.2.2 Digital Tab Control Options

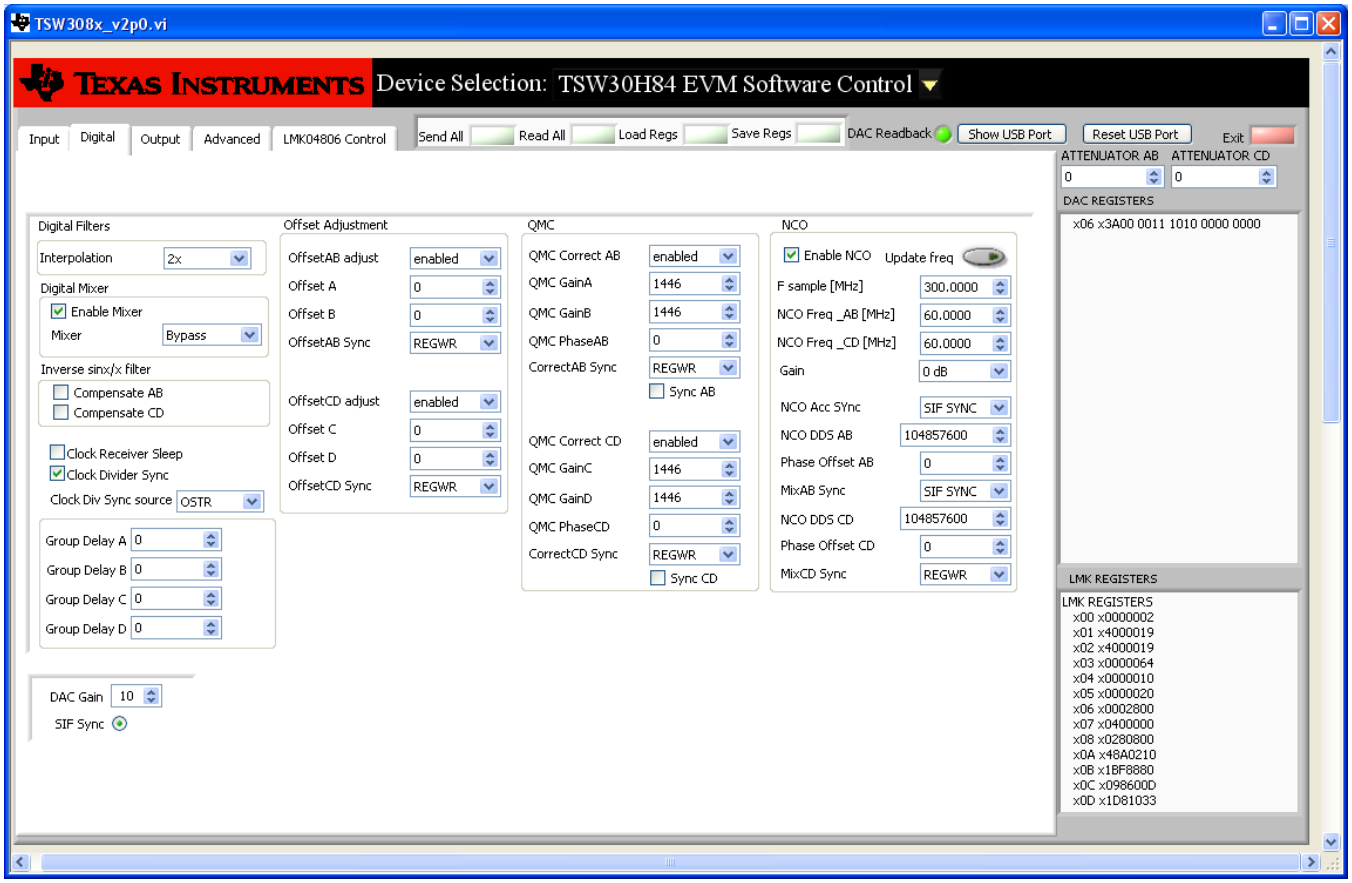


Figure 4. Digital Tab Control Options – DAC348x

- Interpolation: allows control of the data rate versus DAC sampling rate ratio (i.e., data rate × interpolation = DAC sampling rate).
- Digital Mixer: allows control of the coarse mixer function.
  Note: If fine mixer (NCO) is used, the Enable Mixer button must be checked, and the coarse mixer must be bypassed. See the following NCO bullet for detail.
- Inverse sinx/x filter: allows compensation of the sinx/x attenuation of the DAC output.
  Note: If inverse sinx/x filter is used, the input data digital full-scale must be backed off accordingly to avoid digital saturation.
- Clock Receiver Sleep: allows the DAC clock receiver to be in sleep mode. The DAC has minimum power consumption in this mode.
- Clock Divider Sync: allows the synchronizing of the internal divided-down clocks using either Frame, Sync, or OSTR signal. Enables the divider sync as part of the initialization procedure or resynchronization procedure.
- Group Delay: allows adjustment of group delay for each I/Q channel. This is useful for wideband sideband suppression.
- Offset Adjustment: allows adjustment of dc offset to minimize the LO feedthrough of the modulator output. This section requires synchronization for proper operation. The synchronization options follow:
  - *REGWR*: auto-sync from SIF register write.
  - *OSTR*: sync from the external LVPECL OSTR signal. Clock divider sync must be enabled with OSTR set as sync source.
  - *SYNC*: sync from the external LVDS SYNC signal.

  - *SIF SYNC:* **sync from SIF Sync. Uncheck and check the SIF Sync button for sync event.**
- QMC Adjustment: allows adjustment of the gain and phase of the I/Q channel to minimize sideband power of the modulator output.
  - *REGWR*: auto-sync from SIF register write.
  - *OSTR*: sync from the external LVPECL OSTR signal. Clock Divider Sync must be enabled with OSTR set as sync source.
  - *SYNC*: sync from the external LVDS SYNC signal.
  - *SIF SYNC:* **sync from SIF Sync. Uncheck and check the SIF Sync button for sync event.**
- NCO: allows fine mixing of the I/Q signal. The procedure to adjust the NCO mixing frequency follows.
  1. Enter the DAC sampling frequency in Fsample.
  2. Enter the desired mixing frequency in both NCO freq_AB and NCO freq_CD.
  3. Press Update freq.
  4. Synchronize the NCO block from the following options.
     - *REGWR*: auto-sync from SIF register write. Writing to either *Phase OffsetAB* or *Phase OffsetCD* can create a sync event.
     - *OSTR*: sync from the external LVPECL OSTR signal. Clock Divider Sync must be enabled with OSTR set as sync source. See the data sheet for OSTR period requirement.
     - *SYNC*: sync from the external SYNC signal.
     - *SIF SYNC:* **sync from SIF Sync. Uncheck and check the SIF Sync button for sync event.**

2.2.3 Output Tab Control Options

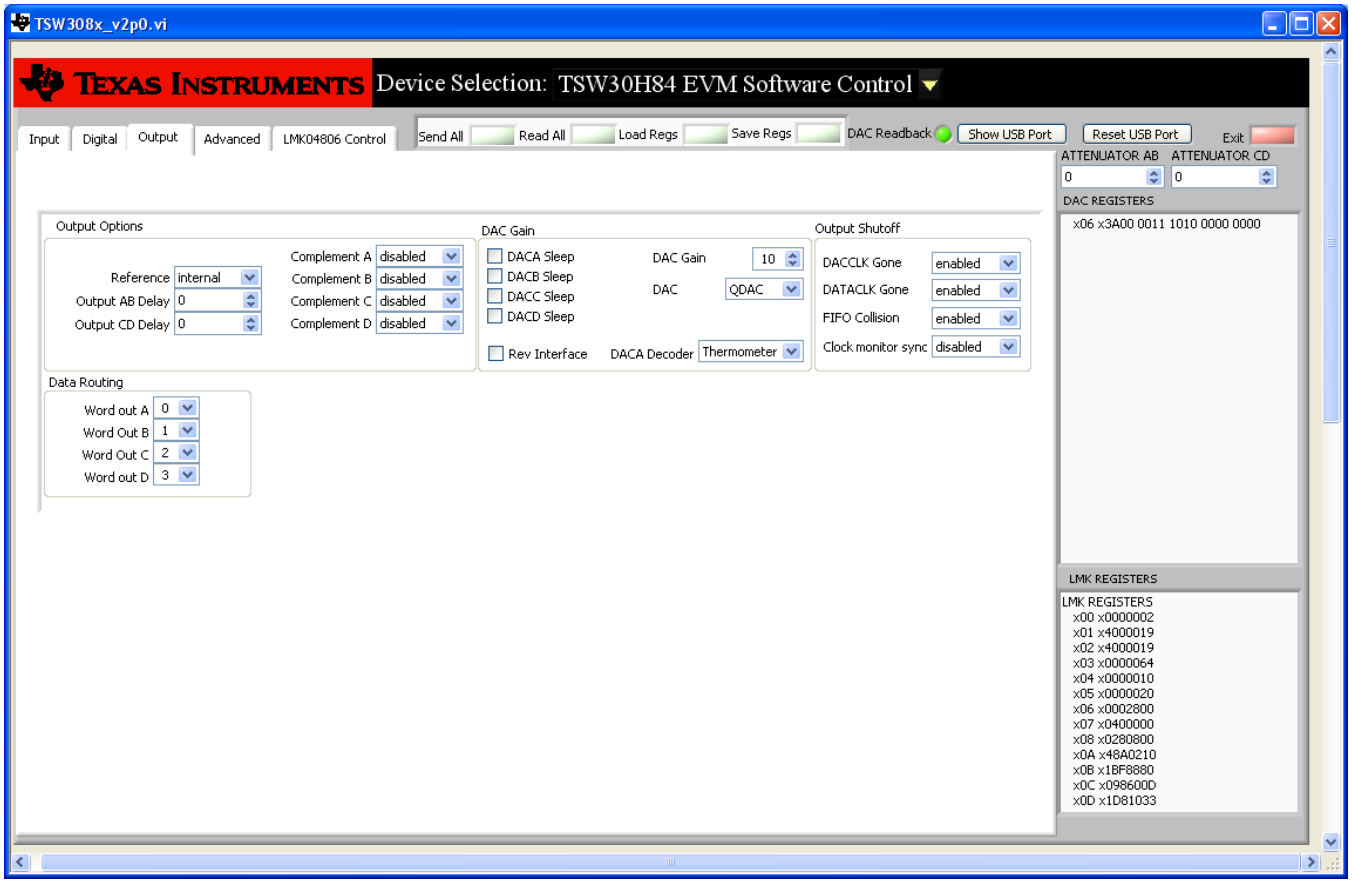


Figure 5. Output Tab Control Options – DAC348x

- Output Options: allows the configuration of reference, output polarity, and output delay
- Data Routing: provides flexible routing of the A, B, C, and D digital path to the desired output channels. **Note:** The DAC3482 does not support this mode.
- DAC Gain: configures the full-scale DAC current and DAC3484/DAC3482 mode. With Rbiasj resistor set at 1.28 kΩ:
  - DAC Gain = 15 for 30-mA, full-scale current.
  - DAC Gain = 10 for 20-mA, full-scale current (default).
- DAC: sets DAC mode
  - DAC3484 = QDAC
  - DAC3482 = DDAC
- Output Shutoff On: allows outputs to shut off when DACCLK GONE, DATACLK GONE, or FIFO COLLISION alarm event occurs.

2.2.4 LMK04806B

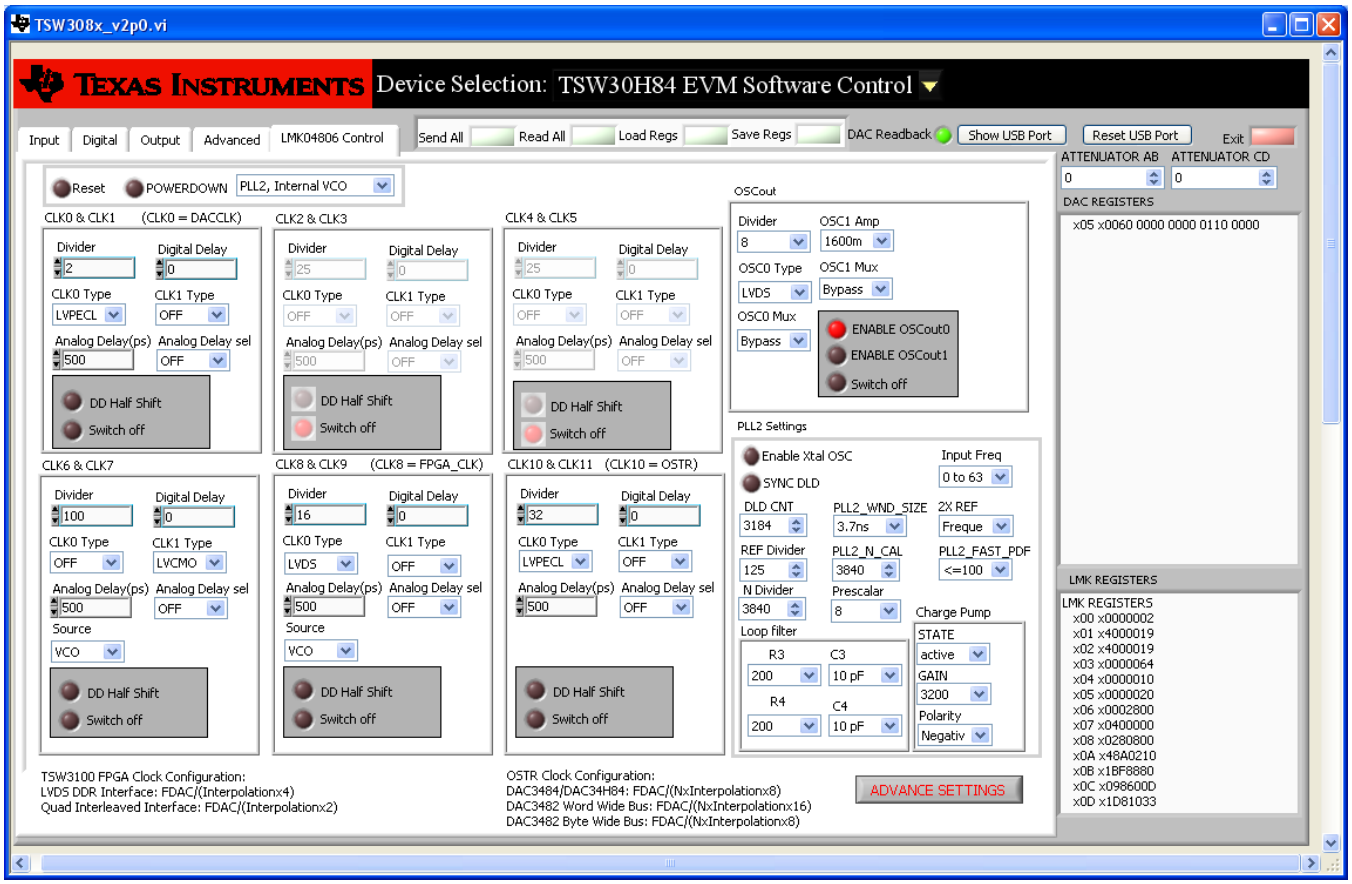


Figure 6. LMK04806B Tab Control Options

Clock control is determined by register values in the LMK04806B Control tab. See the LMK0480x family data sheet for detailed explanations of the register configurations.

The LMK04806B has 12 available output clocks. The following LMK04806 outputs are used by the TSW308xEVMs:

- CLK0: DAC348x DAC sampling clock. If the DAC348x is configured for internal PLL mode, this becomes the reference clock input for the PLL block.
- CLK8: TSW3100 FPGA input clock.

  - TSW3085 and TSW30H84 with LVDS Dual Interleaved Rate: the clock rate must be set to F_{DAC}/interpolation/4.
  - TSW3084 with LVDS Quad Interleaved Rate: the clock rate must be set to F_{DAC}/interpolation/2.
- CLK10: DAC348x FIFO OSTR Clock
  - The OSTR signal can be a slower periodic signal or a pulse depending on the application.
  - The OSTR clock rate must be at most F_{DAC}/interpolation/8. See the DAC348x data sheet for more detail.
  - The FIFO OSTR clock must be disabled when the DAC348x is using the on-chip PLL for DACCLK generation.
- CLK6: Spare output clock at SMA J5.
- CLK3: Spare output clock at SMA J2 and J3.

The CLOCK settings are divided into subcontrol sections. These sections allow the user to set the divide ratio, digital delay, type, analog delay, and ON/OFF control. Note that clock pairs share several settings.

The OSCout control section allows the user to configure the settings for the OSCIN input. The TSW308xEVM uses this input as the reference input for Single Loop mode of operation (default configuration). This mode uses PLL2 of the device. This reference can be provided by either the onboard 10-MHz oscillator (default) or from an external source brought in through SMA J11. For details, see Section 4.

The PLL2 Settings control section allows the user to configure the settings for the internal PLL2. The LMK0480x family contains four devices that cover internal VCO frequencies from 1840 MHz to 3072 MHz. The VCO range of the LMK048060B is 2370 MHz to 2600 MHz . The TSW308xEVM default test case uses settings to set the internal VCO to 2457.6 MHz and is locked to the 10-MHz input source on OSCIN.

The default Single Loop PLL settings provided by the example file provide a 1228.8-MHz clock on CLK0 for the DAC348x, the divided-down FPGA clock at CLK8 for the TSW3100 pattern generator input clock, and the divided-down OSTR clock for DAC348x's OSTR input. The CLK6 (J5) is configured as a divide-by-100 CMOS clock. This can be used as part of EVM functionality verification. For details, see Section 3.4.

After the default settings are loaded, the output clocks are synchronized with the onboard 10-MHz reference oscillator as indicated by LED (Lock) being illuminated.

Clicking on the Advance Settings tab at the bottom of the GUI opens a new window allowing the user to set other internal registers for different modes of operation as shown in Figure 7.

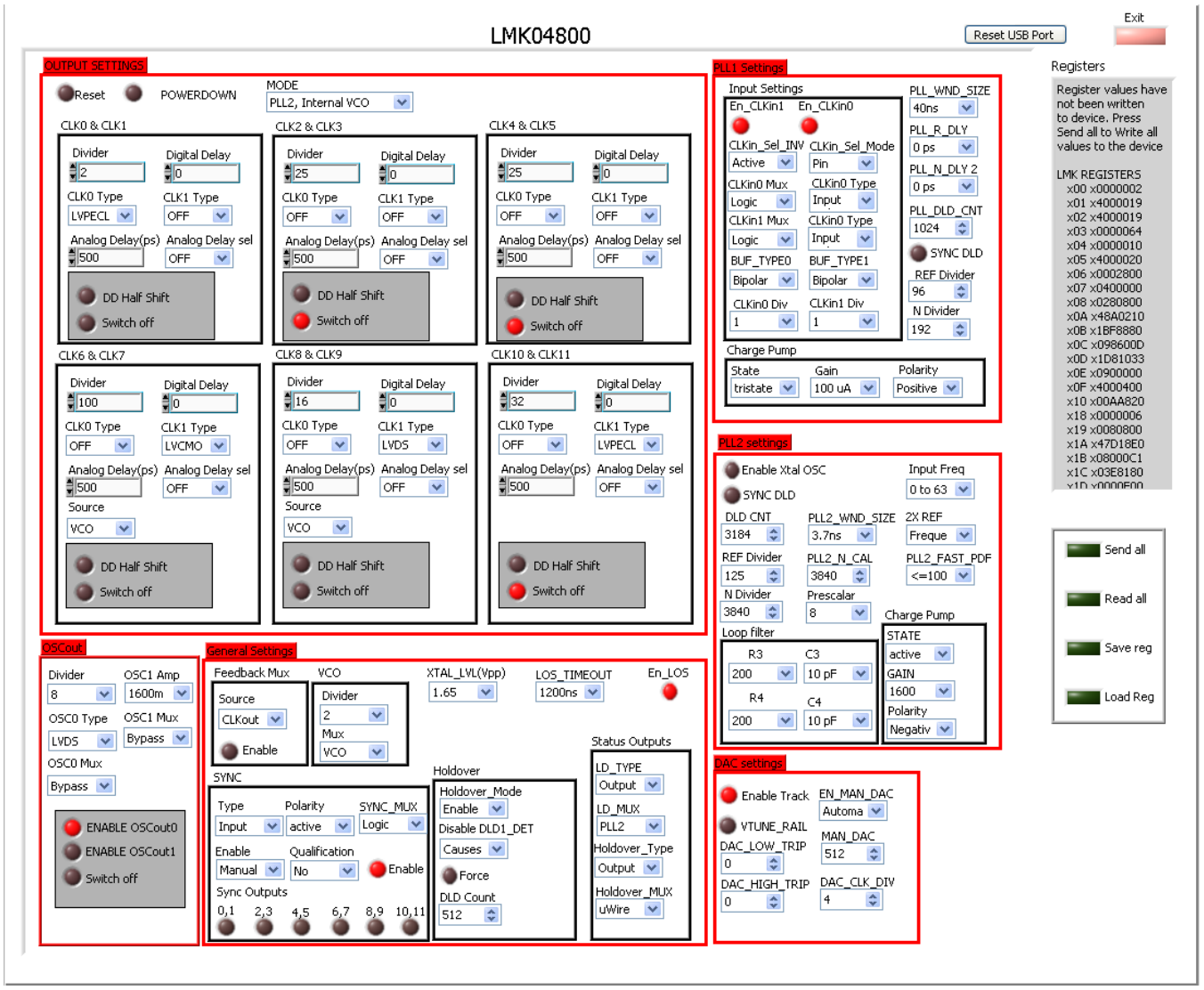


Figure 7. LMK04806B Advanced Settings Control Panel

2.2.5 Register Control

- Send All: sends the register configuration to all devices.
- Read All: reads register configuration from DAC348x and LMK04806B devices.
- Load Regs: loads a register file for all devices. A sample configuration file for a common frequency plan is located in the install directory.
  - Select *Load Regs* button.
  - Double-click on the *TSW308xEVM_Configuration_Files* folder.
  - Double-click on the desired register file.
  - Click on *Send All* to ensure all the values are loaded properly.
- Save Regs: saves the register configuration for all devices.

2.2.6 Attenuator Control

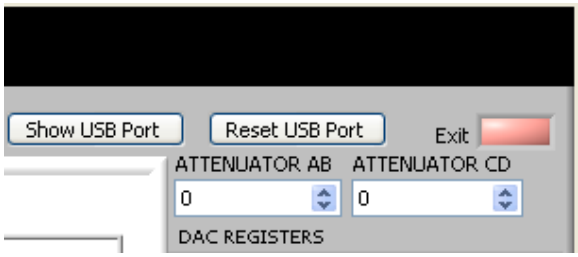


Figure 8. RF Attenuator Control

The RF path on the TSW308xEVM contains a 50-Ω, RF digitally controlled attenuator that operates from DC to 4 GHz. This highly versatile digital step attenuator (DSA) covers a 0-dB to 31.75-dB attenuation range in 0.25-dB steps. It maintains high attenuation accuracy over frequency and temperature and exhibits very low insertion loss (1.9 dB, typical) and low-power consumption. The user can enter a value from 0 (minimum attenuation) to 31.75 (maximum attenuation) in 0.25 increments inside the Attenuator window (Figure 8) or by clicking on the drop-up/-down arrows.

2.2.7 Miscellaneous Settings

- Reset USB: toggle this button if the USB port is not responding. This generates a new USB handle address.
  - Note: It is recommended that the board be reset after every power cycle, and the reset USB button on the GUI be clicked.
- Exit: stops the program

3 Basic Test Procedure

This section outlines the basic test procedure for testing the EVM.

3.1 TSW3100 Quick-Start Operation

See the TSW3100 user's guide (SLLU101) for more detailed explanations of the TSW3100 setup and operation. This document assumes that the TSW3100 software is installed and functioning properly. This information can be found at http://focus.ti.com/docs/toolsw/folders/print/tsw3100evm.html. The TSW30H84 needs TSW3100 operating software version 2.5 or higher with TSW3100 board Rev D (or higher).

The TSW308xEVM sends the FPGA reference clock to the FPGA of the TSW3100EVM in LVDS format. Therefore, a 100-Ω LVDS termination resistor is needed at the TSW3100 FPGA clock input. All the latest TSW3100EVMs from TI have the 100-Ω termination installed at the bottom side of the board on pins T31 and T32 of the FPGA. Contact TI Application Support if the 100-Ω termination is missing and assistance is needed for the 100-Ω installation.

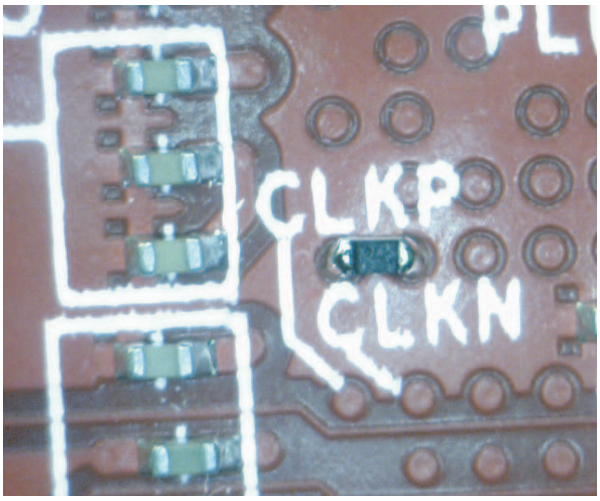
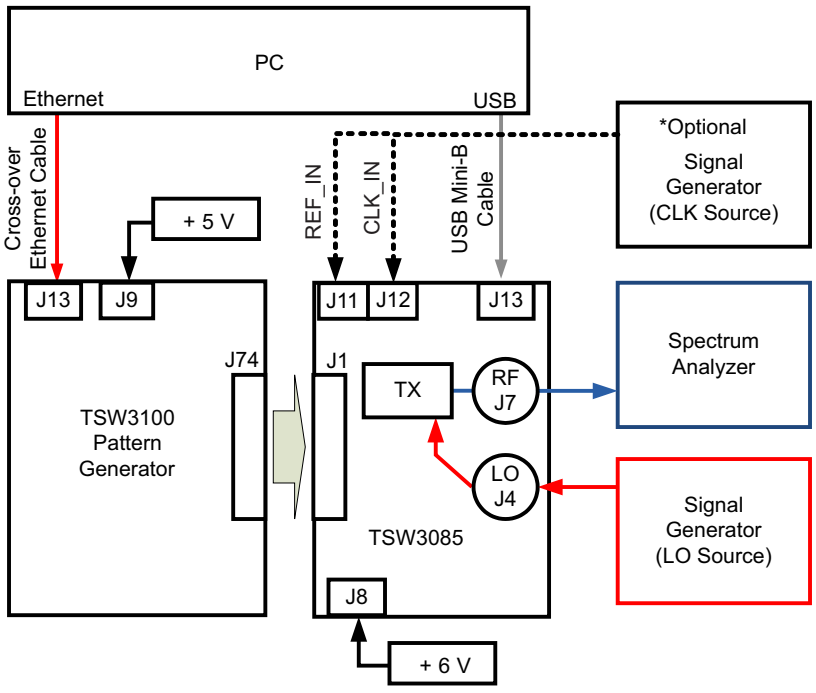


Figure 9. TSW3100 FPGA Clock 100-Ω LVDS Termination at Pins T31 and T32 of the FPGA

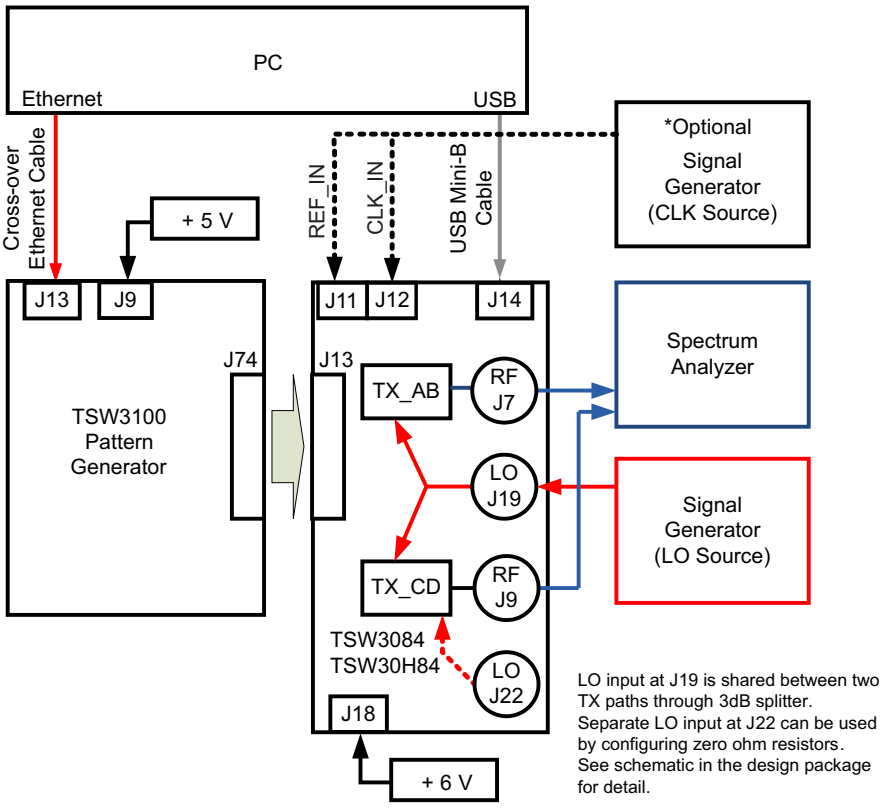
3.2 Test Block Diagram

The test setup for general testing of the TSW308xEVM with the TSW3100 pattern generation board is shown in Figure 10.



***REF_IN to J11 can be applied to LMK04806B in Single PLL Mode. CLK_IN to J12 must be applied to LMK04806B in Clock Distribution Mode or Dual PLL Mode.**

Figure 10. TSW3085 Test Setup Block Diagram



***REF_IN to J11 can be applied to LMK04806B in Single PLL Mode.**
CLK_IN to J12 must be applied to LMK04806B in Clock Distribution Mode or Dual PLL Mode.

Figure 11. TSW3084 and TSW30H84 Test Setup Block Diagram

3.3 Test Setup Connection

- TSW3100 Pattern Generator
  1. Connect 5-V power supply to J9, *5V_IN* jack of the TSW3100EVM.
  2. Connect the PC's Ethernet port to J13, *Ethernet* port of the TSW3100. The cable must be a standard crossover Cat5e Ethernet cable.
- EVM Connections

  – TSW3085EVM
  1. Connect J1 connector of TSW3085EVM to J74 connector of TSW3100EVM
  2. Connect 6 V to the J8, *Power In* jack of the TSW3085EVM
  3. Connect PC's USB port to J13 USB port of the TSW3085EVM. The cable must be a standard A-to-mini-B connector cable.
  4. Provide 15-dBm maximum, 300-MHz to 4-GHz LO source at J4. This provides the LO source to the TRF3705 modulator.
  5. Connect the RF output port J7 to a spectrum analyzer.
  6. If an external reference is to be used with LMK04806B in single PLL mode, provide a 3.3-Vpp maximum, 140-MHz maximum clock to SMA J11.
  7. If the LMK04806B is configured in clock distribution mode, provide a 2.4-Vpp maximum, 3.1-GHz maximum clock to SMA J12.

  – TSW3084/H84EVM
  1. Connect J13 connector of TSW3084/H84EVM to J74 connector of TSW3100EVM

2. Connect 6 V to the J18, Power In jack of the TSW3084/H84EVM.
3. Connect PC's USB port to J14 USB port of the TSW3084/H84EVM. The cable must be a standard A-to-mini-B connector cable.
4. Provide 18-dBm maximum, 300-MHz to 4-GHz LO source at J19. This provides the LO source to the TRF3705 modulator. By default, this LO source is shared between the two TX paths through a 3-dB splitter.
5. Connect the RF output port of J7 and J9 to the spectrum analyzer.
6. If an external reference is to be used with LMK04806B in single PLL mode, provide a 3.3-Vpp maximum, 140-MHz maximum clock to SMA J11.
7. If the LMK04806B is configured in clock distribution mode, provide a 2.4-Vpp maximum, 3.1-GHz maximum clock to SMA J12.

- EVM jumpers: ensure that the following jumpers are at their default setting.

– TSW3085EVM

1. JP2 = (1,2)
2. JP3 = (2,3)
3. JP4 = (1,2)
4. JP5 = (1,2)

– TSW3084/H84EVM

1. JP2 = (1,2)
2. JP3 = (2,3)
3. JP4 = (1,2)
4. JP12 = (2,3)
5. JP13 = (2,3)
6. JP14 = (2,3)
7. JP15 = (2,3)

3.4 TSW308x Example Setup Procedure

- Turn on power to both boards, and press the reset button SW1 on the TSW308xEVM.
- Press the *Reset USB Port* button in the GUI, and verify USB communication.

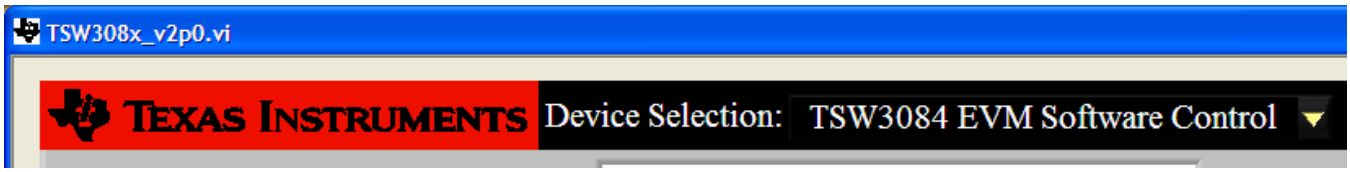


Figure 12. EVM Platform Selection

- Select the appropriate EVM platform on the software menu
- Click on *LOAD REGS*, browse to the installation folder, and load example files. The default installation folder is located at *C:\Program Files\Texas Instruments\TSW308x\TSW308xEVM_Configuration_Files*. To configure the LMK04806B in single PLL mode, select the file in the *LMK04806 PLL Mode 10MHz reference* folder for each EVM. To configure the LMK04806B in clock distribution mode, select the file in the *LMK04806 Clock Distribution Mode* folder for each EVM.
  - For the TSW3085, the file contains settings for 2x interpolation with the DAC3482 running at 1228.8 MSPS. The data rate for each DAC is at 614.4 MSPS. The NCO is enabled at 30 MHz.
  - For the TSW30H84, the file contains settings for 2x interpolation with the DAC34H84 running at 1228.8 MSPS. The data rate for each DAC is at 614.4 MSPS. The NCO is enabled at 30 MHz.
  - For the TSW3084, the file contains settings for 4x interpolation with the DAC3484 running at 1228.8 MSPS. The data rate for each DAC is at 307.2 MSPS. The NCO is enabled at 30 MHz.
  - Load this file and wait a couple of seconds for the settings to go into effect.

- Click on *Send All* to write all of the values to the devices. If the LMK04806B is programmed properly in single PLL mode, the Lock LED near the device will be illuminated. The updated register configuration for the LMK04806B now appears as shown in Figure 6.
- Note: J5 (CLK6) is configured as a divide-by-100 CMOS clock. This is used to verify EVM functionality.
- TSW3100 Single-Carrier WCDMA Output Example Setup
  - Start the TSW3100_CommsSignalPattern Software
  - For TSW3085 and TSW30H84, configure the TSW3100 to output a 614.4 MSPS, LVDS DDR format, 30-MHz IF Single-Carrier WCDMA output. See Figure 13 for details.
    - Change Interpolation value to DAC Clock Rate / Interpolation / 3.84 (i.e., **1228.8** / **2**/ **3.84** = **160**)
    - Enter desired Offset Frequency (i.e., 30 MHz) for each desired carrier
    - Select the **LVDS** output button
    - Check the *LOAD and Run* box
    - Press the green *Create* button

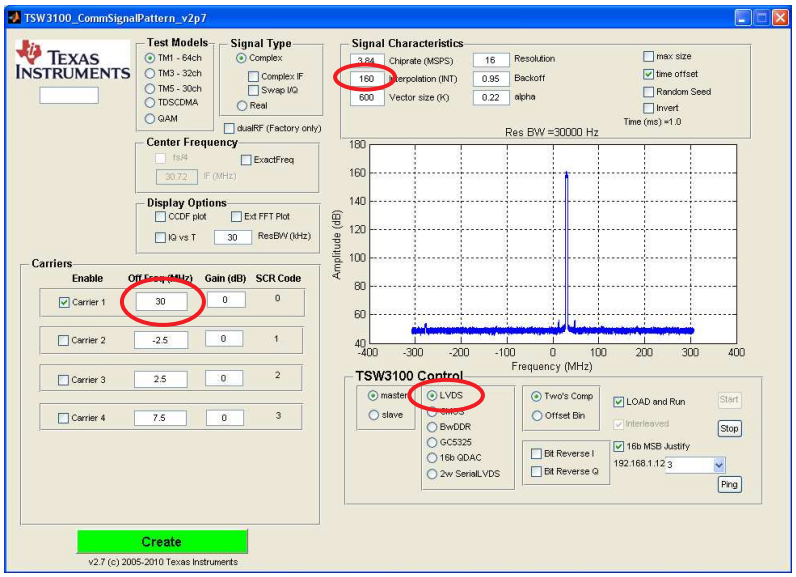


Figure 13. TSW3100 GUI for LVDS DDR Format

  - For TSW3084, configure the TSW3100 to output a 307.2 MSPS, LVDS Quad Interleave format, 30-MHz IF Single-Carrier WCDMA output.
    - Change Interpolation value to DAC Clock Rate / Interpolation / 3.84 (i.e., **1228.8** / **4** / **3.84** = **80**)
    - Enter desired Offset Frequency (i.e., 30 MHz) for each desired carrier
    - Select the **16b QDAC** output button
    - Check the *LOAD and Run* box
    - Press the green *Create* button

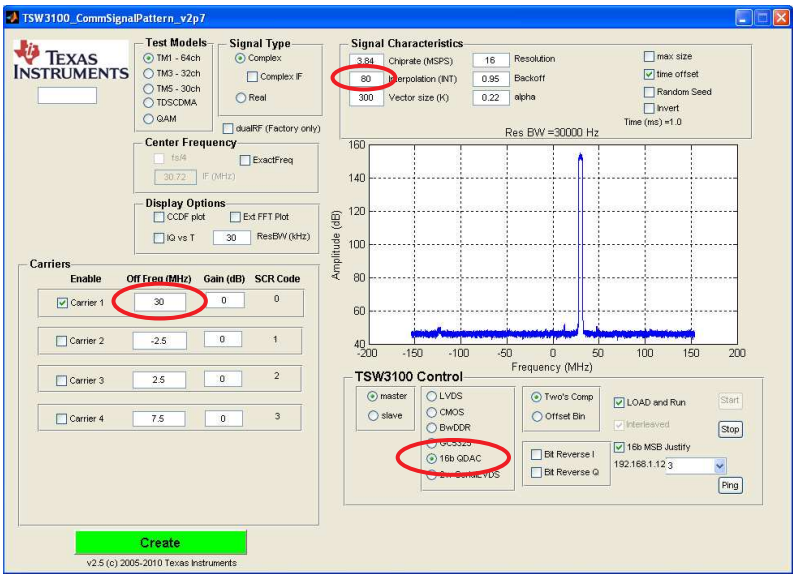
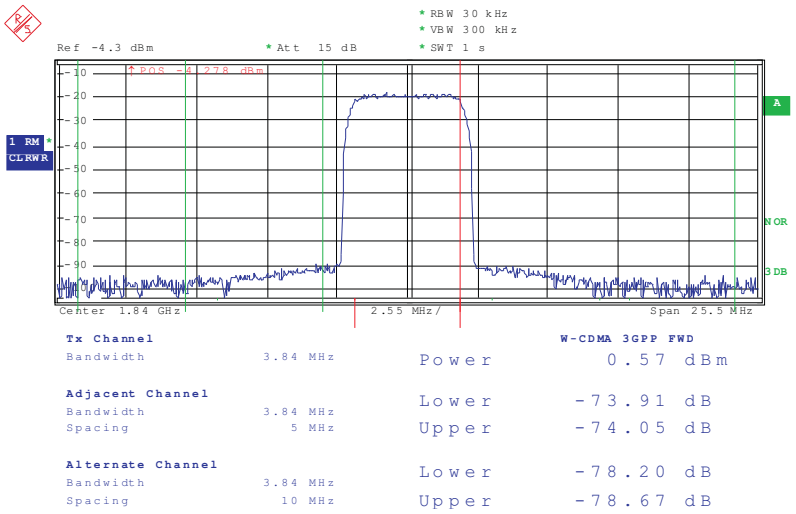


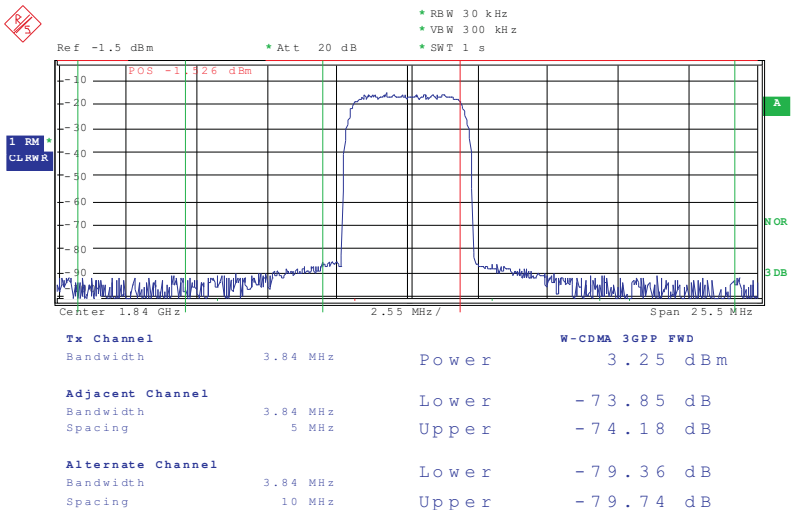
Figure 14. TSW3100 GUI for LVDS Quad Interleaved Format

- Verify the spectrum using the Spectrum Analyzer at the two RF outputs of the TSW308xEVM (J7 for TSW3085. J7 and J9 for TSW3084 and TSW30H84).
- **(Toggle the SIF SYNC button to synchronize the appropriate digital blocks, if example file with NCO setting is used.)**



NOTE: Baseband = 30 MHz, NCO = 30 MHz with NCO Gain disabled, QMC Gain = 1446, LO = 1780 MHz

Figure 15. TSW308x WCDMA Output (TRF3705 Low-Gain Mode)



NOTE: Baseband = 30 MHz, NCO = 30 MHz with NCO Gain disabled, QMC Gain = 1446, LO = 1780 MHz

Figure 16. TSW308x WCDMA Output (TRF3705 High-Gain Mode)

4 Optional Configuration

The onboard LMK04806B has the following configuration options for the flexible clocking of the DAC348x.

Figure 17. LMK04806 Mode Selection

4.1 Configuring the LMK0480x for Clock Distribution Mode

To use this mode:

- Provide a 2.4-Vpp maximum, 3.1-GHz maximum external clock at SMA J12.
- Select the *Clock Distribution* option in the LMK04806 Control tab.

4.2 Configuring the LMK0480x for Single PLL (PLL2 Only) Mode

To use this mode:

- The default reference is a 10-MHz crystal oscillator for the Single PLL mode.
- A 3.3-Vpp maximum, 140-MHz maximum external reference can be applied at SMA J11.
  - For the TSW3085EVM, set JP5 to the 2-3 position.
  - For the TSW3084EVM and TSW30H84EVM, set SJP5 to the 2-3 position.
- Select the *PLL2* options in the LMK04806 Control tab.

4.3 Configuring the LMK0480x for Dual PLL (PLL1 + PLL2) Mode.

To use this mode, the following steps must be made to the EVM:

- Replace oscillator Y1 with a VCXO, such as a FVXO-HC73 series 3.3V VCXO from Fox.
- For the TSW3085EVM, install R273, R274, R76, C116, and C122.
- For the TSW3084EVM and TSW30H84EVM, install R273, R274, R90, C177, and C300.
- Provide an external reference at SMA J12.
- Select the Dual PLL options in the LMK04806 Control tab.

Consult the LMK0480x data sheet for proper device configuration for this mode of operation.

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 5.5 V to 7 V and the output voltage range of 0 V to 3.3 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

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During normal operation, some circuit components may have case temperatures greater than 60° C. The EVM is designed to operate properly with certain components above 60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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