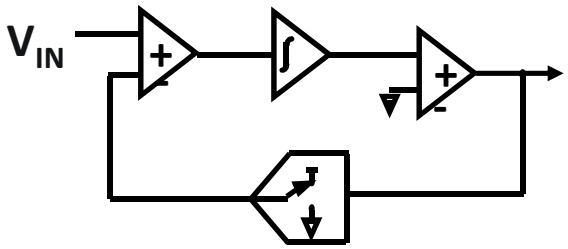
Common ADC Architectures: Internal Anatomy Key Takeaways

Delta Sigma (ΔΣ)

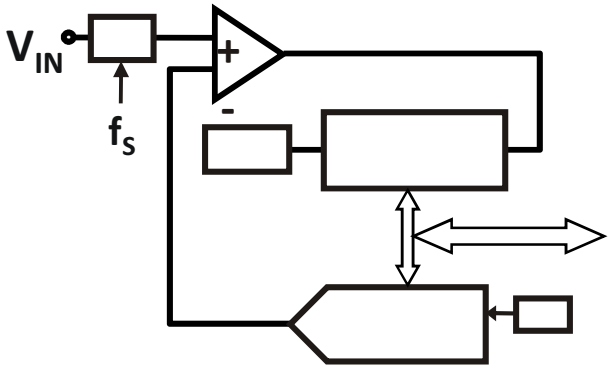


Delta-Sigma
Resolution: 16-24 bits
Speed: 1ksps-10Msps
Latency: Long

Highlights:
- Low cost (essentially a digital part)
- High resolution and accuracy

Challenges:
- Limited frequency response
- Most effective with continuous inputs
- Latency

SAR

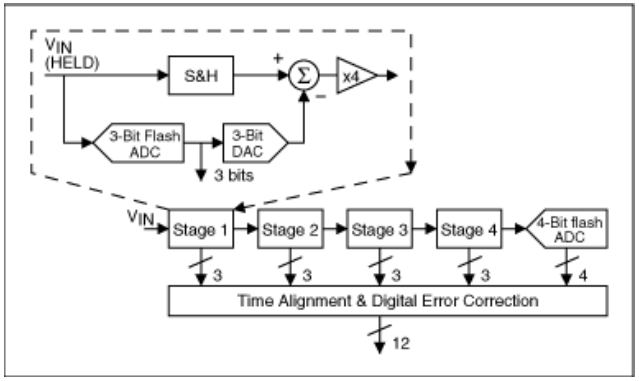


SAR
Resolution: 8-18 bits
Speed: 5ksps-5Msps
Latency: None

Highlights:
- Low Power
- No Latency
- Easy to use and multiplex
- High resolution and accuracy

Challenges:
- Sampling Rate Limited to ~5MSPS

Pipeline



Pipeline
Resolution: 8-16 bits
Speed: 5Msps-1Gsps
Latency: Some

Highlights:
- High Speed
- High Bandwidth

Challenges:
- Lower resolution
- Pipeline delay / latency
- Power consumption

ADC Checklist

- Aiming Application

1) SPEED (Sample Rate)_____ and RESOLUTION____ bits

- ***Accuracy expectation***
- ***Which one is more important? S or R***
- ***Is there a preferred Architecture? D-S, S, P***

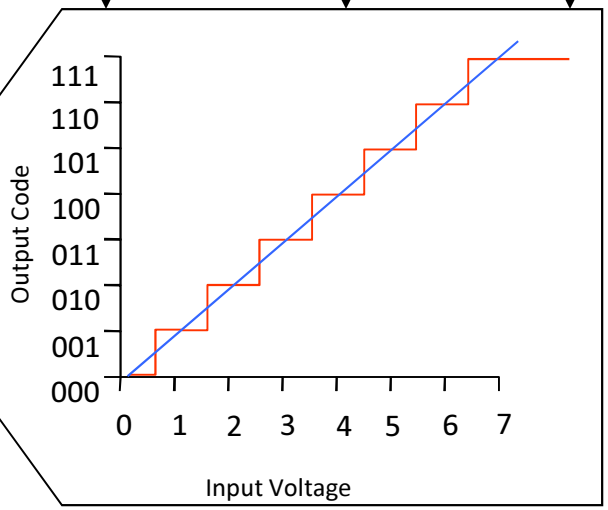
Analog Supply Voltage AVDD ____

Reference Voltage VRef ____

Digital Supply Voltage DVDD ____

2) Analog Input A_{IN}

Number of Channels _____
Muxed or Simultaneous
Single Ended or Differential
Unipolar or Bipolar
Input Voltage Range _____



3) Digital Output D_{OUT}

Interface:
Serial/SPI
I²C
Parallel
LVDS: Serialized or Parallel

4) Other limitations

Power Budget: **Is Size a Concern:** **Processor/FPGA:**

Sample Need Date: **Production Need Date:** **Cost Goal:** **Volume:**