Interfacing the ADS8332 to TMS320F28335 DSP

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ABSTRACT

This application report presents a solution for interfacing the 8-channel, 16-bit successive approximation register (SAR), analog-to-digital converter (ADC) ADS8332, to the serial peripheral interface (SPI) port of the TMS320F28335 DSP. The main focus of this report is the TMS320F28335 SPI port's configuration and initialization and the ADS8332's software control. The software demonstrates how to achieve exact conversion control by using the DSP timer and configure an external interrupt receiver on the DSP to collect the conversion result.

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1. Introduction

The ADS8332 is an 8-channel, 16-bit, 500 Kilosamples-per-second (KSPS), SAR, ADC with SPI interface and non-simultaneous sampling ADC with internal unipolar 8-to-1 input multiplexer. The ADS8331 offers the same core with a 4-channel option. This application report presents a hardware and software solution for interfacing and using the ADS8332 with the popular TMS320F28335 Digital Signal Processor (DSP™). The software for this report was developed with *Code Composer Studio*™ V3.3 based on the eZdsp™ F28335 from Spectrum Digital Incorporated and the ADS8332EVM from Texas Instruments. This sample code uses Timer0 of the TMS320F28335 DSP to create exact sampling control by general purpose I/O (GPIO) and uses external interrupt to collect 8192 samples from the ADS8332 data converter. Search "Interfacing the ADS8332 to the TMS320F28335" on the www.ti.com website for the associated software in zip format.
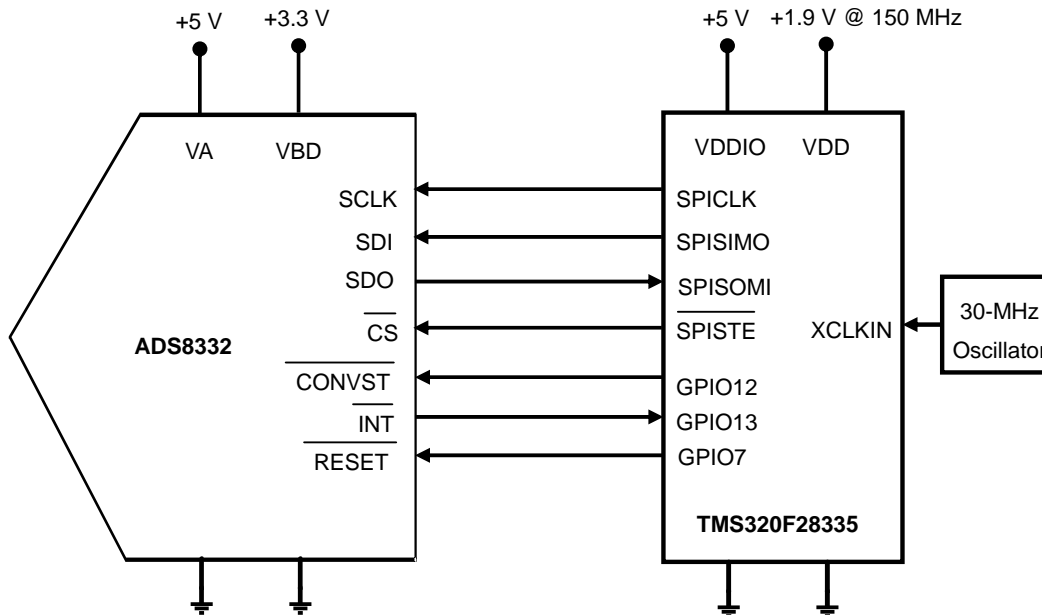
Figure 1. Hardware Connection

2. ADS8332 Interface

An internal oscillator in the ADS8332 can be used as the conversion clock (CCLK) source and also can be programmed to run the conversions using the external CPU's serial clock (SCLK). For simplicity, this report uses the internal oscillator.

The ADS8332 requires 18 conversion clock (CCLK) cycles to complete a conversion, and the minimum acquisition and sampling time is 3 CCLKs. The minimum time between two consecutive $\overline{CONVST}$ signals for the ADS8332 is 21 CCLKs (1826 ns with an 11.5-MHz typical internal CCLK).

The ADS8332 is programmable for Manual Channel Select mode, enabled through the configuration register (CFR) by setting the CFR_D11 bit to *0*, and then the desired channel is selected by writing to the command register (CMR). Auto Channel Select mode is enabled by setting the CFR_D11 bit to *1*, the first conversion is always from the channel of the last conversion completed before this mode is enabled.

The ADS8332 is configured for Manual-Trigger Mode by setting the CFR_D9 bit to *1*, the conversion can be initiated on the falling of the $\overline{CONVST}$ signal. Auto-Trigger Mode can also be selected by setting the CFR_D9 bit to *0*, automatically start conversion without $\overline{CONVST}$ signal.

Table 1 summarizes the different conversion modes.

Table 1. Different Types of Conversion Modes

Mode	Select Channel	Start Conversion
Automatic	**Auto Channel Select**	**Auto-Trigger Mode**
	No need to write channel number. Use internal sequence for ADS8332.	Start conversion based on conversion clock CCLK
Manual	**Manual Channel Select**	**Manual-Trigger Mode**
	Write channel number to CMR	Start conversion with $\overline{CONVST}$

Tips:

1. The conversion result can be read while converting or sampling; read while sampling, the data is the current conversion result, read while converting, the data is the previous conversion result.

2. The output data should be read during one conversion period, it depends on the sampling rate and SCLK frequency of DSP SPI port.

3. Select Auto Channel Select mode to reduce the DSP's resource allocation. To implement the desired sampling rate, Manual-Trigger is often used. Both are used in this report.

4. The ADS8332 also supports three power-down modes to reduce power dissipation; Nap, Deep, and Auto-Nap. For most industrial applications, it's not necessary, so this report does not use these power-down modes.

Table 2 shows the connections required for interfacing the ADS8332 to the TMS320F28335 DSP.

Table 2. ADS8332 to TMS320F28335 Interface Definition

DSP Pin No. (PGF package)	DSP Pin function	ADC Pin No. (TSSOP package)	Signal Description
62	SPICLK	10	SPI clock for serial interface (SCLK)
27	SPISIMO	12	SPI serial data in (SDI)
28	SPISOMI	13	SPI serial data out (SDO)
63	$\overline{\text{SPISTE}}$	11	Chip select input for SPI ($\overline{\text{CS}}$)
21	GPIO12	15	Conversion start ($\overline{\text{CONVST}}$)
24	GPIO13	9	Status output (EOC/$\overline{\text{INT}}$/CDI)
16	GPIO7	8	External reset ($\overline{\text{RESET}}$)

3. TMS320F28335 SPI Interface

Configure the SPI port of TMS320F28335 as the master by setting the MASTER/SLAVE bit to *1* (SPICTL.2) in spi_init() of mail.c.

3.1 SPI Clocking Schemes and Setting

The SPI's CLOCK POLARITY bit (SPICCR.6) and the CLOCK PHASE bit (SPICTL.3) control four different clocking schemes on the SPICLK pin as following: the CLOCK POLARITY bit selects the active edge, either rising or falling of the clock, the CLOCK PHASE bit controls the phase of the SPICLK signal. These two bits can be set in spi_init() of mail.c.

Table 3. SPI Clocking Scheme

Clock Polarity (SPICCR.6)	Clock Phase (SPICTL.3)	Clocking Scheme Description
0	0	Transmits data on the rising edge and receives data on the falling edge of SPICLK
0	1	Transmits data one half-cycle ahead of the rising edge and receives data on the rising edge of the SPICLK
1	0	Transmits data on the falling edge and receives data on the rising edge of the SPICLK
1	1	Transmits data one half-cycle ahead of the falling edge and receives data on the falling edge of the SPICLK

Because the ADS8332's output data bits are valid on the falling edge of SCLK with the t_{D2} delay (Figure 3 in the ADS8332's datasheet) and the data input is read on the falling edge of SCLK, so the SPI Clocking Scheme of TMS320F28335 can be configured to 00 or 11 (Clock Polarity : Clock Phase).

The SPI baud rate is decided by SPI SPIBRR register and LSPCLK. LSPCLK is decided by LOSPCP register and SYSCLKOUT. SYSCLKOUT is determined by OSCCLK (XCLKIN), PLLCR[DIV] and PLLSTS[DIVSEL] registers. LOSPCP can be found in DSP2833x_SysCtrl.c, PLLCR and PLLSTS[DIVSEL] in DSP2833x_Examples.h.

$$\text{SPI Baud Rate} = \frac{\text{LSPCLK}}{(\text{SPIBRR} + 1)} = \frac{\text{SYSCLKOUT}}{(\text{SPIBRR} + 1) * (\text{LOSPCP} * 2)}$$

Where:

LSPCLK = Low-speed peripheral clock

SPIBRR = SPI baud-rate register

LOSPCP = Low-speed peripheral clock prescaler register

SYSCLKOUT = System clock

OSCCLK = CLKIN = External oscillator clock

PLLCR = PLL control register

PLLSTS = PLL status register

In the software code for this report, the default values: PLLCR = 10, PLLSTS = 2,

$$\text{SYSCLKOUT} = \frac{\text{OSCCLK} * 10}{2} = \frac{\text{XCLKIN} * 10}{2} = \frac{30\text{MHz} * 10}{2} = 150\text{MHz}$$

The default value for LOSPCP is 2(0x0002) in InitPeripheralClocks() of DSP2833x_SysCtrl.c, SPIBRR is set to 10 (0x000A) in spi_init() of main.c, so

$$\text{SPI Baud Rate} = \frac{\text{SYSCLKOUT}}{(\text{SPIBRR} + 1) * (\text{LOSPCP} * 2)} = \frac{150\text{MHz}}{11 * 4} = 3.4\text{MHz}$$

The maximum SPI clock frequency the ADS8332 can accept is 40 MHz.

3.2 GPIO Pin Functions Setting

GPIO12, 13 and 7 pins are selected as a connection to ADS8332. DSP's GPAMUX1 register can configure these pins as GPIO function. When GPIO12 is configured as an output, it is assigned to the $\overline{\text{CONVST}}$ function. When GPIO13 is configured as an input, it is assigned to the $\overline{\text{INT}}$ function as an interrupt input from ADS8332. GPIO7 is configured as an output and assigned to $\overline{\text{RESET}}$ to ADC. The GPADIR register determines these GPIO's direction (input or output), the GPASET or GPACLEAR register decides the initialization status of these pins.

3.3 Timer Initialization and Configuration

In DSP2833x_CpuTimers.c, InitCpuTimers(void) is used to initialize CPU timers to a known state, ConfigCpuTimer(struct CPUTIMER_VARS *Timer, float Freq, float Period) is used to configure the selected timer (Timer0) to the specified period, here the *Freq* should be entered as *MHz* and the Period in *μSeconds*.

The Timer0 can be used to create an exact sampling control with GPIO12 pin as $\overline{\text{CONVST}}$ signal to ADS8332 ADC in Timer0 interrupt service subroutine of the main.c file. One $\overline{\text{CONVST}}$ pulse is created for one interrupt. The Sampling_Period in main.c is used to set the Timer0 interrupt interval. When the Sampling_Period is set to 1000, Timer0 creates one Timer interrupt per 1000 μs, this means that the sampling rate of the ADS8332 is 1 KSPS. If the Sampling_Period is set to 10, the sampling rate of the ADS8332 is 100 KSPS.

3.4 External Interrupt Setting

GPIO13 of the DSP is selected by GPIOXINT1SEL register as XINT1 external interrupt input in main.c file. XINT1CR external interrupt control register in main.c determines whether the interrupts are triggered on the rising edge, the falling edge of a signal or both the rising and falling edges on the GPIO13 pin. The falling edge is default for this application report.

4. ADC Configuration and Operation

4.1 $\overline{\text{RESET}}$

Except internal power-on reset (POR) and software reset, an external reset signal can be used to $\overline{\text{RESET}}$ pin of ADS8332 from GPIO7 of DSP, this pin must be held at low pulse for a minimum of 25 ns to reset the device and return to default mode.

4.2 $\overline{\text{INT}}$

The status output pin can be programmed as an EOC or $\overline{\text{INT}}$ output, it is set as interrupt output, $\overline{\text{INT}}$ in this report. The pin is low (default) after the end of conversion and returns high after $\overline{\text{CS}}$ goes low. The polarity of this pin can be programmed through the D7 bit of ADS8332's CFR register.

4.3 $\overline{\text{CS}}$

The $\overline{\text{SPISTE}}$ signal from the DSP can be connected to the $\overline{\text{CS}}$ pin of ADS8332 as Chip Select function. This pin is automatically driven low by the DSP before transmitting data to the ADS8332 and is taken high after the transmission is complete.

4.4 Writing and Reading Register/Data

There are two different types of writes to the register of the ADS8332: a 4-bit write to the CMR register and a full 16-bit write to the CMR plus CFR registers. A simple write for Manual Channel Selection, Wake up and Default mode only needs four SCLKs. A 16-bit writing CFR or reading CFR/Data takes at least 16 SCLKs. Only writing to the CFR register requires a 4-bit CMR command followed by 12 bits of valid data to the CFR register.

The conversion result can be read through the SDO pin of the ADS8332 in DSP's interrupt service subroutine of main.c. Data output from the SDO is left-adjusted MSB first. The output data bits are valid on the falling edge of SCLK. Generally 16 SCLKs are necessary, depending on read mode.

4.5 Starting Conversion

ADS8332's conversion for Manual-Trigger mode can be initiated by bringing the $\overline{\text{CONVST}}$ pin (GPIO12 from DSP) low for a minimum of 40 ns and then brought high, at the same time the acquisition and sampling phase is ended. The ADS8332 switches from conversion to acquisition and sampling mode on the falling edge of the $\overline{\text{INT}}$ signal.

Channel selection can also be done automatically if Auto Channel Select mode is selected (default status in the software code for this application report). The signals from all channels are converted in a fixed order. The channels are scanned sequentially and automatically.
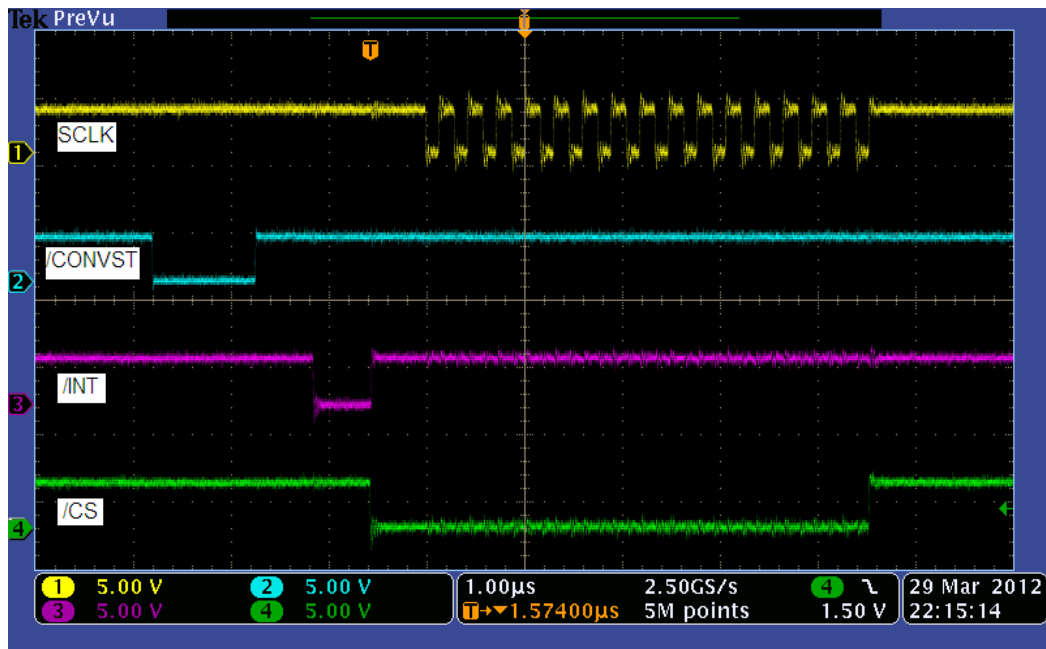
Figure 2. Screenshot of General Timing

5. Conclusion

This application report introduces a solution for interfacing the ADS8332 converter to the TMS320F28335 DSP, including hardware connection, software configuration and control. The software from this report can be used as sample code when developing specific application software. This application report is also suitable for ADS8331 ADC from Texas Instruments.

6. Reference

1. *ADS8332, ADS8331 datasheet* (SBAS363C)
2. *TMS320x2833x, 2823x Data Manual* (SPRS439M)
3. *TMS320x2833x, 2823x System Control and Interrupts Reference Guide* (SPRUFB0D)
4. *TMS320x2833x, 2823x Serial Peripheral Interface (SPI) Reference Guide* (SPRUEU3A)

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