Precision DAC Essentials

Precision DAC Applications

Texas Instruments

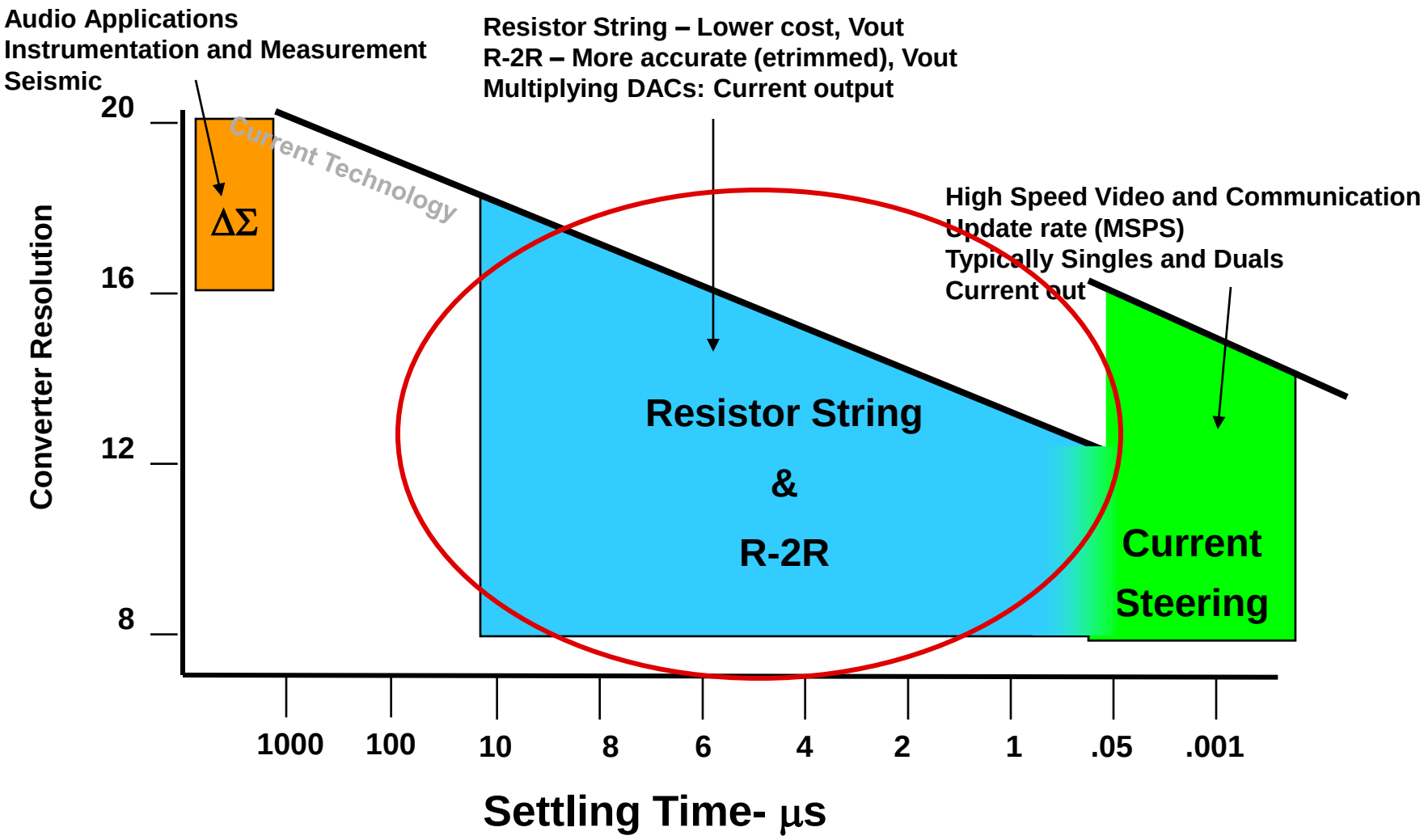
What is this presentation?

- A guide to understanding fundamental DAC specifications
- An explanation of DAC architectures to leverage when making device selection
- How TI measures each specification to provide an ‘apples to apples’ comparison to competitors devices

Presentation Agenda

- TI DAC Landscape & Precision DACs
- The Ideal DAC
- DAC Architectures
  - String
  - R2R MDAC
  - R2R BDAC
- Static DAC Specifications
  - TUE & Calibration
- Dynamic Specifications
- Closing the Loop

DAC Architectures & Applications



Precision DAC Strategy and Growth Areas

Industrial



Applications:
Industrial Automation - Sensors/PLC - Motor Control -
Test & Measurement Equipment

Products:
DAC8750/60 with 4-20mA and ±10V
DAC8770 with Power Management
DAC874x loop powered w. HART

Communications



Applications:
Basestation Analog Monitor and Control (AMC) -
WI - Backhaul - Optical Networking

Products:
AMC7832 12 bit integrated ADC & DAC
AMC7834: 12 bit integrated ADC & DAC
AMC7812 12 bit integrated ADC & DAC

Catalog & Automotive



Applications:
Medical -Automotive - Consumer - Computer

Products:
DAC8562 smallest 2-channel DAC
DAC7311 1-channel DAC in SC70
DAC8568 8-channel 16-Bit DAC

*Devices in RED are not yet released

> 600 orderables **> 1500 customers**

Texas Instruments

Where are Precision DACs used?

- DC Bias and offset control
- Closed loop control systems
- Driving a voltage controlled oscillator
- Automated test equipment
- Industrial Communication

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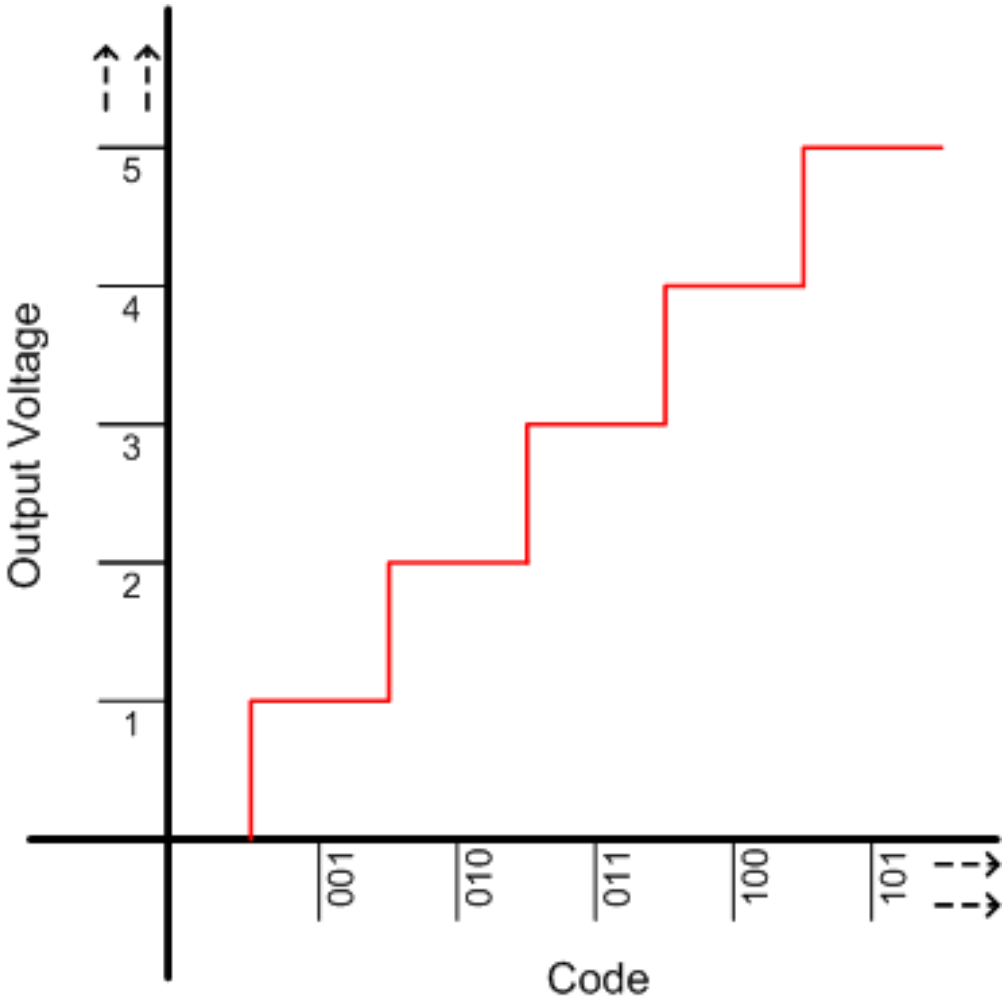
Ideal Transfer Function



Resolution = ***n*** – The number of bits used to quantify the output

Codes = 2^n – The number of input code combinations

Full Scale code = 2^n-1 – The largest code that can be written

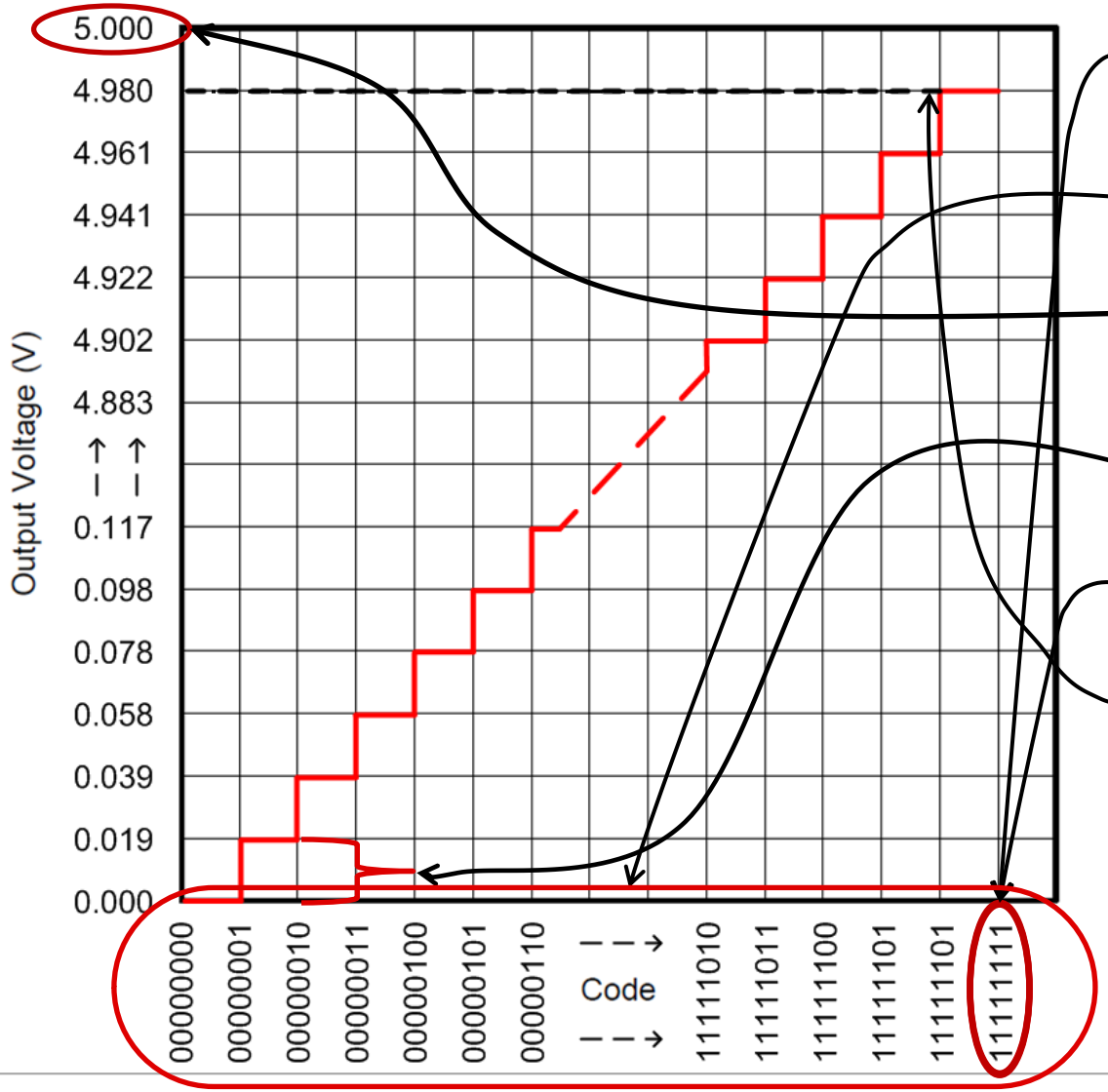
Reference Voltage = **Vref** – Sets the LSB voltage or current size and converter range

LSB = **Vref / 2^n** – The output voltage or current step size of each code

Full Scale Voltage = **Vref – 1LSB** – Full scale output voltage of the DAC

Transfer Function = **Vref x (code/ 2^n)** – Relationship between input data word and output voltage or current

Example DAC Transfer Function



Bits = ***n*** = **8 bits**

Codes = 2^n = **256**

Reference Voltage = **Vref** = **5.00V**

LSB = **Vref** / 2^n = **19mV**

Full Scale code = 2^n**-1** = **0xFF**

Full Scale Voltage = **Vref – 1LSB = 4.980V**

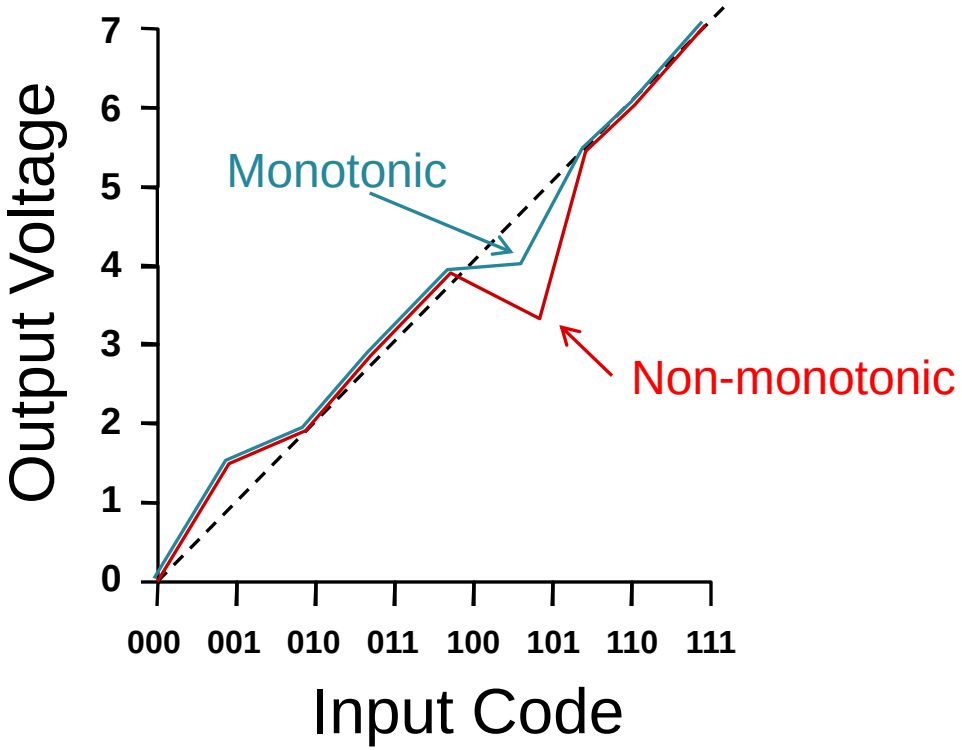
Transfer Function = **Vref x (code/ 2^n) =**

Vout = 5V x (code/ 256)

Ideal DAC Properties

- Near rail-to-rail output set by the reference input
  - Remember the full scale output voltage is Vref – 1 LSB
- Any two sequential codes are exactly 1 LSB apart
- No missing codes
- Instantaneous transition from code-to-code
- Fully monotonic

But what's Monotonicity?



In a monotonic DAC

- Analog output always increases or remains constant as the digital input increases.

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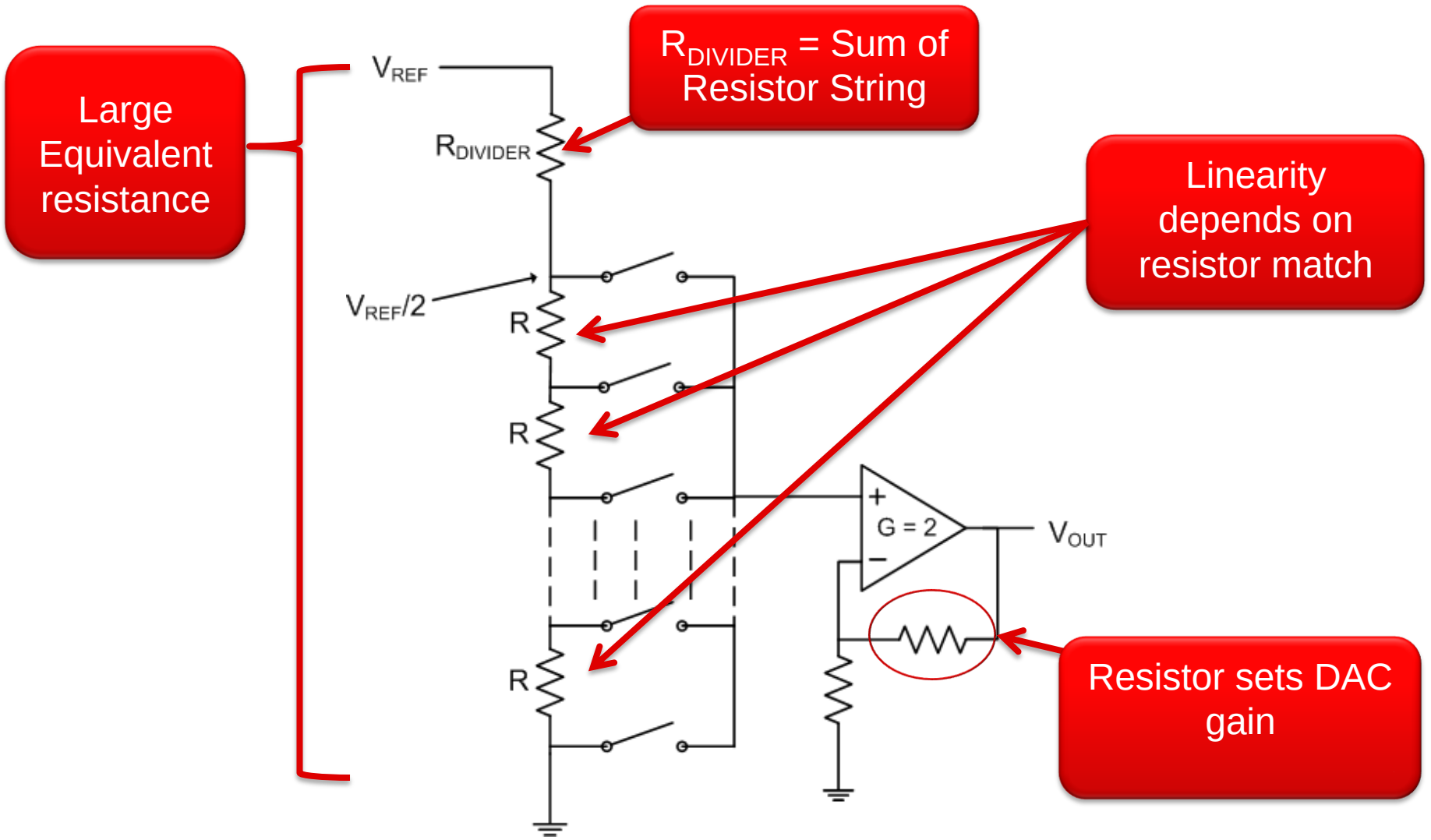
String DAC / Kelvin Divider DAC

The String DAC Architecture



String DAC

Advantages

- Inexpensive
- Low glitch energy
- Inherently monotonic
- Low power
- Small package

Disadvantages

- Limited resolution
- Linearity
- Buffer required to isolate from point of load

Applications

Portable equipment

Closed Loop Systems

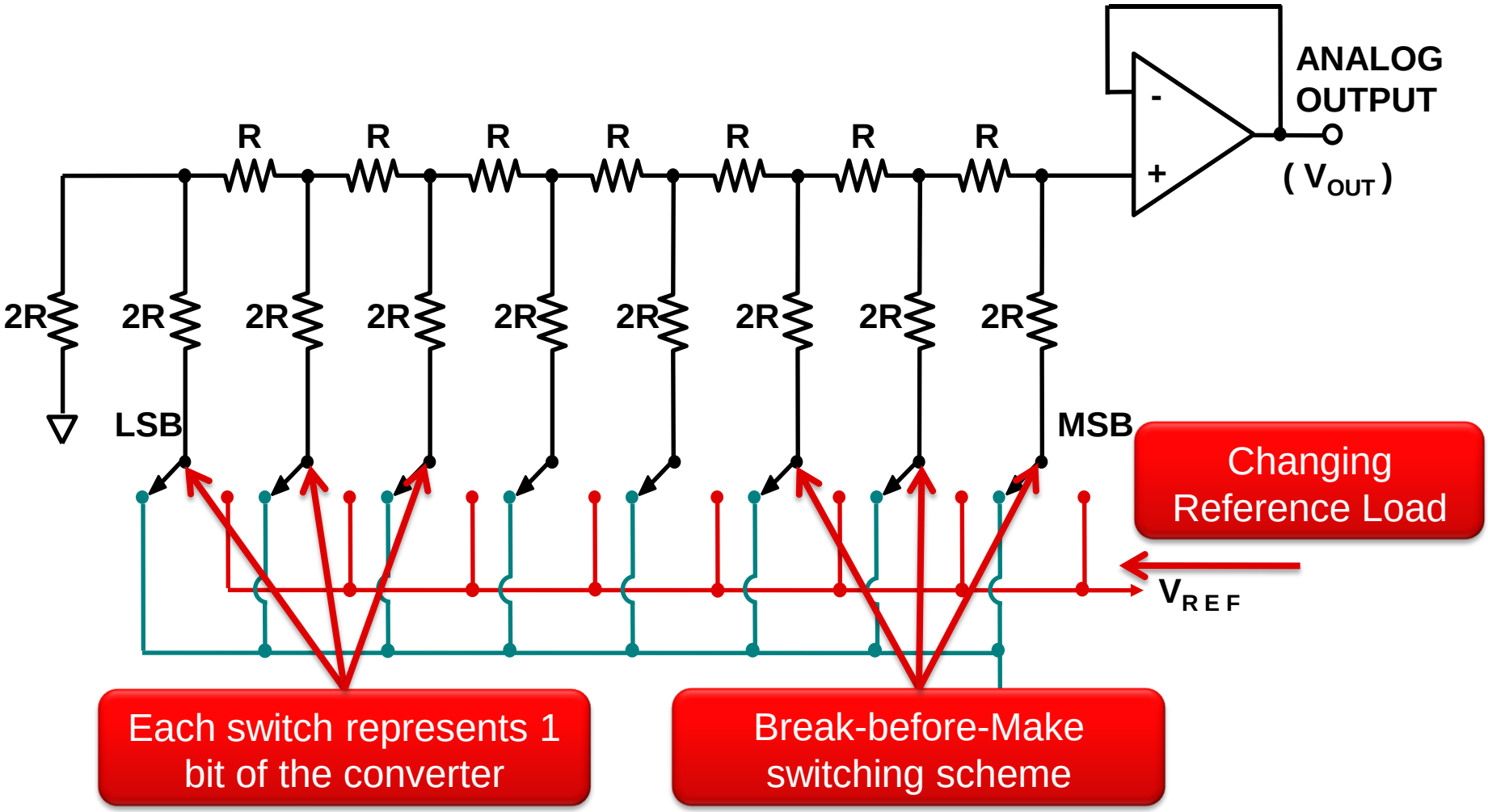
Adjustable Reference

DC Biasing

•Example parts: DAC8562, DAC8560, DAC8568, DAC7678, DAC8411, DAC8718, DAC8728

R-2R DAC / Back DAC

R-2R Back DAC


ANALOG
OUTPUT
(V_{OUT})
-
+
R
2R
LSB
MSB
V_{REF}
Changing
Reference Load
Each switch represents 1
bit of the converter
Break-before-Make
switching scheme

R-2R DAC

Advantages

- Strong linearity
- Low noise

Disadvantages

- Code dependent reference loading
- High glitch impulse
- Longer settling
- Output buffer requirements

Applications

Precision Instrumentation

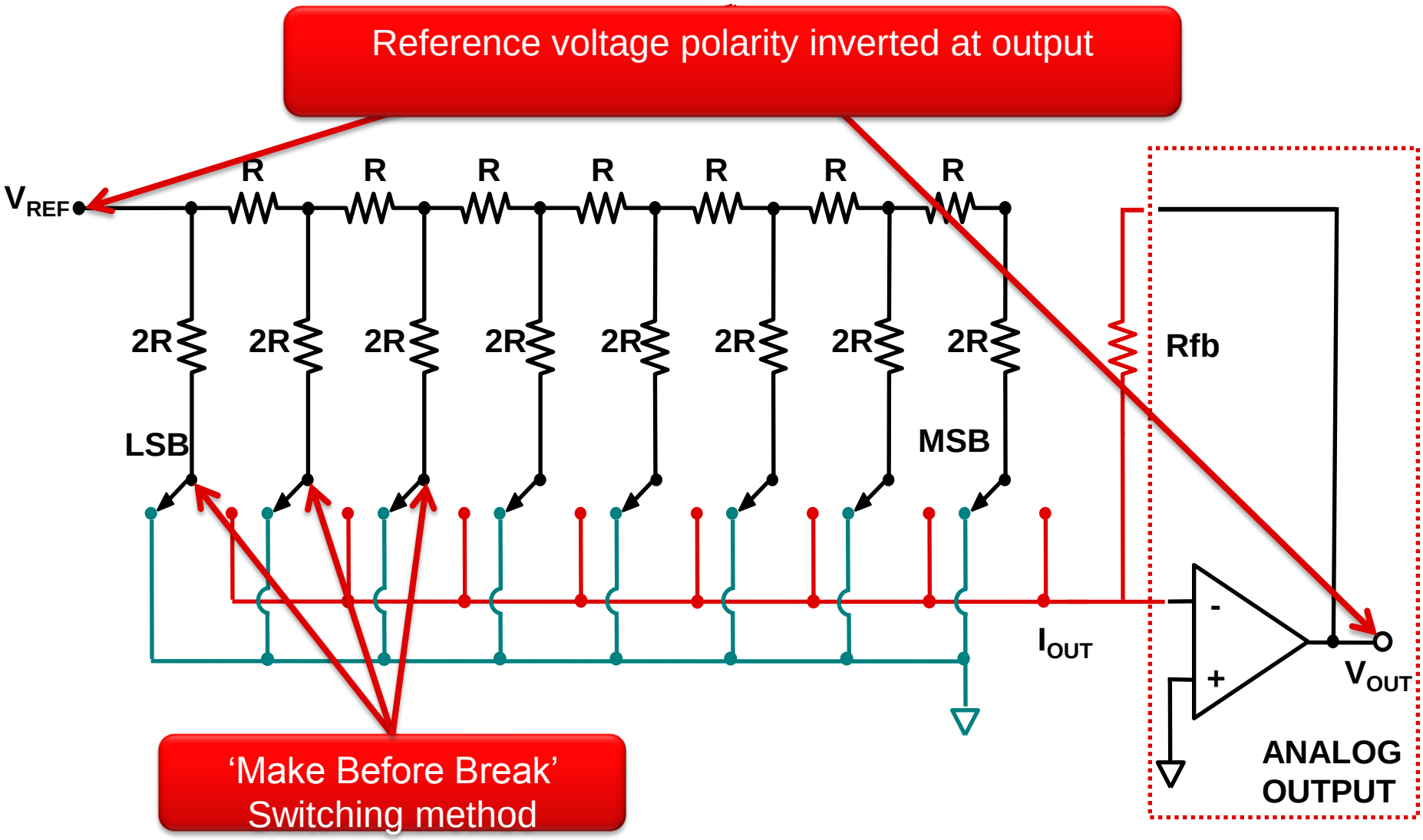
Industrial Control & Automation

Test Equipment

•Example parts: DAC7644, DAC7654, DAC8881, DAC9881

MDAC / R-2R Multiplying DAC

R-2R Multiplying DAC Architecture



MDAC

Advantages

- Strong linearity
- Low noise
- Fastest switching
- Lower glitch vs R-2R
- Constant reference loading

Disadvantages

- Transimpedance output stage
- Output is inverted referred to the reference

Applications

Industrial Control PLCs

Waveform Generation

AC Applications

•Example parts: DAC8801, DAC8811, DAC8814, DAC8822, DAC8734

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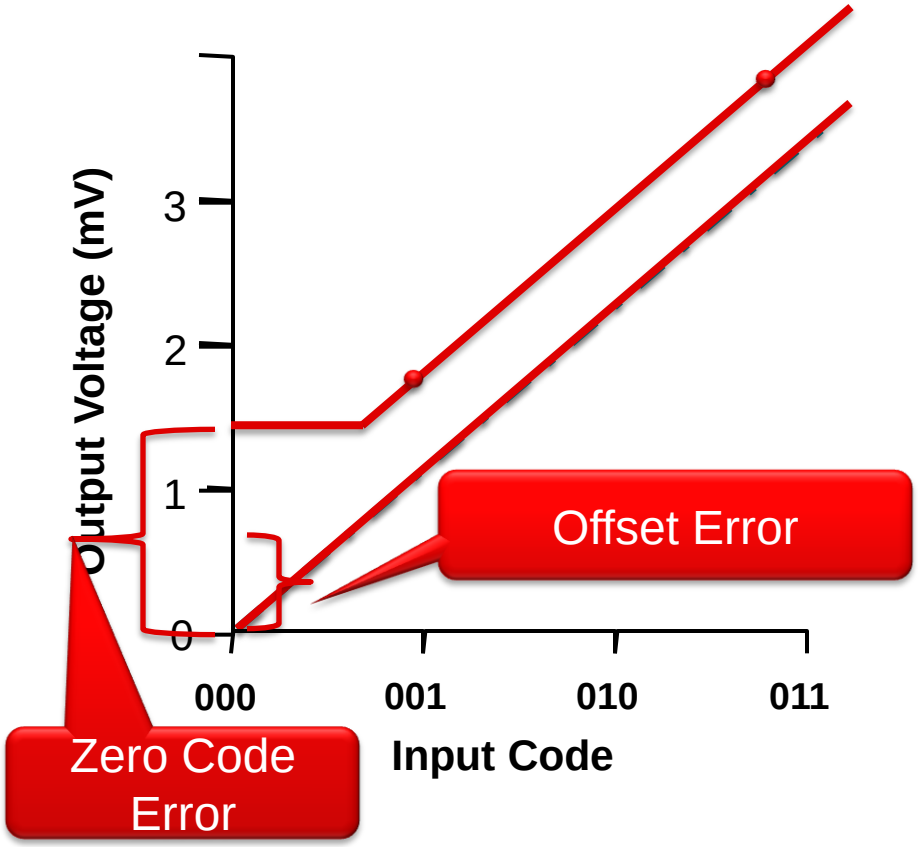
Offset & Zero Code Error



Offset Error(mV):

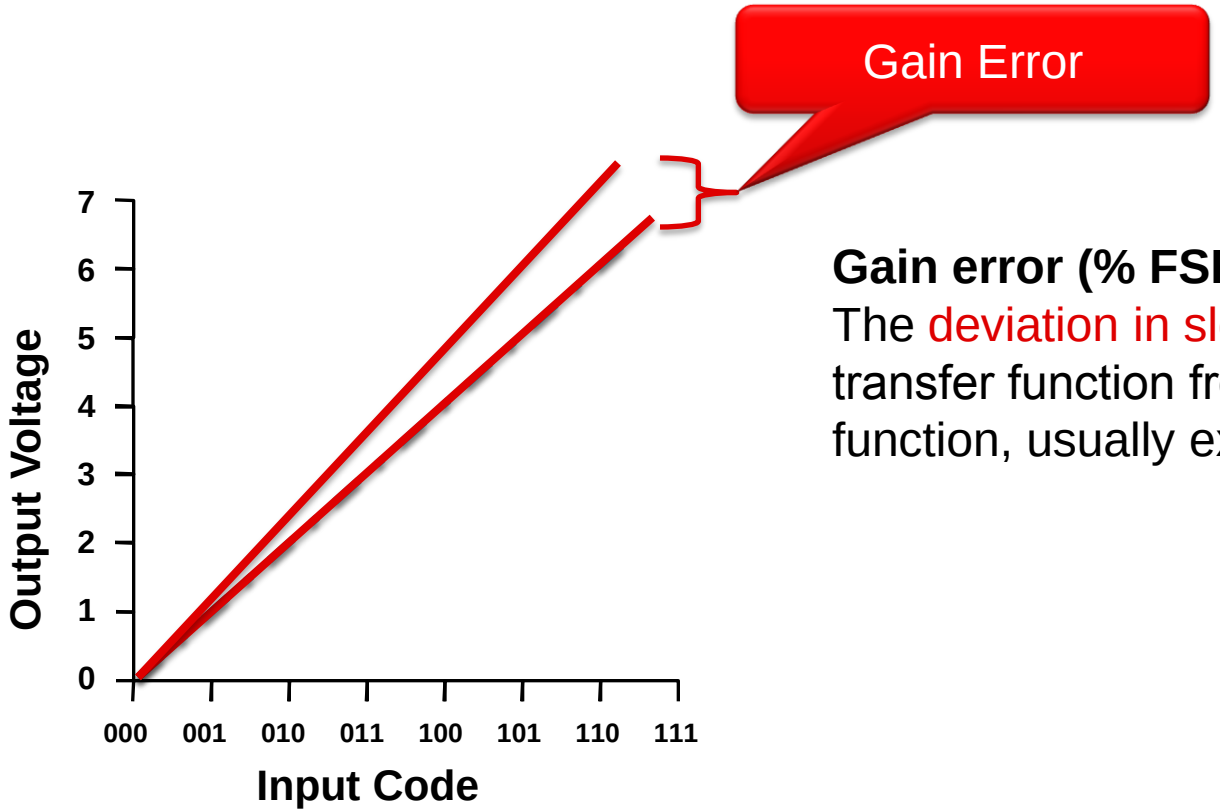
- Difference between measured and ideal output voltage in the linear region of the transfer function
- Indicates how much the entire transfer function is shifted from the ideal transfer function

Zero Code Error (mV):

- Output when loading all zeros into the DAC register
- Error is created from the internal op amp headroom from the negative rail.

Offset error	Extrapolated from two-point line[1], unloaded	±1	±4	mV
Zero-code error	DAC register loaded with all '0's	1	4	mV

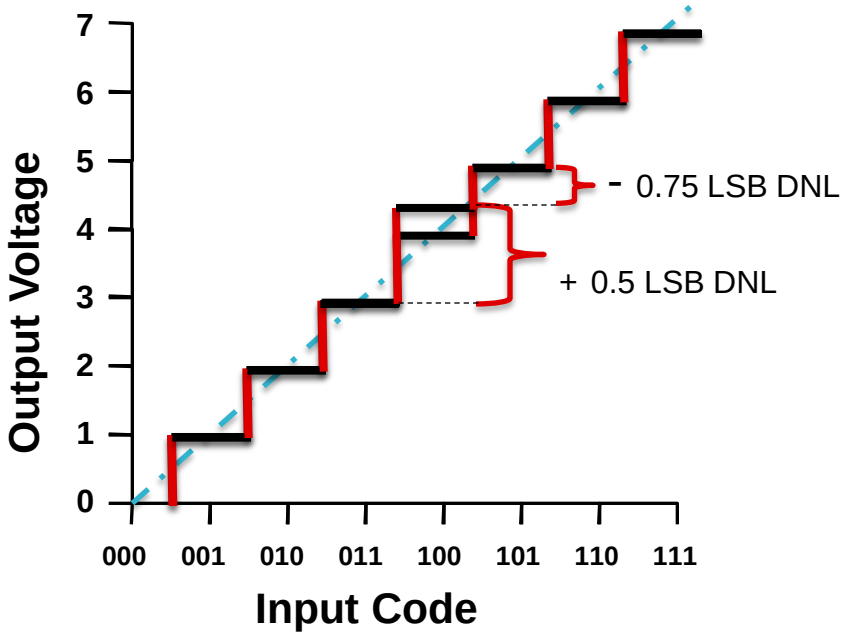
Gain Error



Gain error (% FSR):
The deviation in slope of the DAC's measured transfer function from it's ideal transfer function, usually expressed in %FSR

Gain error	Extrapolated from two-point line[1], unloaded	±0.01	±0.15	% of FSR

Differential Non Linearity (DNL)

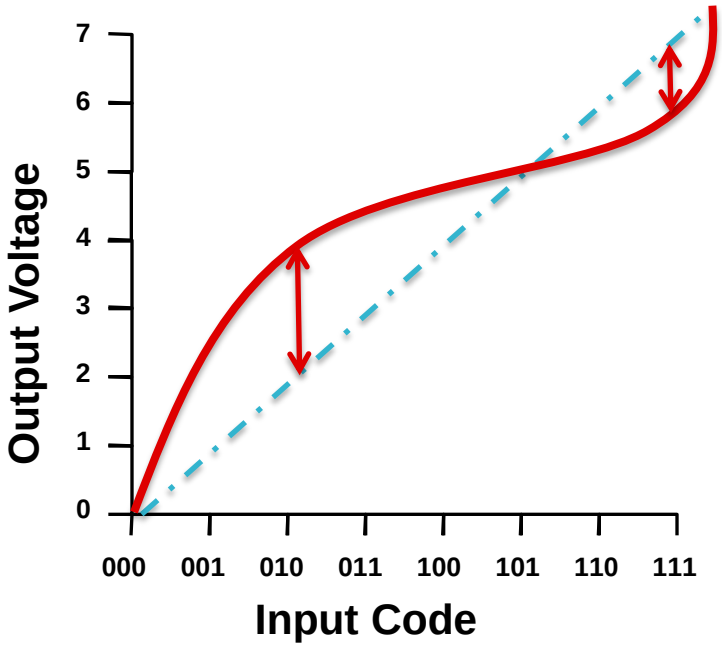


- Ideally LSB width stays constant for every sequential code transition - **DNL = 0**
- Actual DAC sequential code transitions are not all equal to 1 LSB - **DNL = +/- 1, 2, etc**
- DNL expresses the difference between measured LSB size and ideal LSB size for sequential DAC codes

$$DNL = \frac{V_{n+1} - V_n}{V_{lsb}} - 1$$

Resolution		16		Bits
Relative accuracy	Measured by the line passing through codes 485 and 64714		±4 ±12	LSB
Differential nonlinearity	16-bit monotonic		±0.2 ±1	LSB

Integral Non Linearity (INL)



INL is the **maximum** deviation between the ideal output of a DAC and the actual output level (corrected for offset and gain)

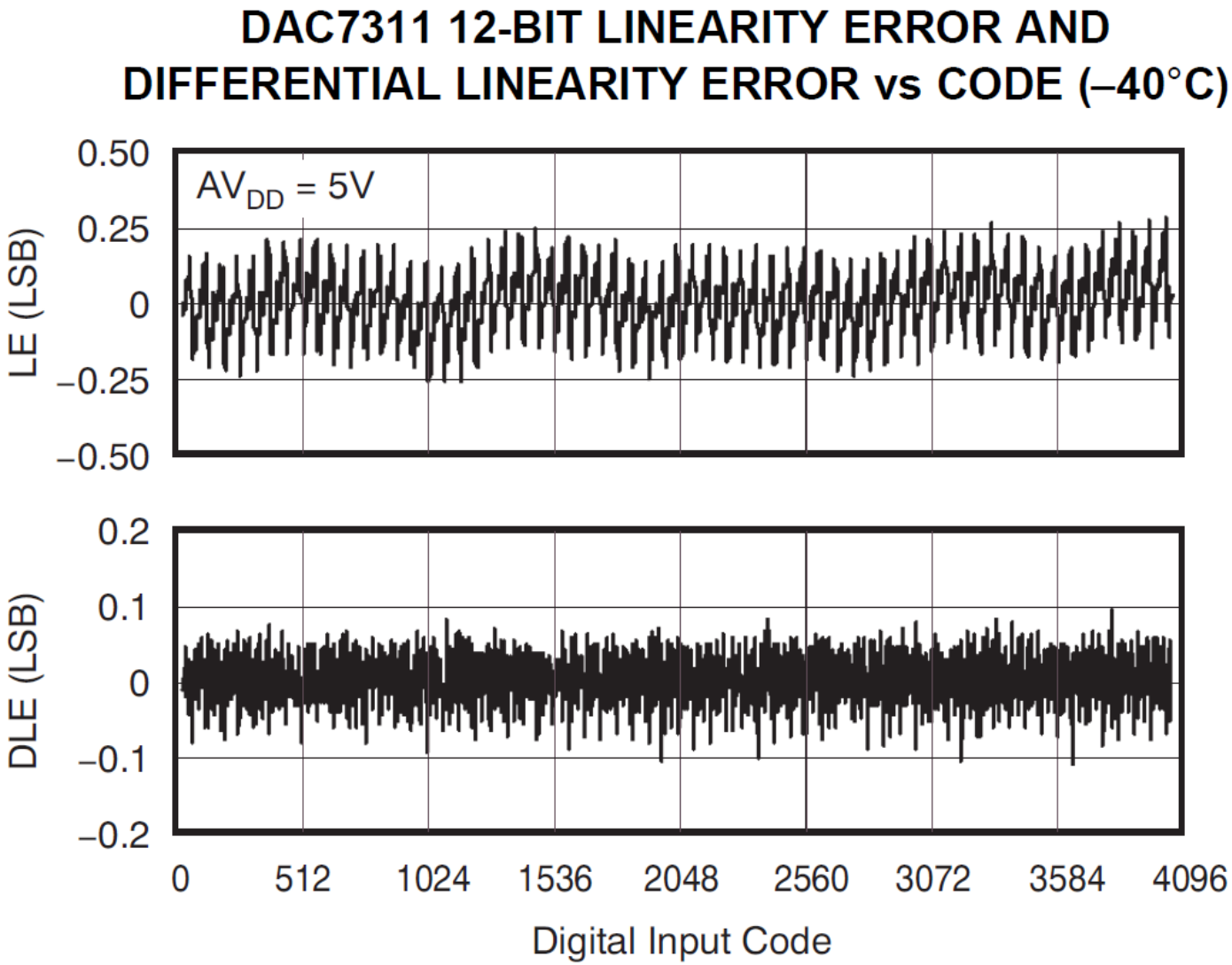
INL is often referred to as **"Relative Accuracy"**

Low max INL (≤1 LSB) is important in high accuracy applications

$$INL \cong \frac{V_n - V_{zero-scale}}{V_{lsb}} - n$$

Resolution		16		Bits
Relative accuracy	Measured by the line passing through codes 485 and 64714	±4	±12	LSB
Differential nonlinearity	16-bit monotonic	±0.2	±1	LSB

INL & DNL Graphs



Comparing Specifications

	LSB	Volts	% FSR	PPM
LSB	***	$\frac{LSB}{2^N} \times V_{REF}$	$\frac{LSB}{2^N} \times 100$	$\frac{LSB}{2^N} \times 10^6$
Volts	$\frac{V \times 2^N}{V_{REF}}$	***	$\frac{V}{V_{REF}} \times 100$	$\frac{V}{V_{REF}} \times 10^6$
% FSR	$\frac{\%}{100} \times 2^N$	$\% \times V_{REF}$	***	$\% \times 10^4$
PPM	$\frac{PPM}{10^6} \times 2^N$	$\frac{PPM}{10^6} \times V_{REF}$	$\frac{PPM}{10^4}$	***

Total Unadjusted Error

- Static specifications likely carry the largest impact on total unadjusted error in any system
  - INL/DNL
  - Offset Error
  - Gain Error
- Reference accuracy in any data conversion is key
- A root-sum-squared approach is appropriate to summarize the TUE

$$TUE = \sqrt{inlError^2 + gainError^2 + offsetError^2}$$

Total Unadjusted Error

$$TUE = \sqrt{inlError^2 + gainError^2 + offsetError^2}$$

- DAC8562 – 16 bit, 0-5V output
  - INL Error: +/- 12 LSB — 12 LSBs
  - Offset Error: +/- 4mV — 52 LSBs
  - Gain Error: +/- 0.15% FSR — 98 LSBs
- Probable Maximum TUE = +/-111 LSBs, +/-8.5mV, or 0.17% FSR
- Typical TUE = +/- 23 LSBs, 1.78 mV, or 0.0356% FSR
- Absolute Maximum TUE = 150 LSBs

Calibration & Total Unadjusted Error

$$TUE = \sqrt{inlError^2 + gainError^2 + offsetError^2}$$

- INL errors are unavoidable
- Digital calibration can remove offset & gain error
- First, calibrate offset error by taking a two point measurement to determine system offset error

$$AdjustedCode = Code + OffsetCalCode$$

- Next, determine the required scalar to set the offset corrected DAC output full scale output to the ideal full scale output voltage

$$AdjustedCode = GainCalRatio * Code + OffsetCalCode$$

- TUE is greatly improved by removal of offset & gain error
  - Max calibrated TUE: 12 LSBs, 0.91mV, or 0.01% FSR
  - Typ calibrated TUE: 4 LSBs, 0.305mV, or 0.006% FSR

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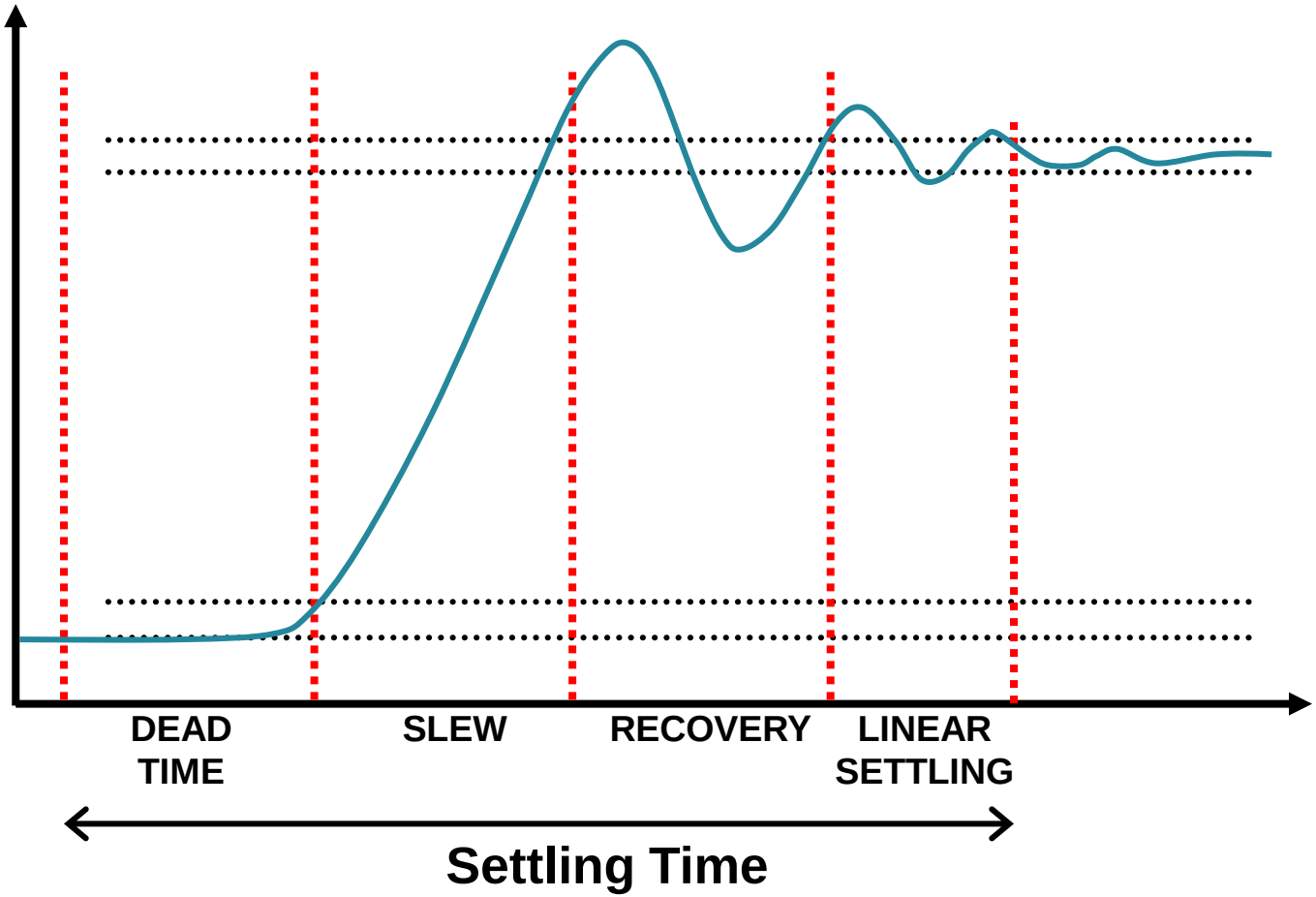
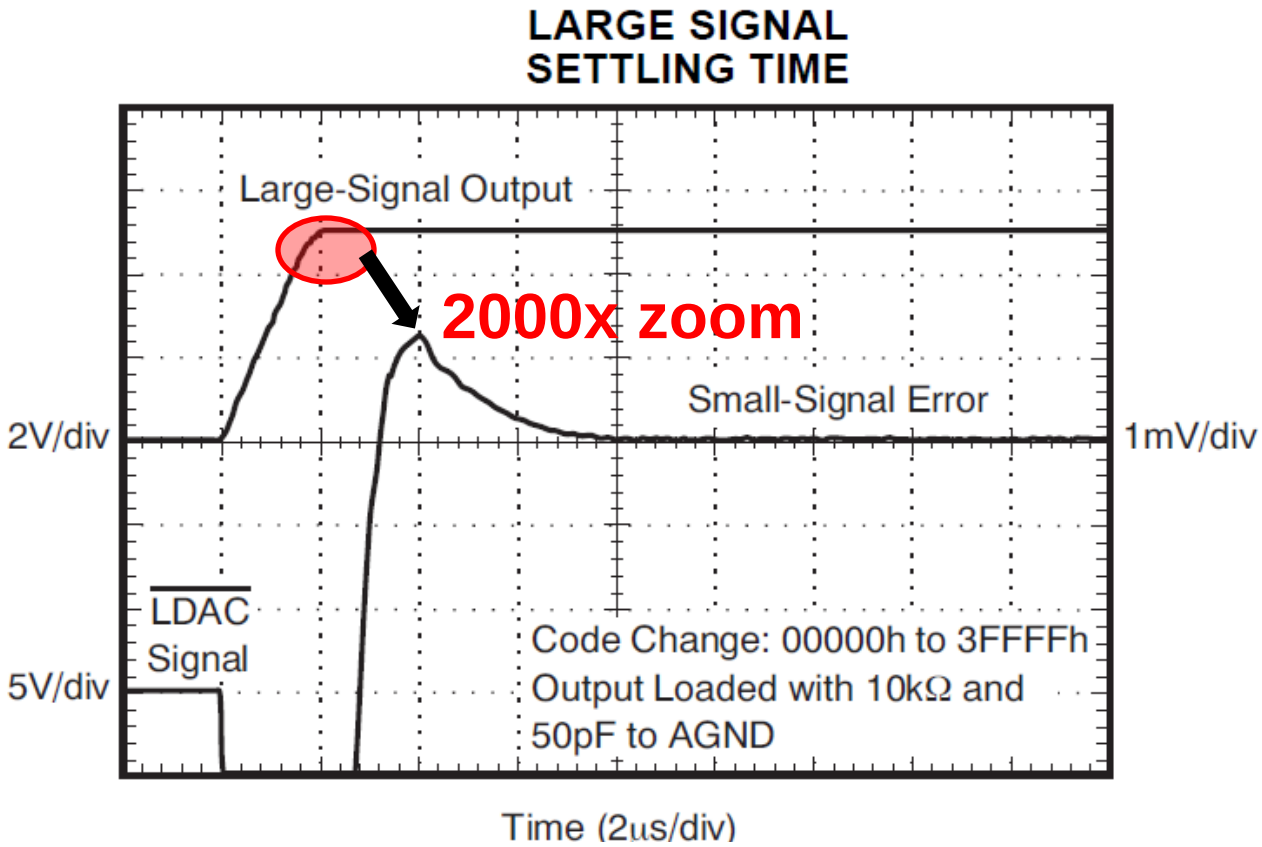
Settling Time



Settling Time in Real Devices



DYNAMIC PERFORMANCE[2]			
Settling time	To ±0.003% FS, R_L = 10kΩ, C_L = 50pF, code 04000h to 3C000h	5	µs

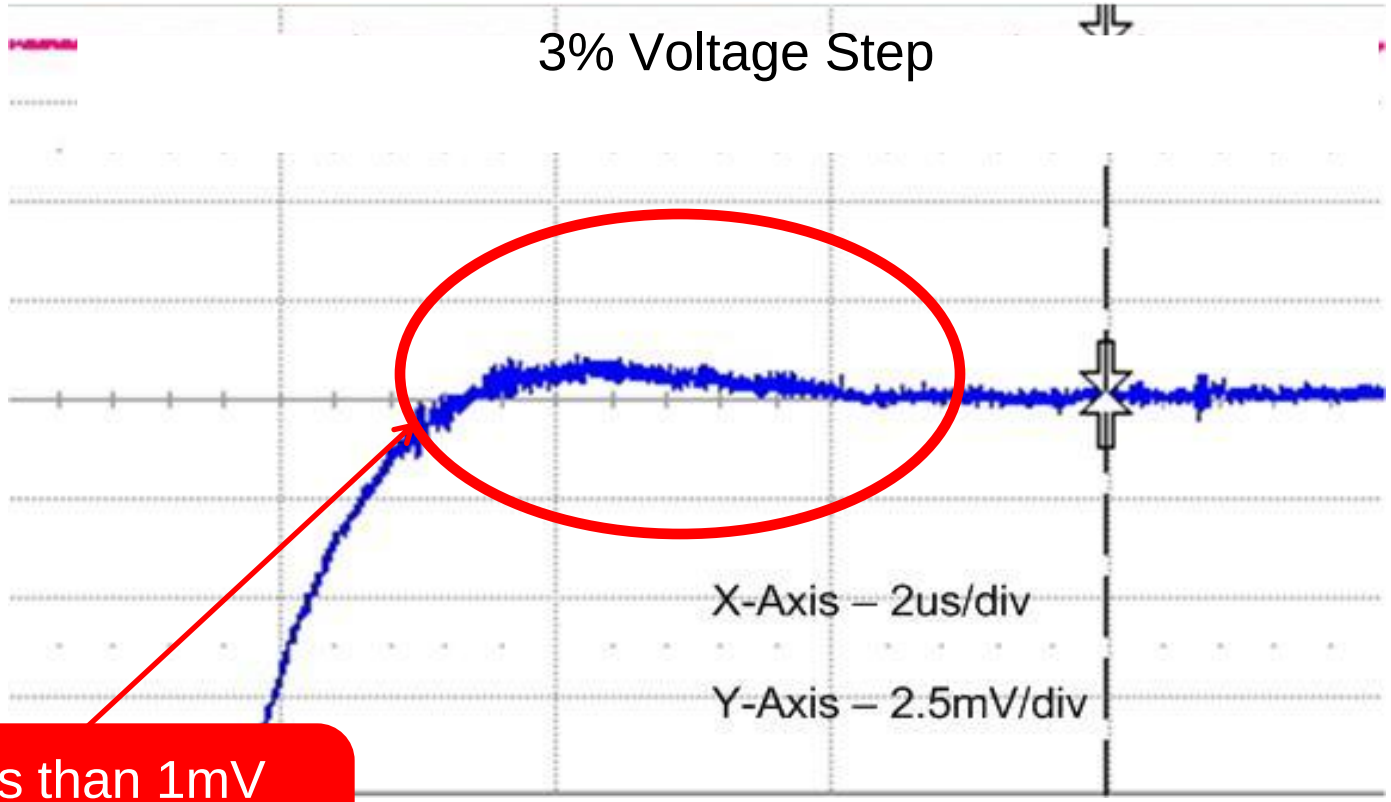
DAC9881

Settling Time in Real Devices

150mV Output Voltage Step

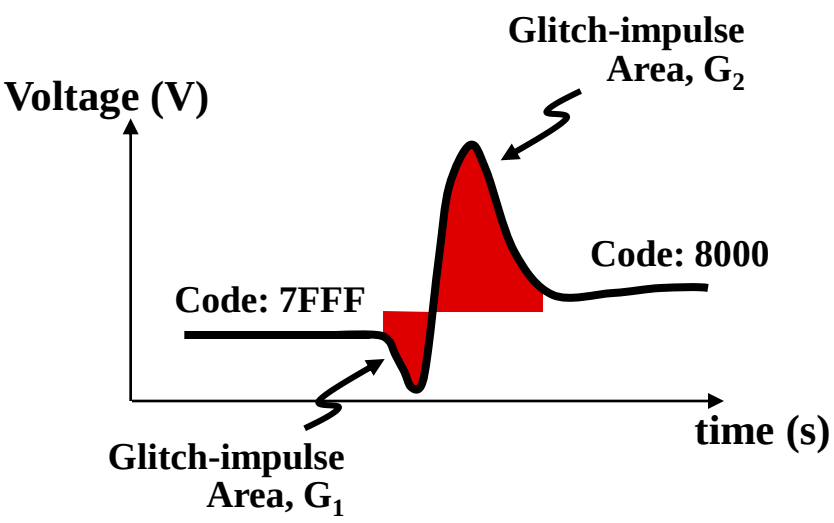
Code 0x02000 to 0x04000

3% Voltage Step



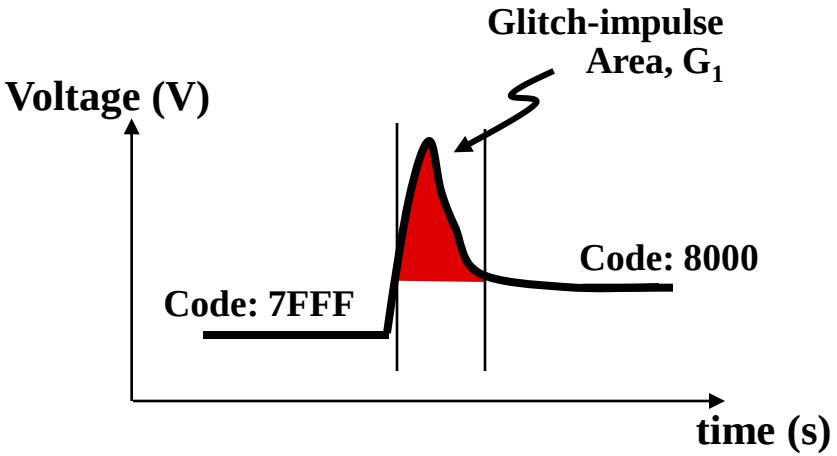
Less than 1mV amplitude

Glitch



Glitch-impulse = $G_2 - G_1$

a.) Two Lobe Glitch



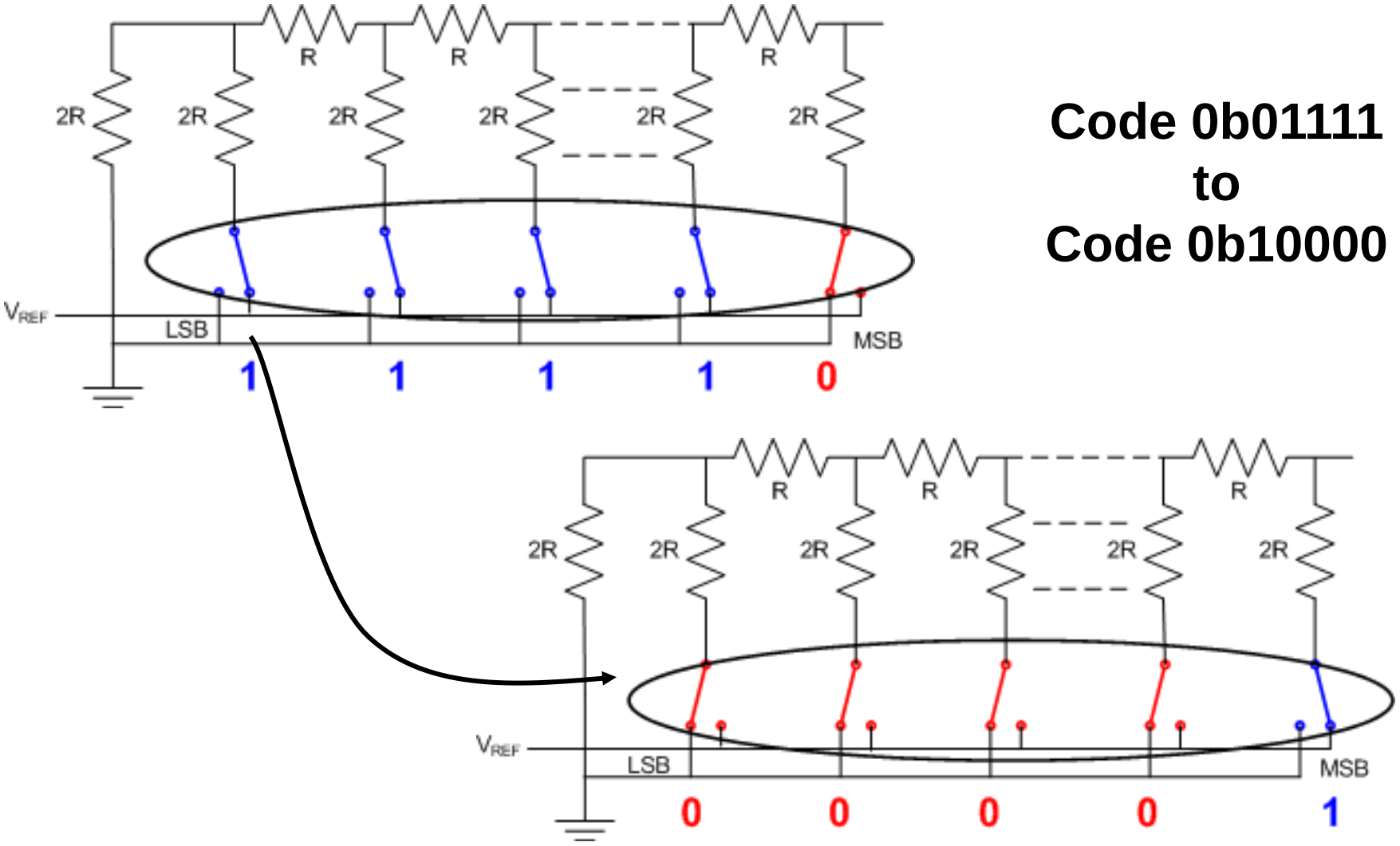
Glitch-impulse = G_1

b.) Single Lobe Glitch

Glitch Sources

- Two main sources
  - Switches switching!
    - When the switches transition the current has to take a new path
  - Switch synchronization
    - The switches will not be perfectly synchronized
- Major Carry Transition
  - Code changes that cause a majority of switches to transition in an R-2R or MDAC
  - This is the worst case possible
  - 0111 → 1000
  - 0100 → 1011

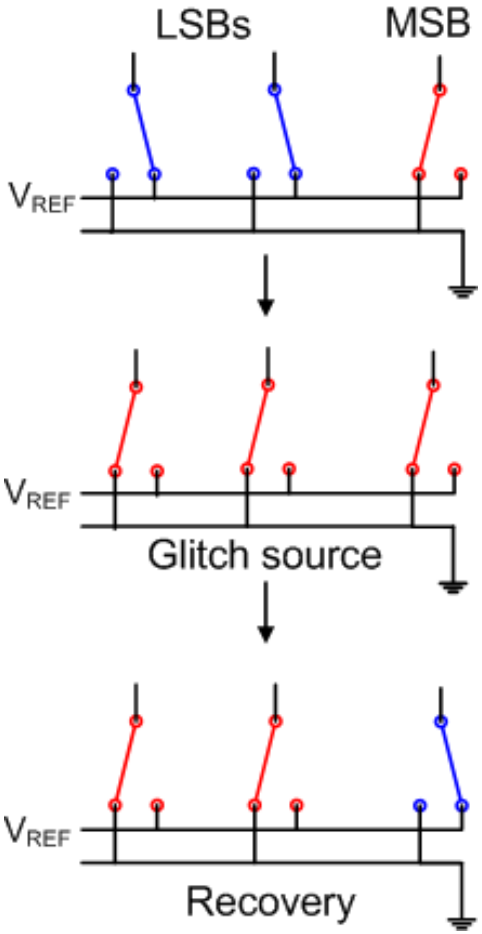
Major Carry Transition



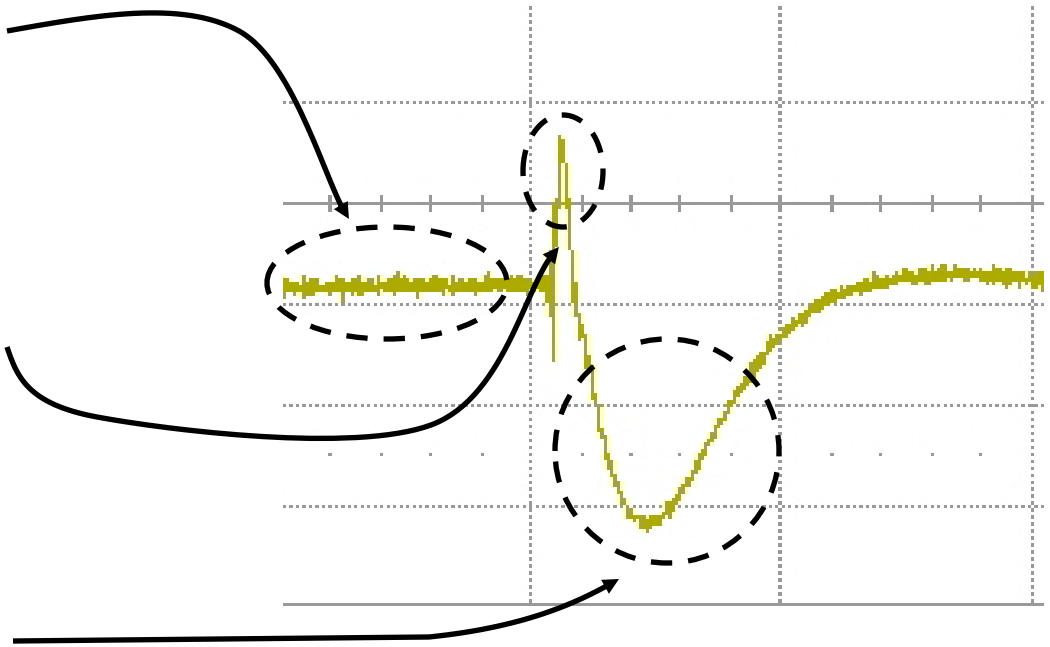
Code 0b01111
to
Code 0b10000

Major Carry Transition

R2R Structure



Output Voltage Glitch

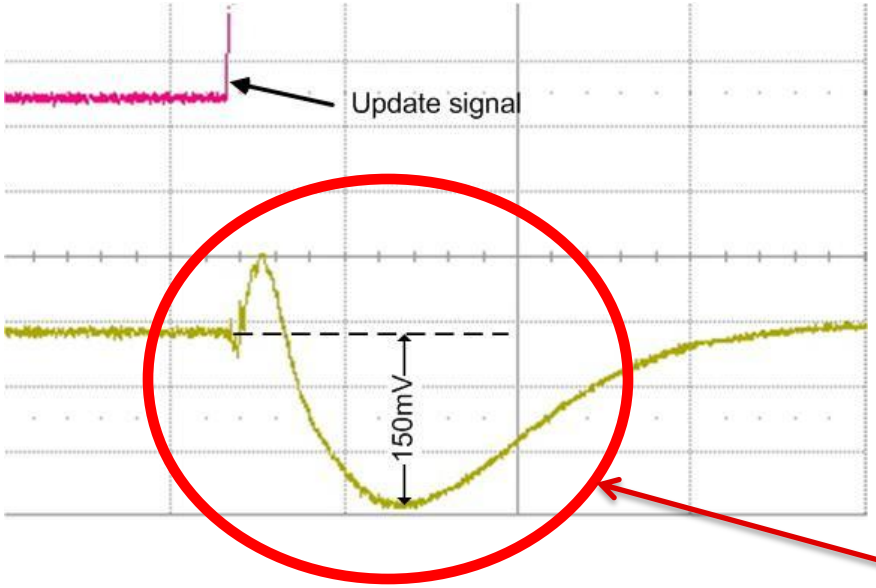


DAC Major Carry Transition

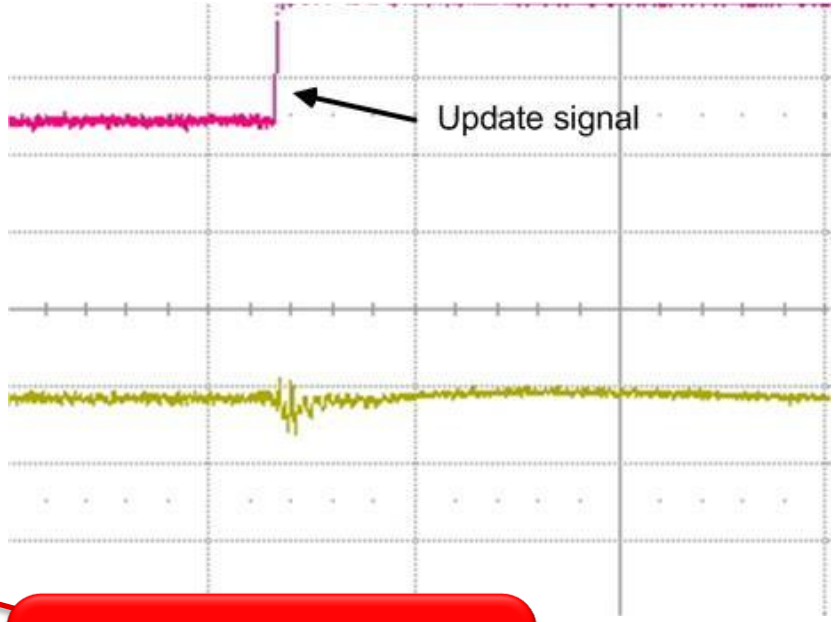
Code to Code Glitch

0x1FFFF to 0x20000

(major carry transition)



0x20000 to 0x20001

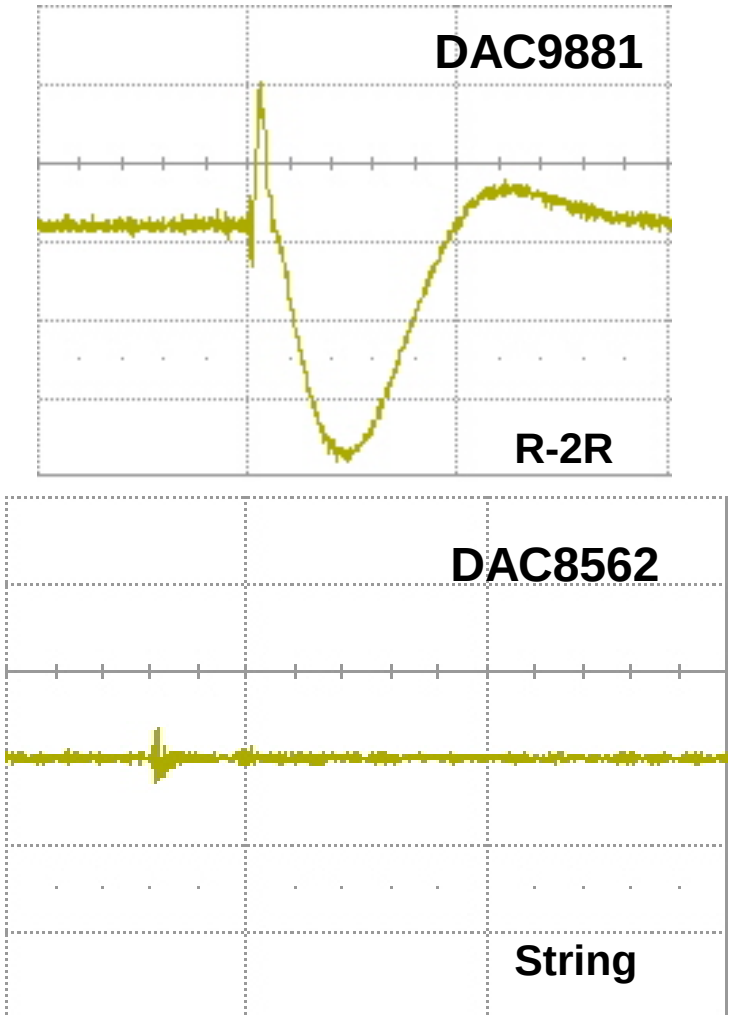


150mV amplitude glitch

Glitch vs. DAC structure

- R2R DAC – DAC9881
  - Simultaneous switching
  - Synchronization
  - Large glitch amplitude
  - Settling of Internal Amplifier
- String DAC – DAC8562
  - Simple switch network
  - Tap into resistor string
  - Single Lobe glitch
  - Small glitch amplitude

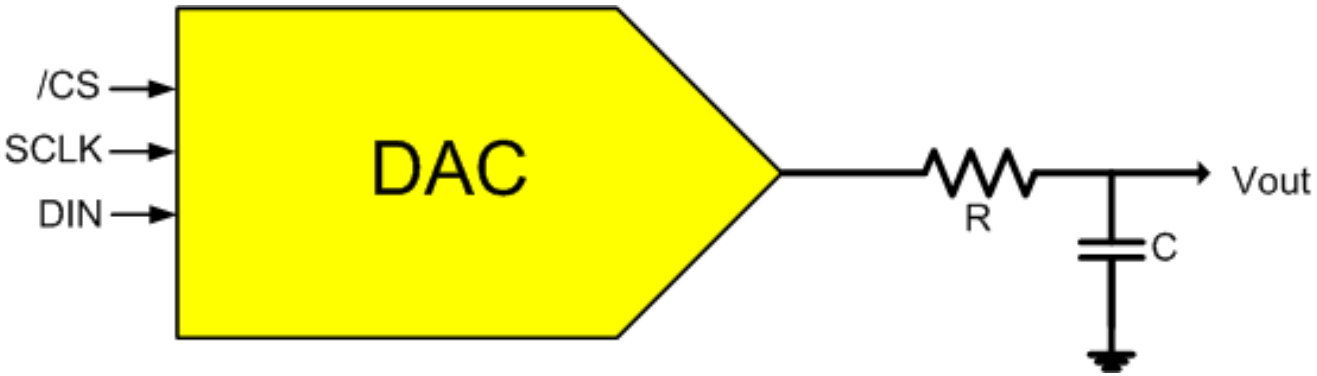
Graphs: 500ns/div 50mV/div



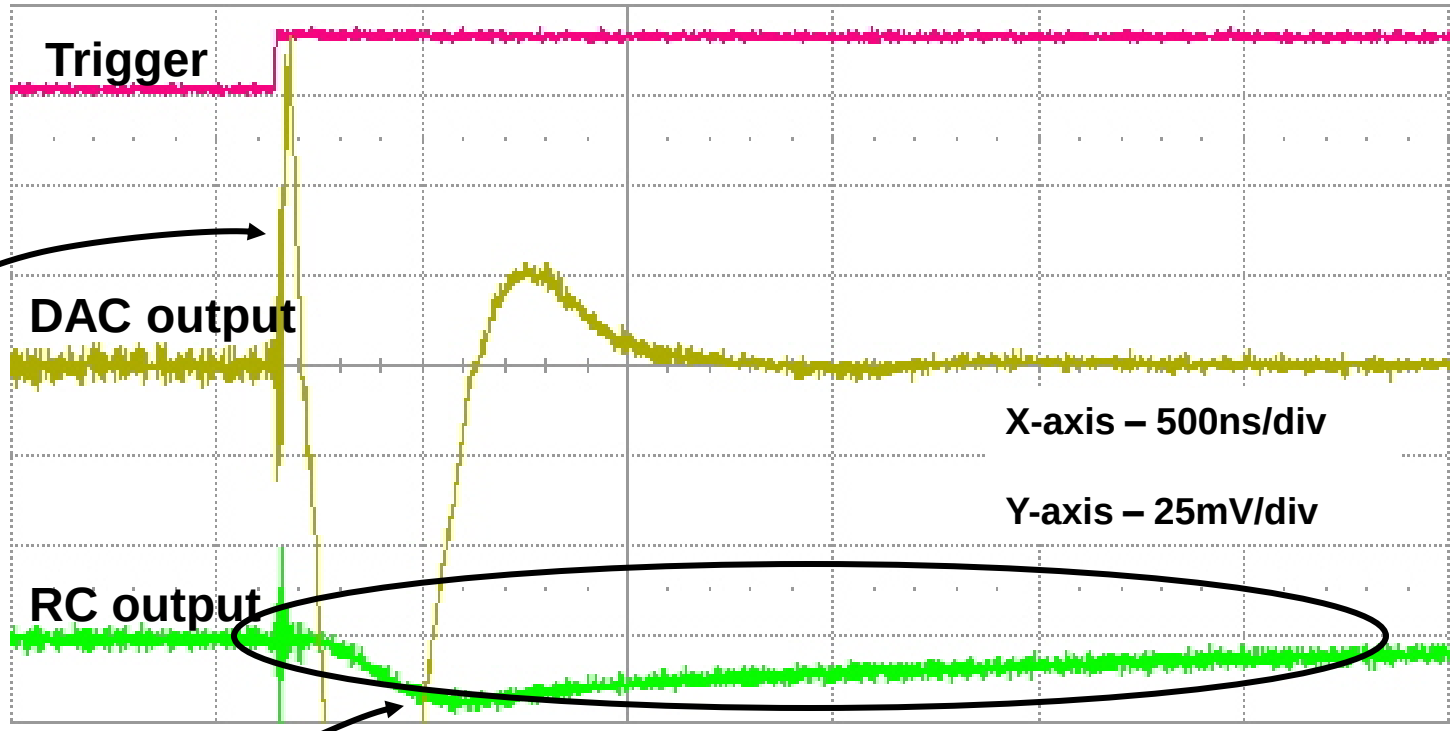
Glitch Reduction - RC Filter

- Attenuate glitch at cost of increased settling time
- Easy to implement
  - Cost effective
  - Uses minimal board space
- Voltage loss across resistor in network
  - Voltage dependent on output load
- RC value determined by period of the glitch
  - Period = 2πRC
  - Select 3dB point a decade prior to glitch

$$F_C = \frac{1}{2\pi RC}$$



Glitch Reduction - RC Filter cont.



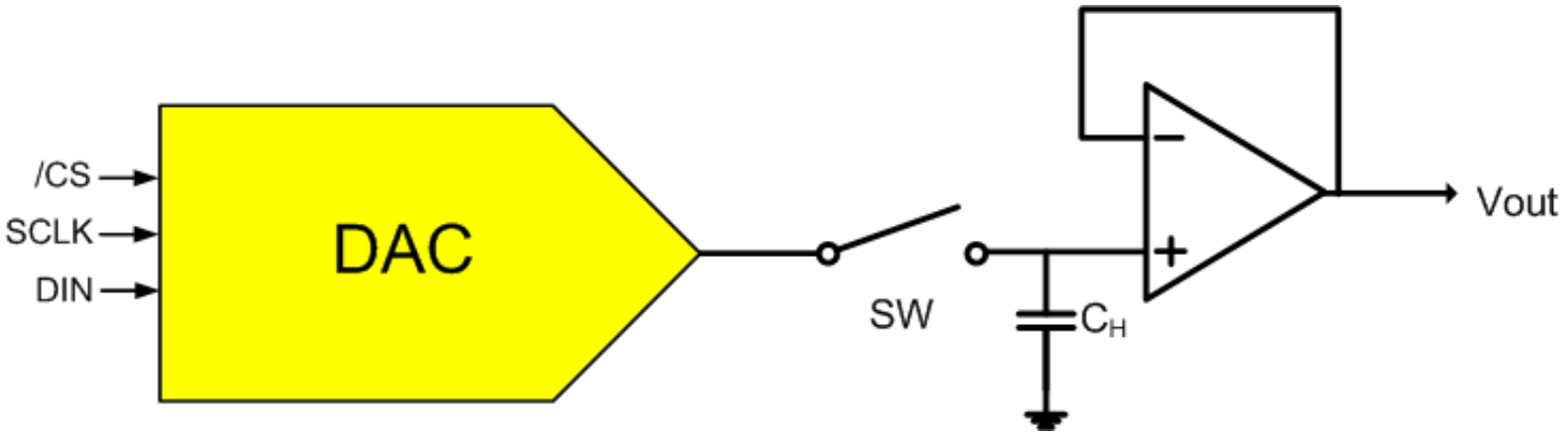
Texas Instruments DAC8881

Conditions: Vref = 5V, AVDD = 5V, Code transition 0x7FFF to 0x8000

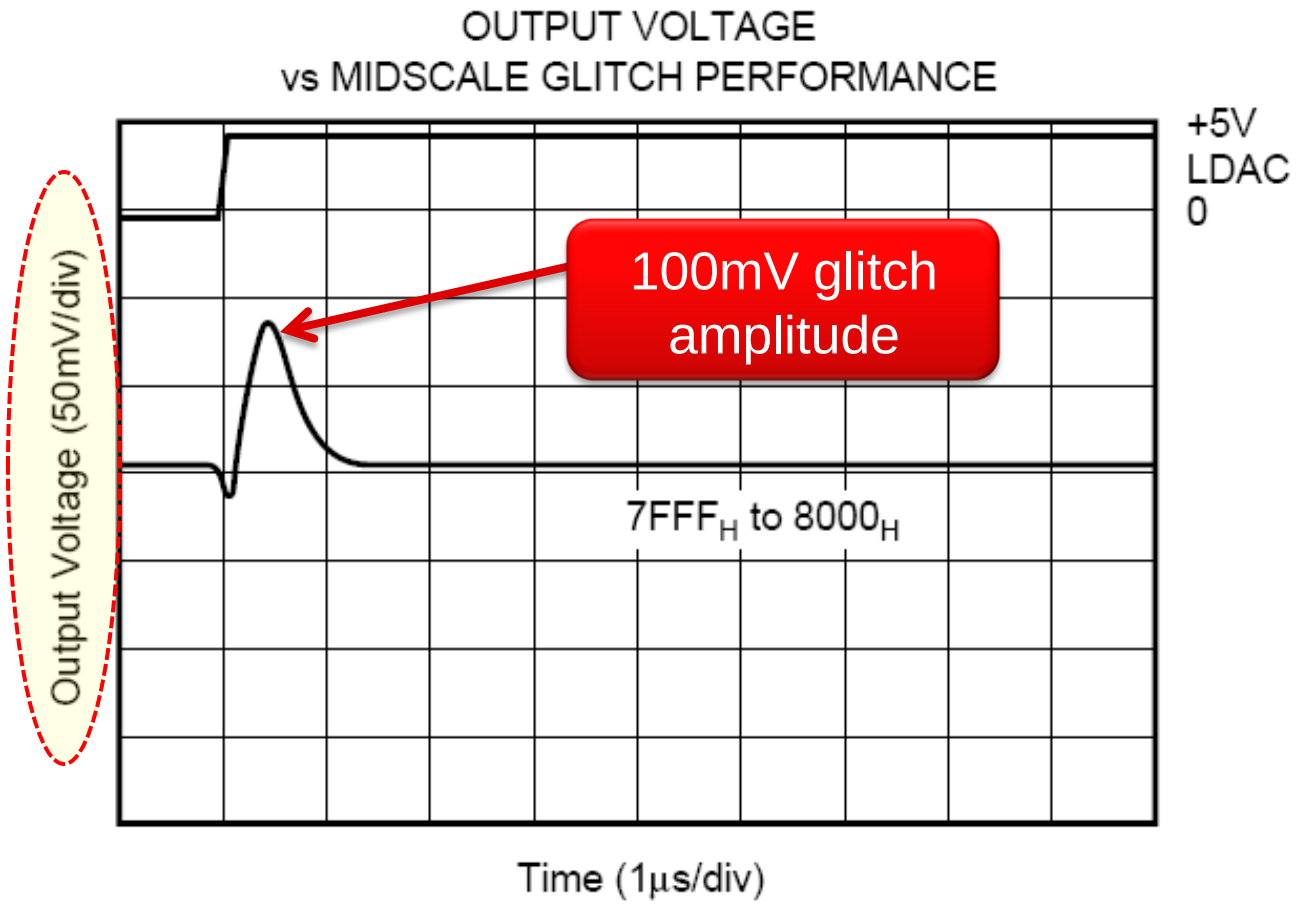
R = 20 ohm, C = 100nF

Glitch Reduction – Sample and Hold

- Eliminate Glitch from R2R ladder
  - No increase to settling time
  - Small transient from S/H switch
- Complex implementation - Strict timing
- Cost, board space, etc.

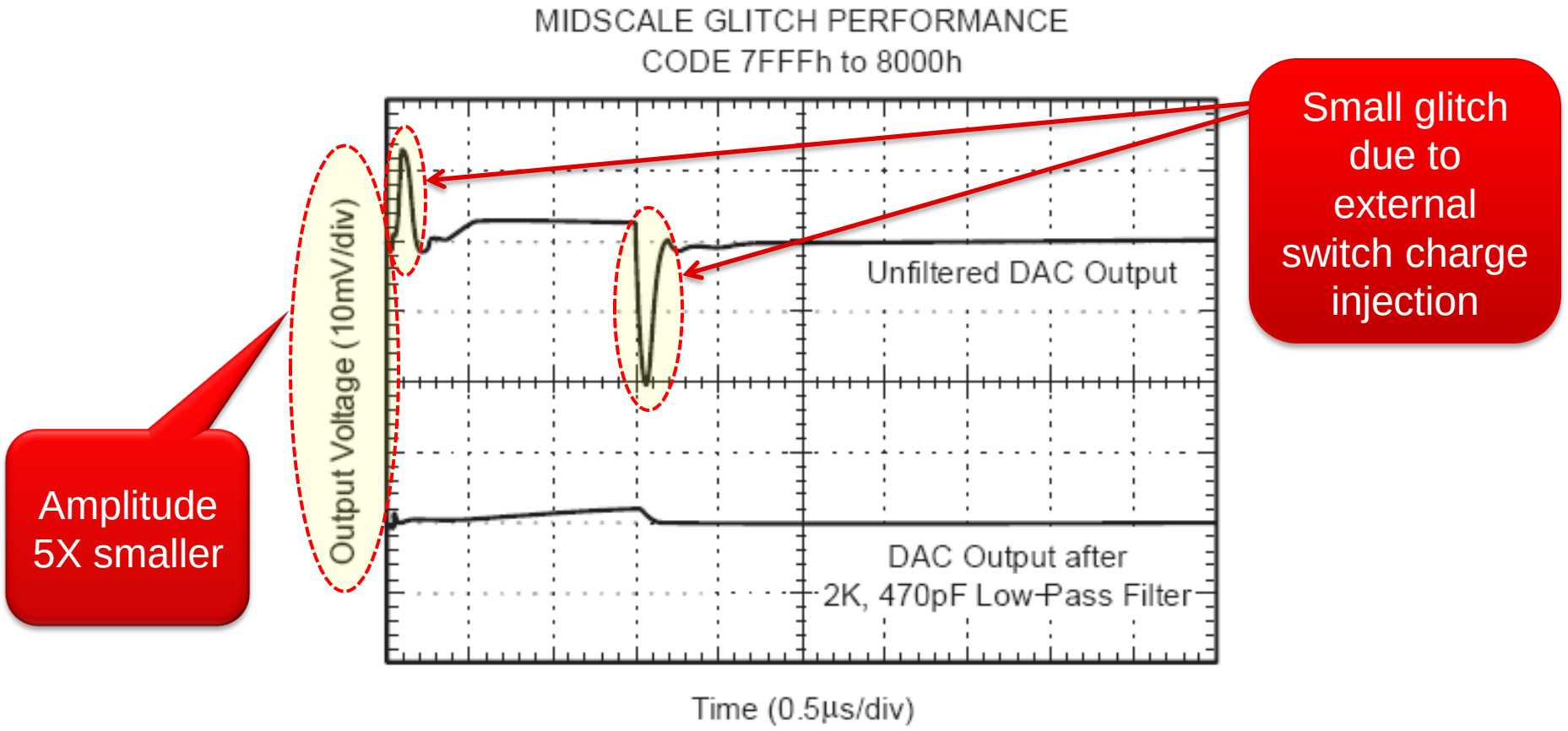


Glitch Reduction – S/H cap cont.



DAC7644 – without S/H amp

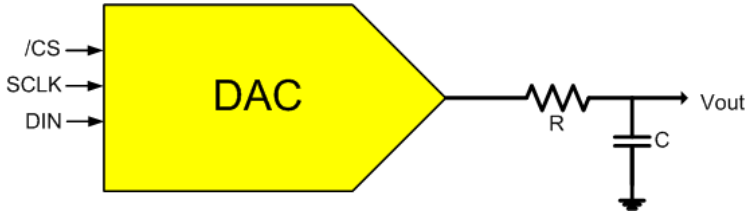
Glitch Reduction – S/H cap cont.

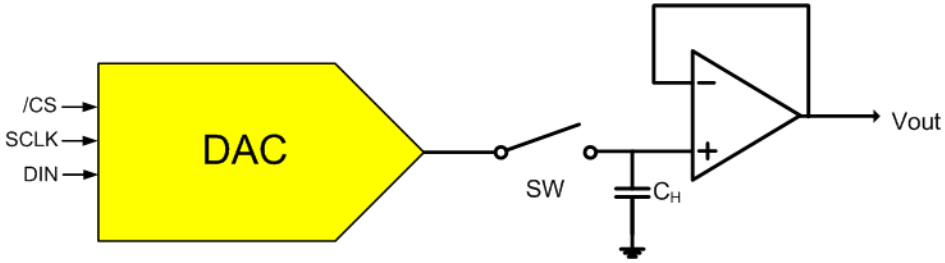


DAC7654 – Includes S/H amp

Glitch Reduction Techniques

- RC filter
  - Easy to implement
  - Not a complete removal of the glitch
  - Decrease glitch amplitude
  - Increased settling time
- Switch cap solution
  - Completely remove glitch
  - Strict timing
  - Difficult to implement
  - Slower update rates

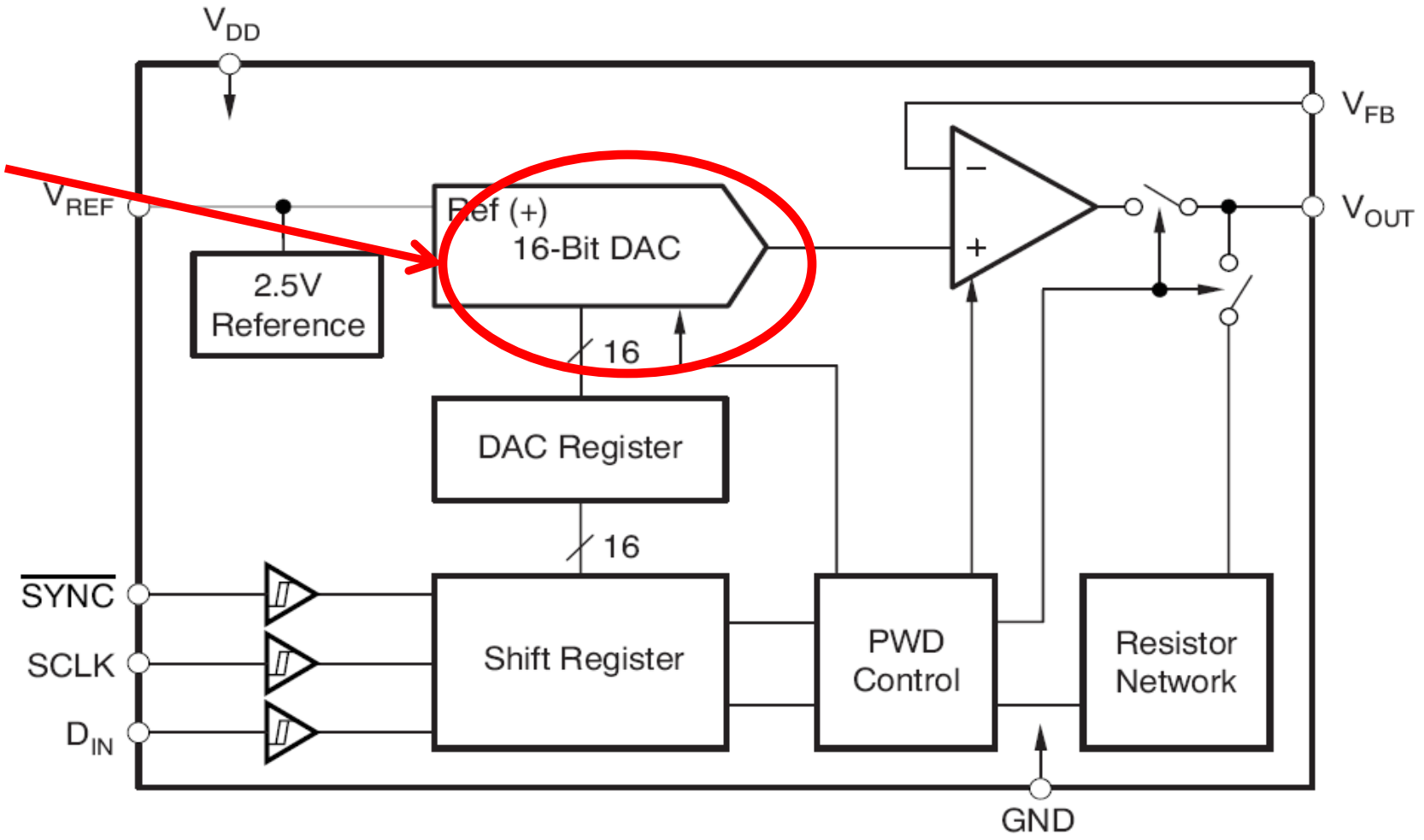




DAC Output Noise sources

- Internal resistor string
- Output amplifier
- Reference voltage

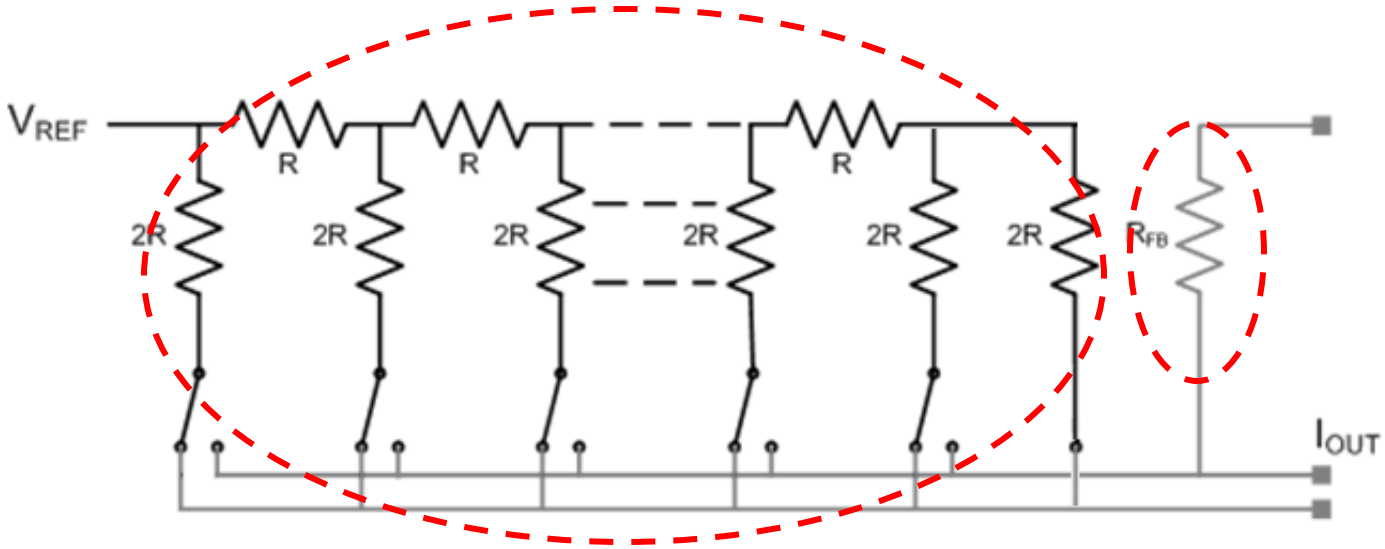
Internal Resistor String Noise



Internal Resistor String Noise

$$e_n = \sqrt{4 \times K \times T \times R \times B}$$

- Thermal Resistor noise
  - K = Boltzman constant = 1.3806503e-23
  - T = Temperature = 300 deg K for room temperature
  - R = Equivalent Resistance of Resistor String
  - B = Normalized Bandwidth = 1 Hz



Resistor Noise

Verification using DAC8801 current output DAC

- Simple R2R resistor string
- No Internal Op amp
- Full scale equivalent resistance = 5K

Does not include feedback resistor

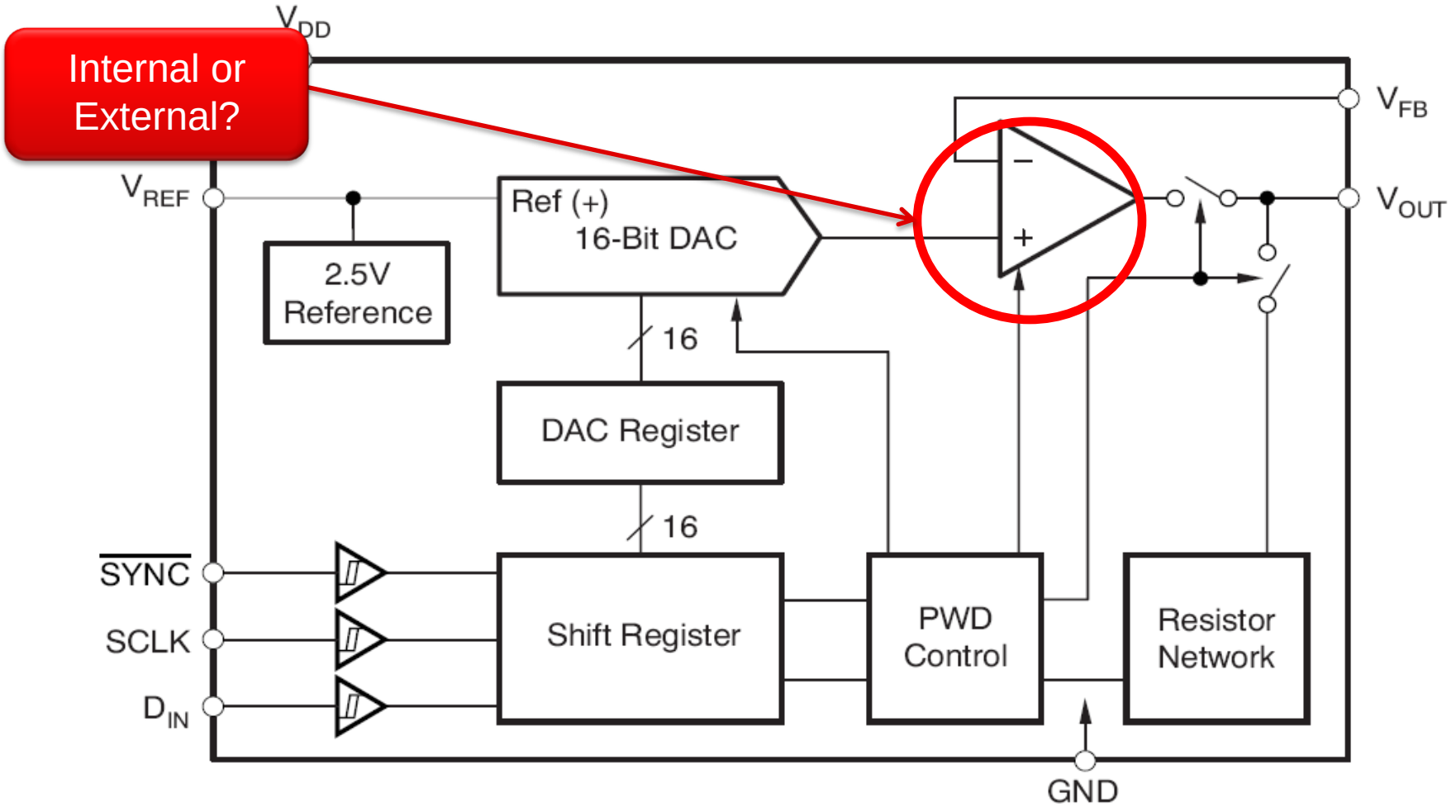
$$e_n = \sqrt{4 \bullet 1.38e-23 \bullet 300 \bullet 5000 \bullet 1} = 9.1 \frac{nV}{\sqrt{Hz}}$$

$$\sqrt{2 \bullet e_n^{\,2}} = \sqrt{9.1^2 + 9.1^2} = 12.87 \frac{nV}{\sqrt{Hz}}$$

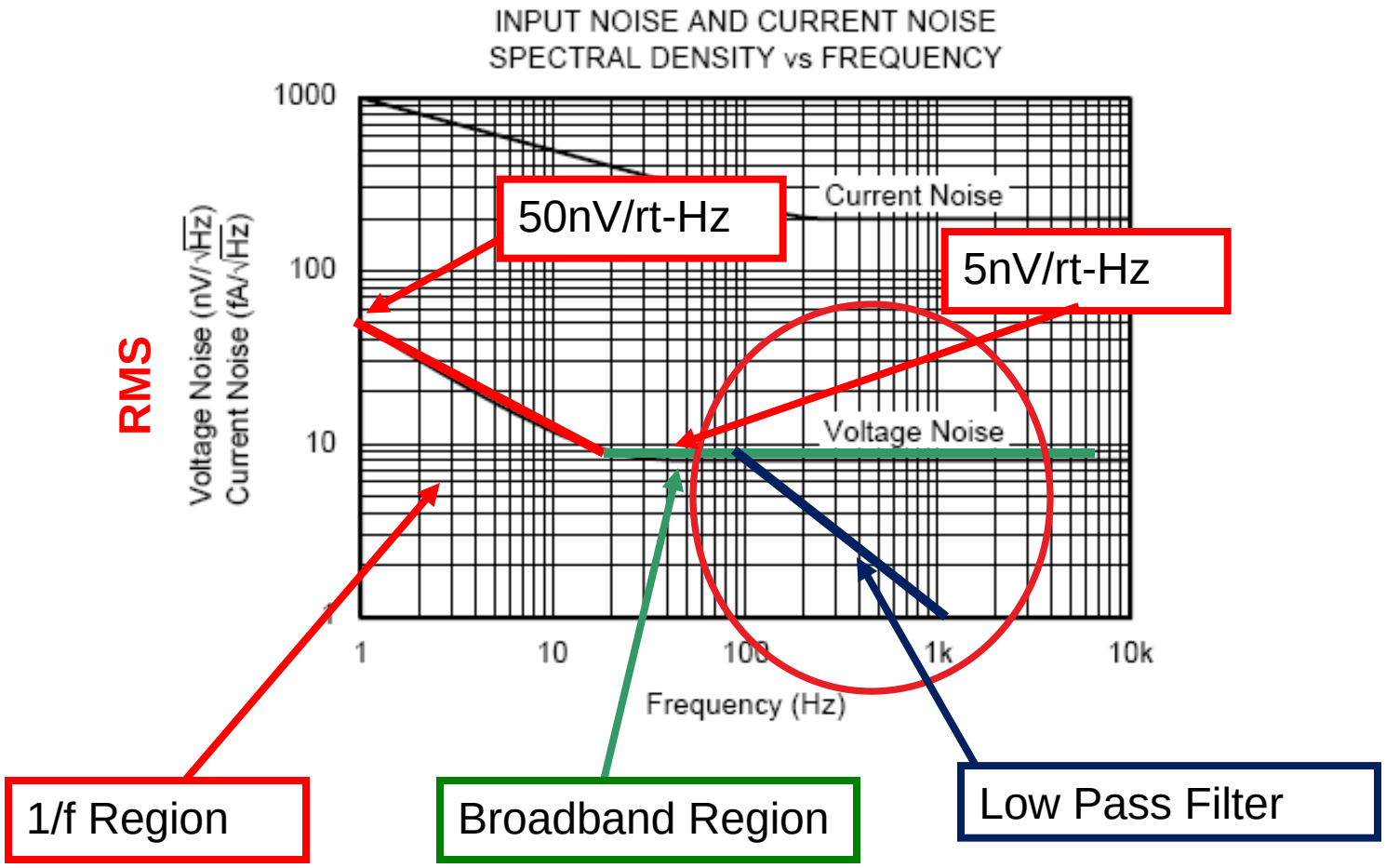
Use Sum squared to account for feedback resistor

PARAMETER	CONDITIONS	DAC8801			UNITS
		MIN	TYP	MAX	
Total harmonic distortion	V_{REF} = 5 V_{PP}, Data = 3FFFh, f = 1 kHz		–105		dB
Output spot noise voltage	f = 1 kHz, BW = 1 Hz		12		nV/√Hz

DAC Amplifier Output Noise



DAC Amplifier Output Noise



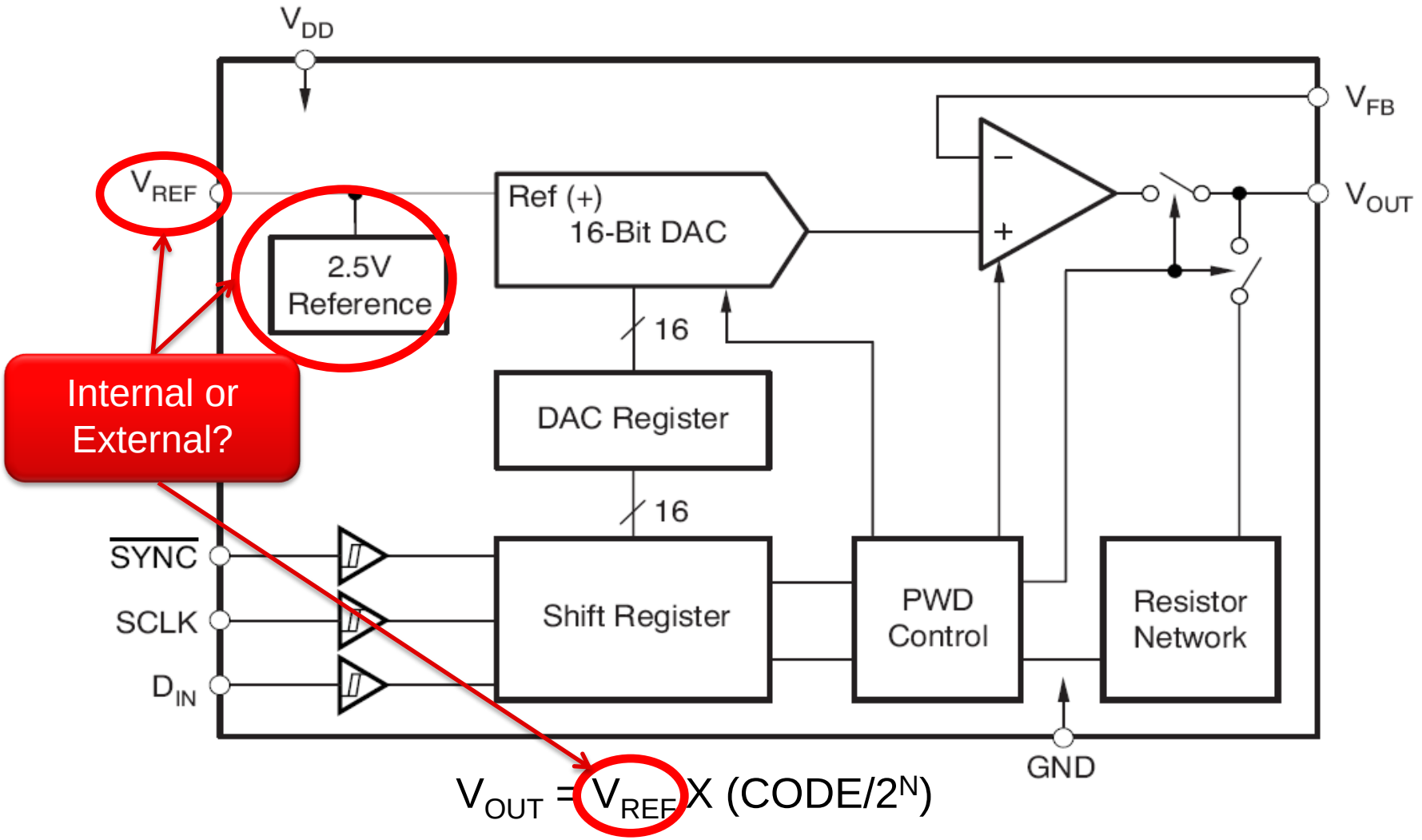
Source: Art Kay, Op Amp Noise 2006

Output Amplifier Noise

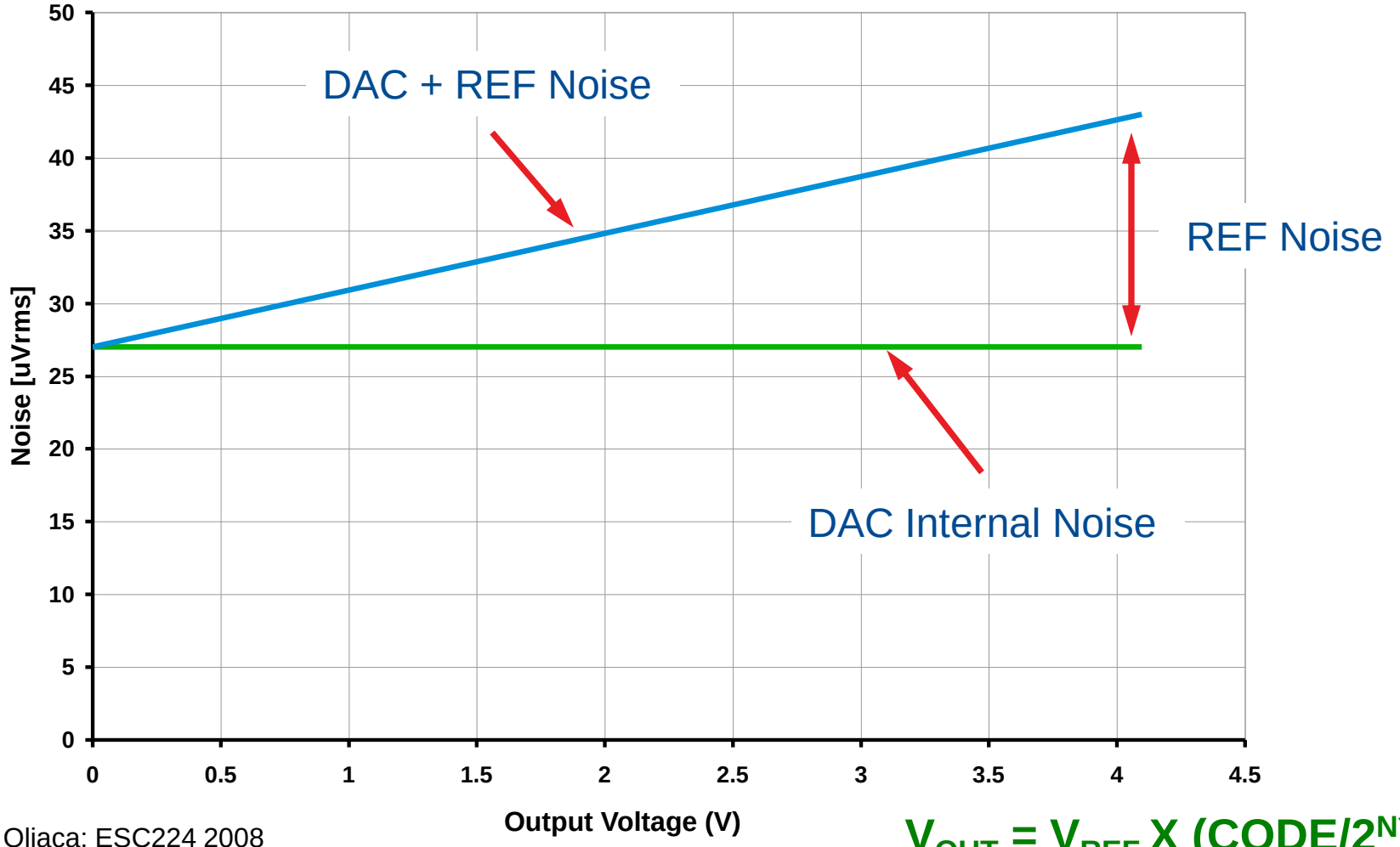
- For external output amplifiers, follow Art Kay's noise presentation for complete noise analysis
  - In general, search for amplifiers with low 1/f noise
- For the internal case, a typical DAC datasheet does a lot of this work for you
  - Usually a number provided in the electrical characteristics table
  - Sometimes a figure to illustrate the noise spectrum

AC PERFORMANCE[2]			
DAC output noise density	T_A = 25°C, at mid-scale input, f_{OUT} = 1 kHz	90	nV/√Hz
DAC output noise	T_A = 25°C, at mid-scale input, 0.1 Hz to 10 Hz	2.6	μV_{PP}

Voltage Reference Selection



Noise Contribution



Source: Miro Oljaca; ESC224 2008

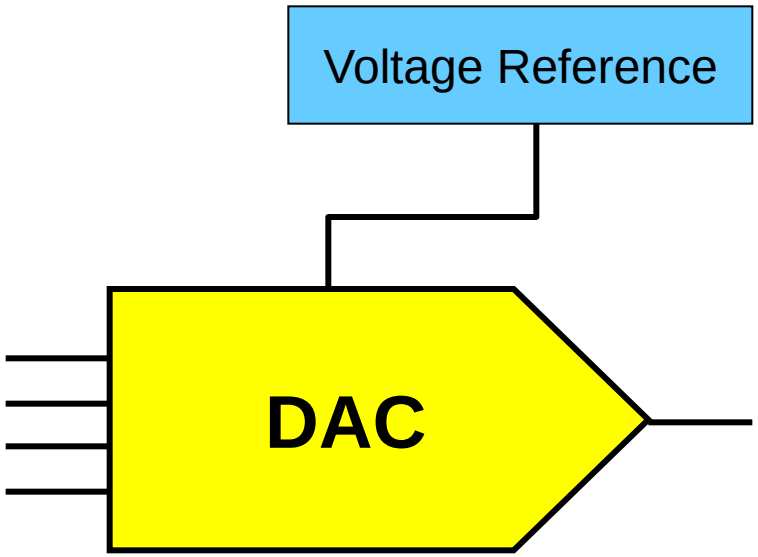
$V_{OUT} = V_{REF} X (CODE/2^N)$

Internal vs. External Voltage References

Device	Initial Accuracy (%)		Tmp. Coef. (ppm/C)		Total Accuracy (%)
	Max	Typ	Max	Typ	Max
MSP430F167	+/-4	---	+/-100	---	+/-4.60
TLV5638	+/-4	---	---	---	---
DAC7678	+/-0.2	+/-5	+/-25	+/-0.23	+/-0.35
DAC8562	+/-0.2	+/-4	+/-10	+/-0.22	+/-0.26
DAC8564/8	+/-0.1	+/-2	+/-5	+/-0.11	+/-0.13
REF30xx	+/-0.2	+/-20	+/-50	+/-0.32	+/-0.50
REF31xx	+/-0.2	+/-10	+/-20	+/-0.26	+/-0.32
REF32xx	+/-0.2	+/-4.0	+/-7.0	+/-0.22	+/-0.24
REF33xx	+/-0.15	+/-30	+/-30	+/-0.33	+/-0.33
REF50xx	+/-0.05	+/-2.5	+/-3.0	+/-0.07	+/-0.09

Voltage Reference Selection

- Design issues to consider
  - Noise
  - Initial Accuracy
  - Power Consumption
  - Source and Sink Current Capability
  - Temperature Drift
  - Long Term Stability



Basic Selection Criteria

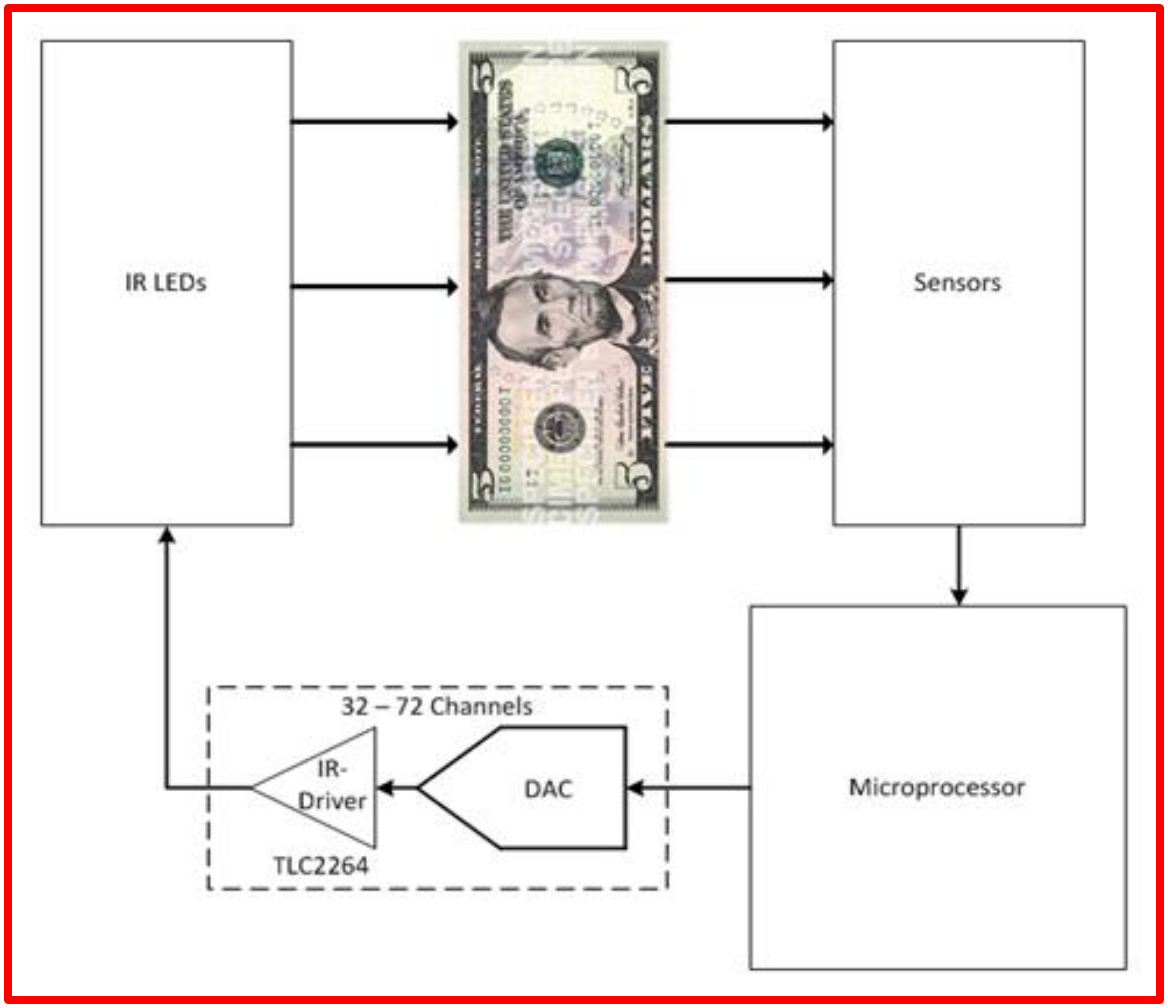
- Primary Criteria[1]
  - Resolution
  - Channels
  - Interface
  - Current/Voltage Output
  - Settling Time
  - DNL, INL, Offset, Gain Errors
  - Output Voltage Range
  - Power
  - Package
- Secondary Criteria [2]
  - Reset to mid-scale/zero scale
  - Supply Range
  - Operating Temp Range
  - Integrated Reference (reference drift, accuracy, drive capability)
  - Glitch Energy
  - Integrated Amplifiers/Multiplying DACs

Conclusion

- What does your Application look like?
- Leverage architectural tendencies to narrow the DACs under consideration
- Understand how specifications are measured, what they mean, and how to apply them into application specific circumstances

Precision DAC Applications

Application#1 – ATM, Currency Counters Automated fair collectors

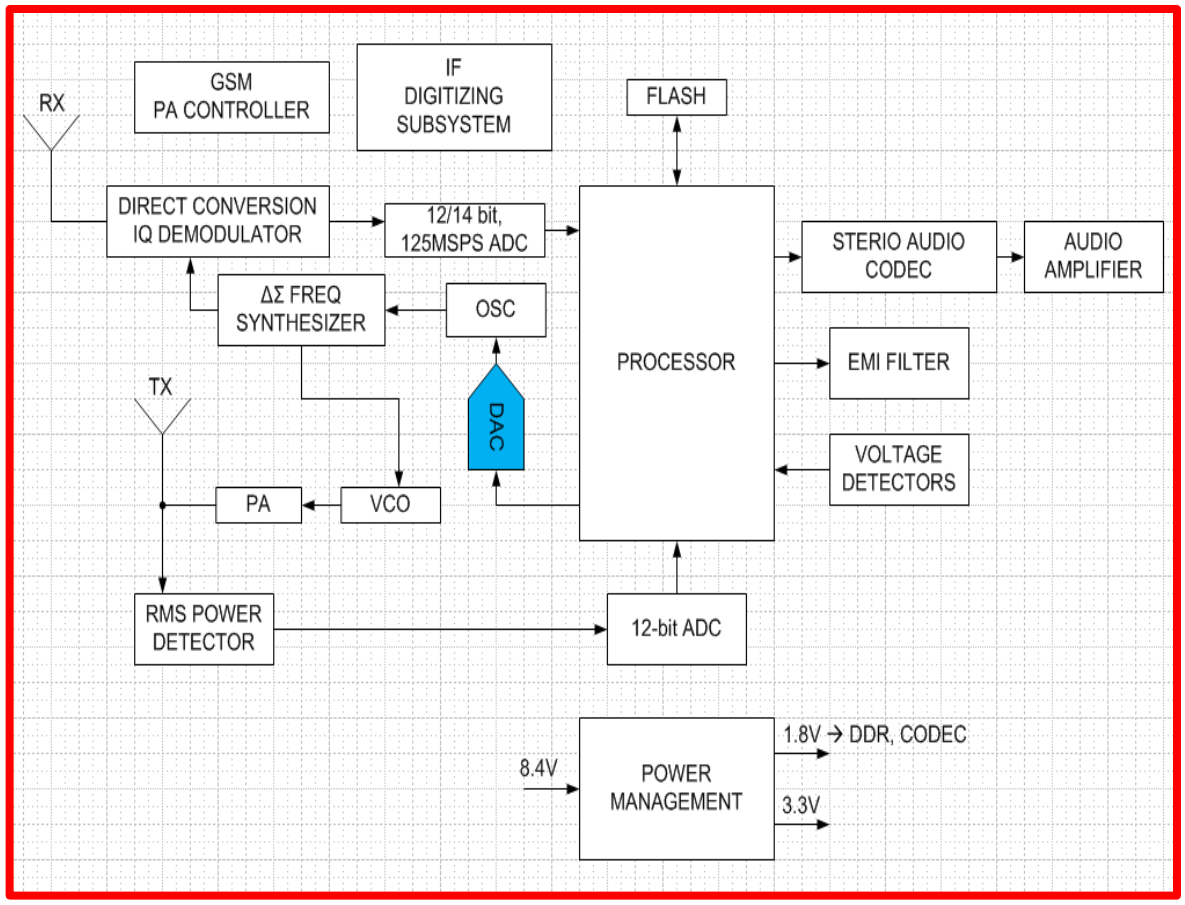


IR LED Driver

- ✓ DAC Key Care about
  - ✓ 8-12-bit
  - ✓ Multichannel
  - ✓ Low cost, I2C

Architecture → String

Application#2 – Digital Walkie-Talkie

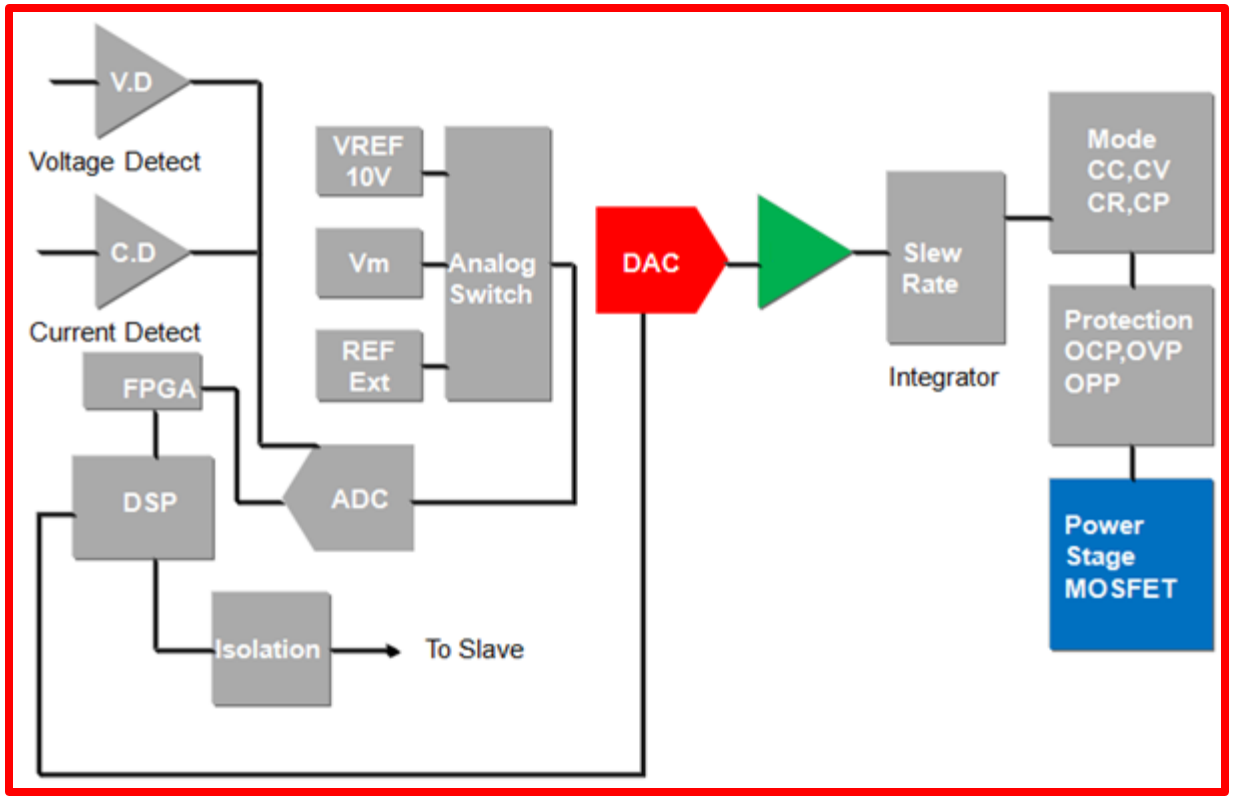


- Automatic Power Control
- PA Bias Control
- TCXO Bias (PLL Ref Clock)

- ✓ DAC Key Care about
  - ✓ 12-bit accuracy
  - ✓ Multichannel
  - ✓ Low power, area

Architecture → String

Application#3 – Power Supply Testing DC Load

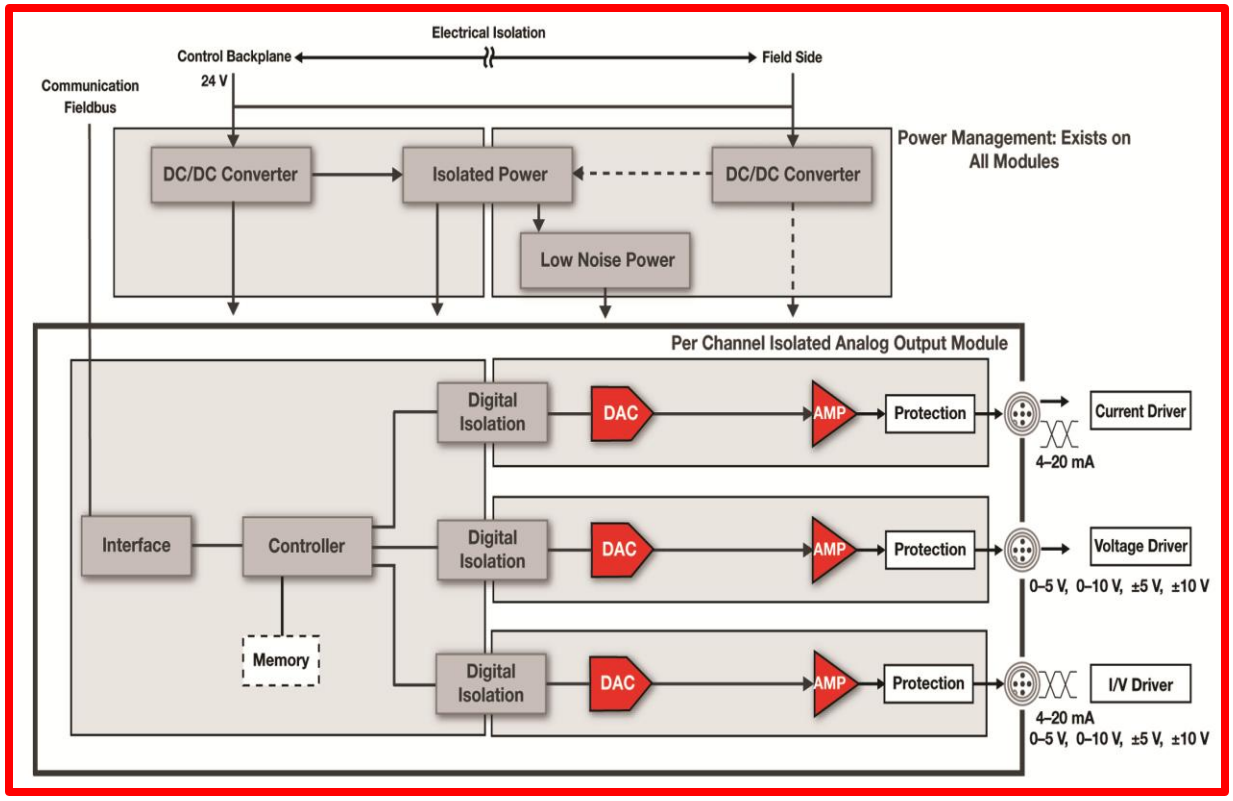


Power MOS gate control

- ✓ DAC Key Care about
  - ✓ 16-bit
  - ✓ Fast settling <1usec
  - ✓ INL<2LSB

Architecture → MDAC

Application#4 – High End Analog Output Modules

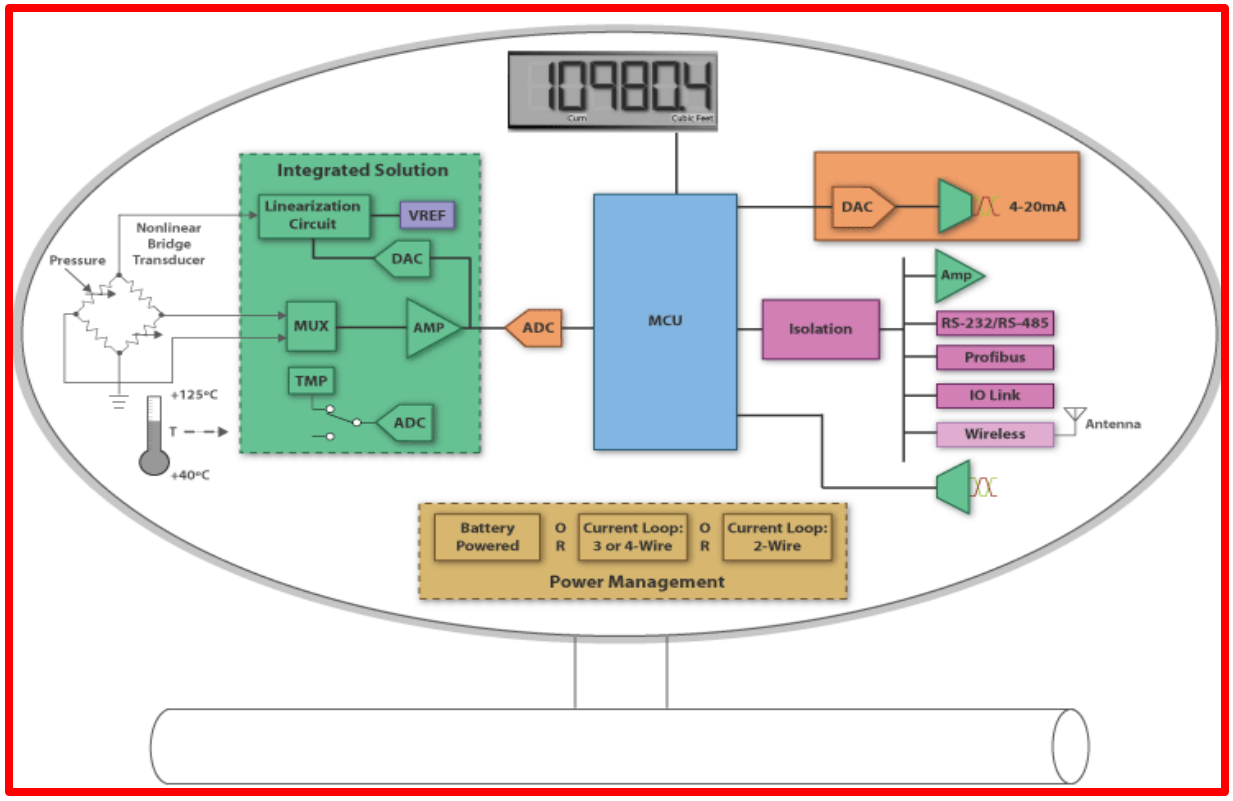


Create V/I Outputs

- ✓ DAC Key Care about
  - ✓ 16-bit
  - ✓ Single/Dual/Quads
  - ✓ <0.05% Total Error

Architecture → R2R, High performance string

Application#5 – Pressure Sensors

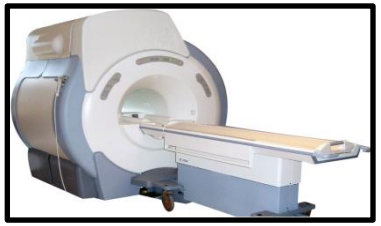


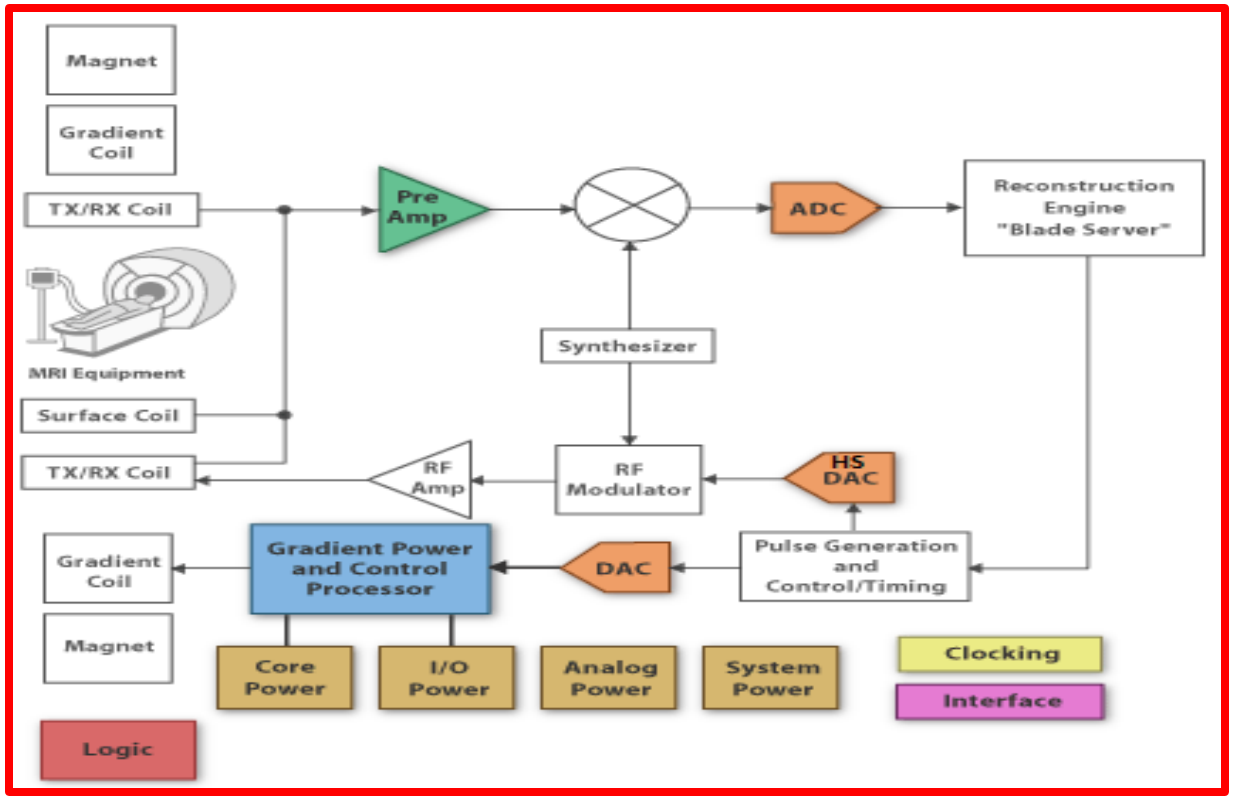
Create 4-20mA current

- ✓ DAC Key Care about
  - ✓ 16-bit
  - ✓ <0.05% Total error
  - ✓ Low Power

Architecture → High performance string

Application#6 – MRI Machines



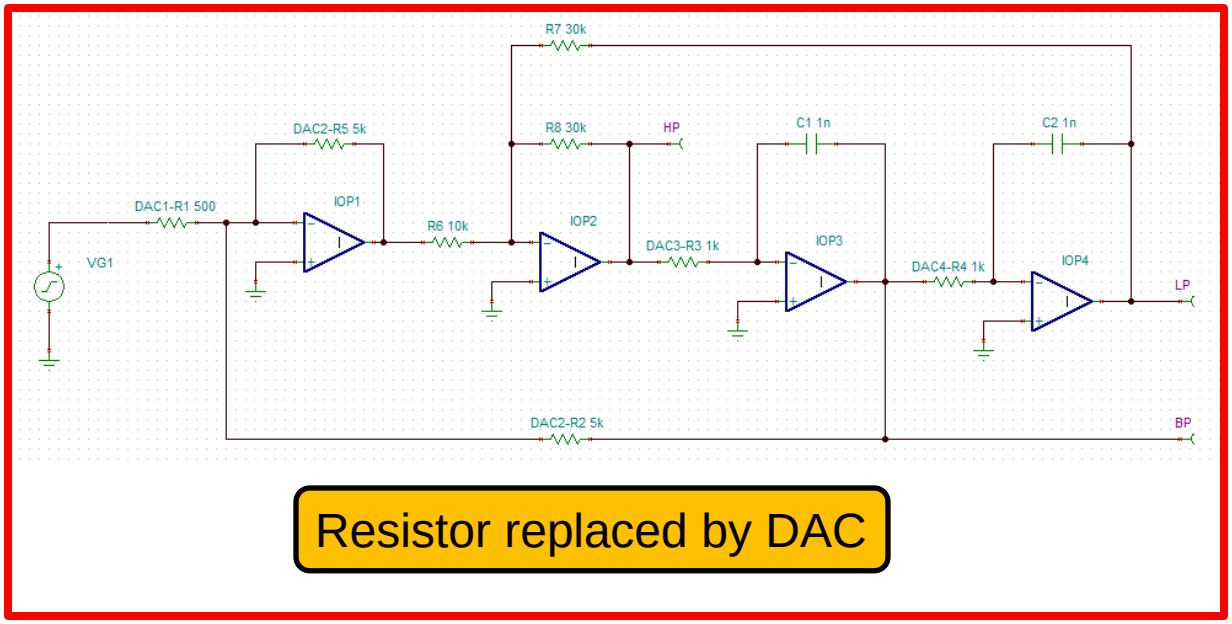


Control Coil gradient

- ✓ DAC Key Care about
  - ✓ ≥16-bit
  - ✓ High Accuracy, speed
  - ✓ ≤1LSB-INL

Architecture → MDACs, Unbuffered R2R

Application#7 – Tunable State Variable Filter



Resistor replaced by DAC

- ω (Frequency) Control
- Q (Quality Factor) Control
- A_v (Gain) Control

- ✓ DAC Key Care about
  - ✓ 8-bit, Multichannel
  - ✓ Tunable resistor
  - ✓ Matching

Architecture → MDACs, Unbuffered R2R

Application#7 – Tunable State Variable Filter