

ADC0xD1520RB Reference Board

REFERENCE DESIGN

SPECIAL NOTES

These schematics reflect the current state of product development. This design had NOT yet been fully tested at the time these schematics were generated.

Since this product is in development, the user of this document is strongly advised to check for the latest revision.

Texas Instruments reserves the right to make changes to this product.

ALL parts labeled "NA" are NOT ASSEMBLED.


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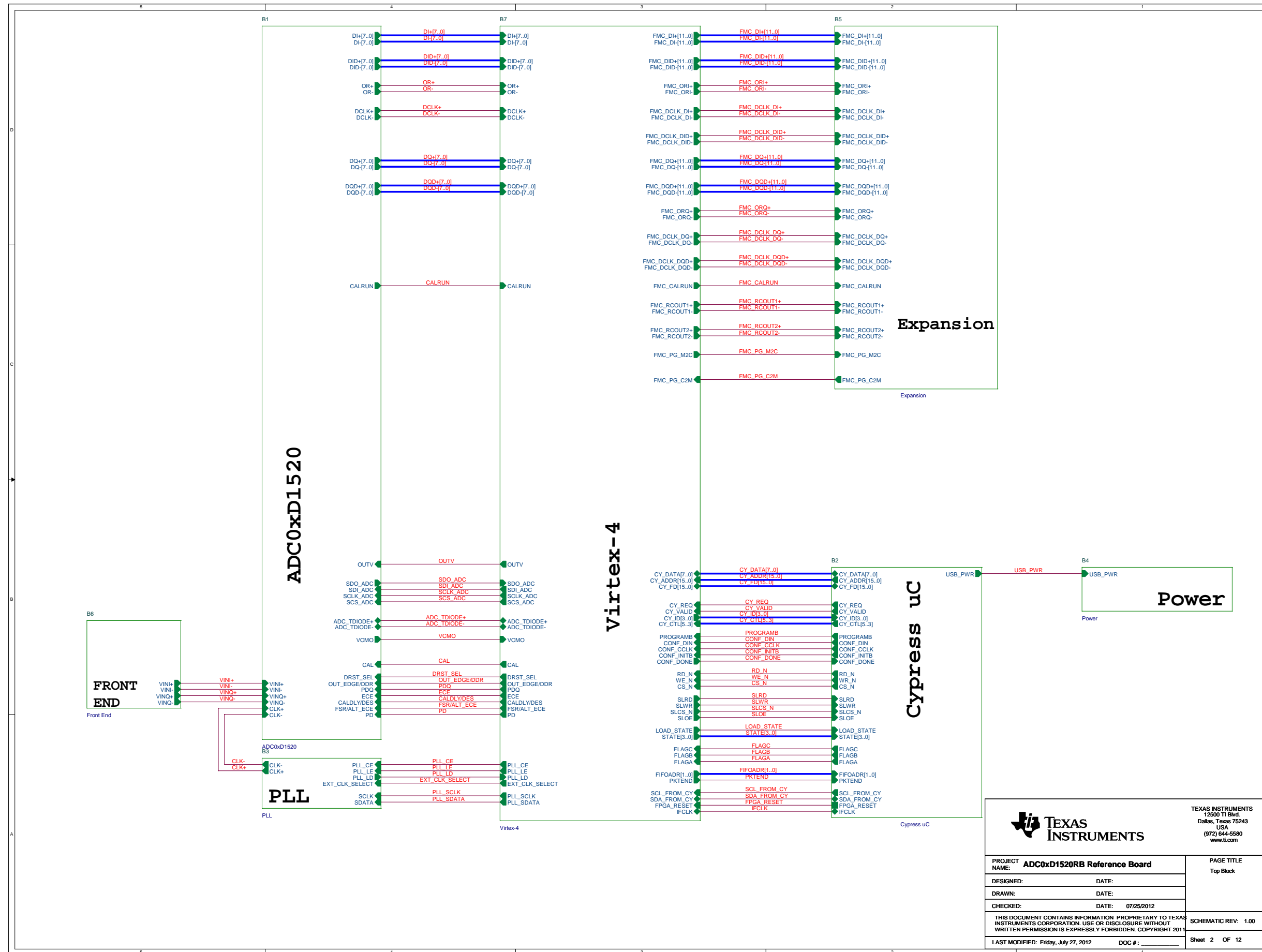
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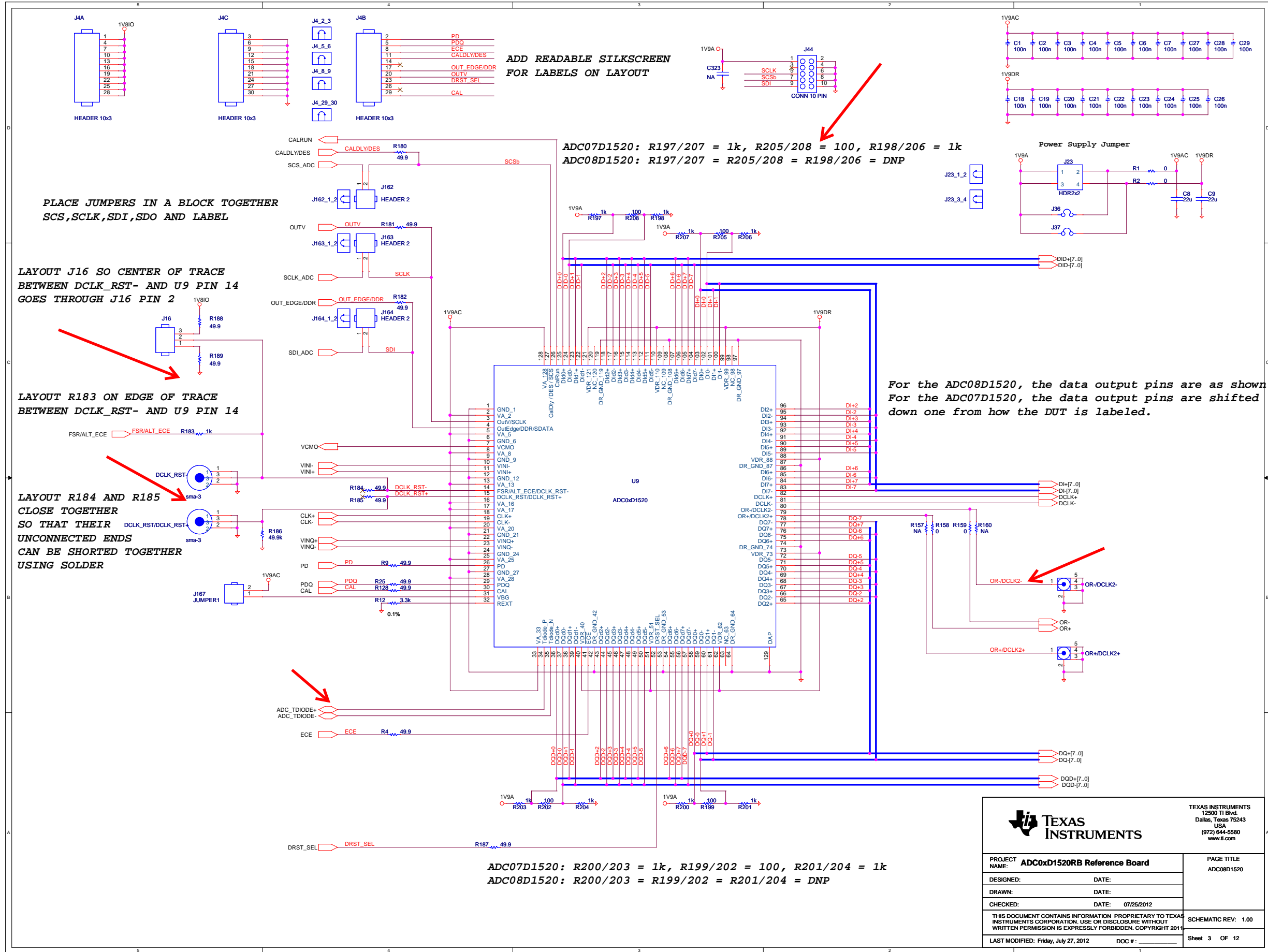
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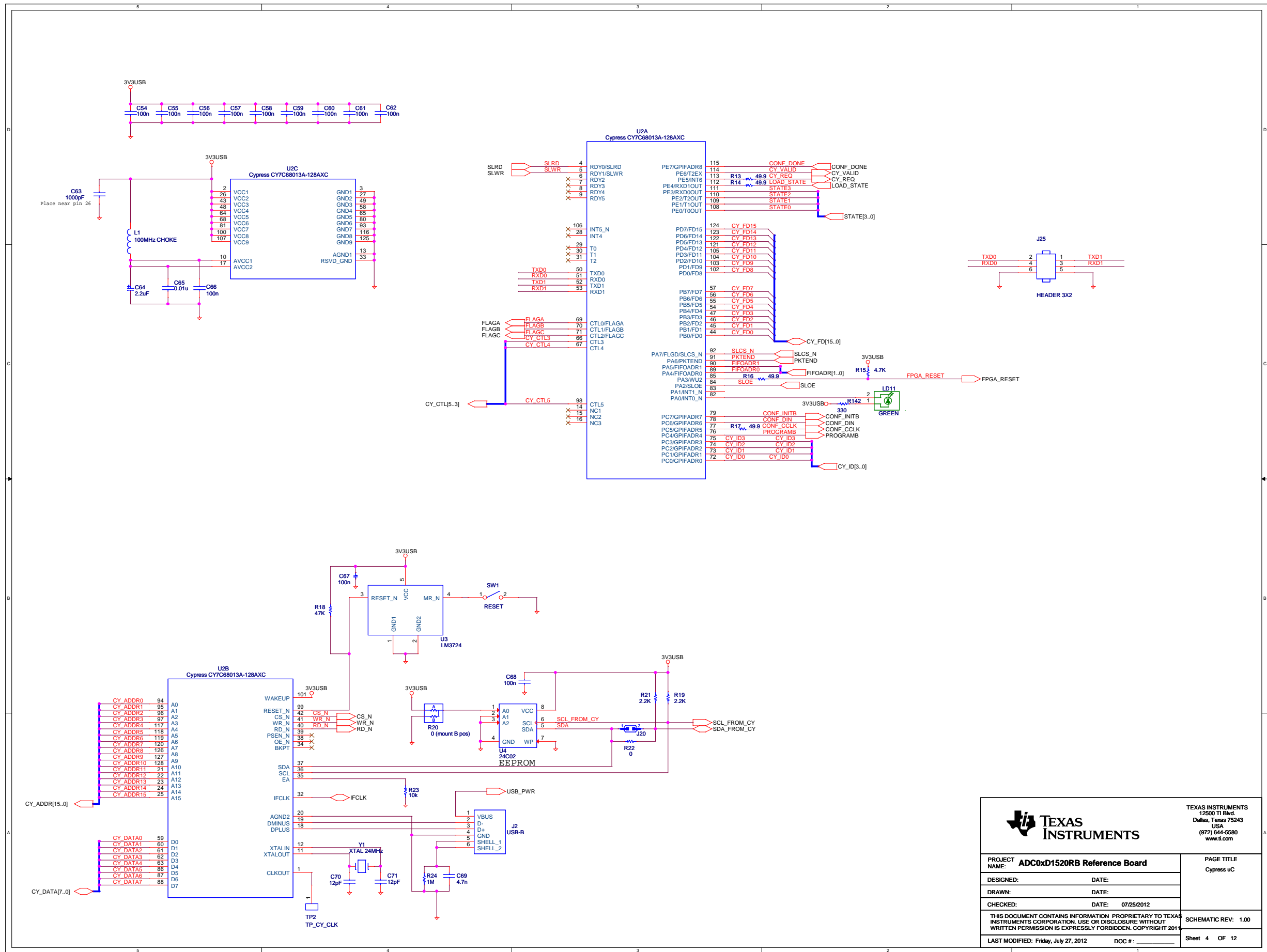


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ASP-134488-01_0

J156_1_2 JUMPER1

R156 10k

FMC PG M2C

FMC DQ+0 FMC DQ-0

FMC DQ+4 FMC DQ-4

FMC DQ+8 FMC DQ-8

FMC DQ+2 FMC DQ-2

FMC DQ+4 FMC DQ-4

FMC DQ+8 FMC DQ-8

FMC ORQ+ FMC ORQ-

FMC DQ+11 FMC DQ-11

FMC DQ+1 FMC DQ-1

FMC DQ+3 FMC DQ-3

FMC DQ+7 FMC DQ-7

FMC DQ+11 FMC DQ-11

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FMC DQ+1 FMC DQ-1

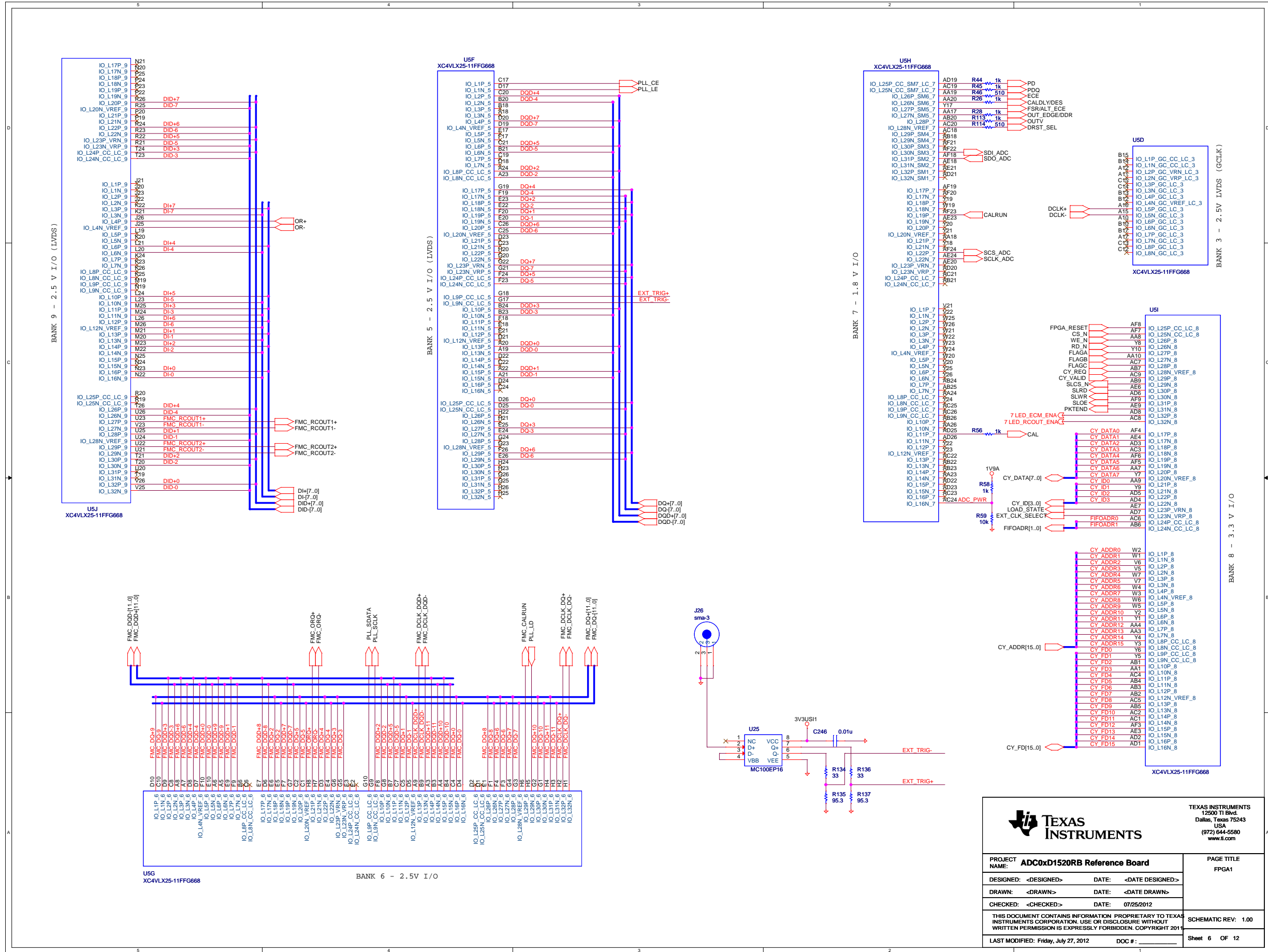
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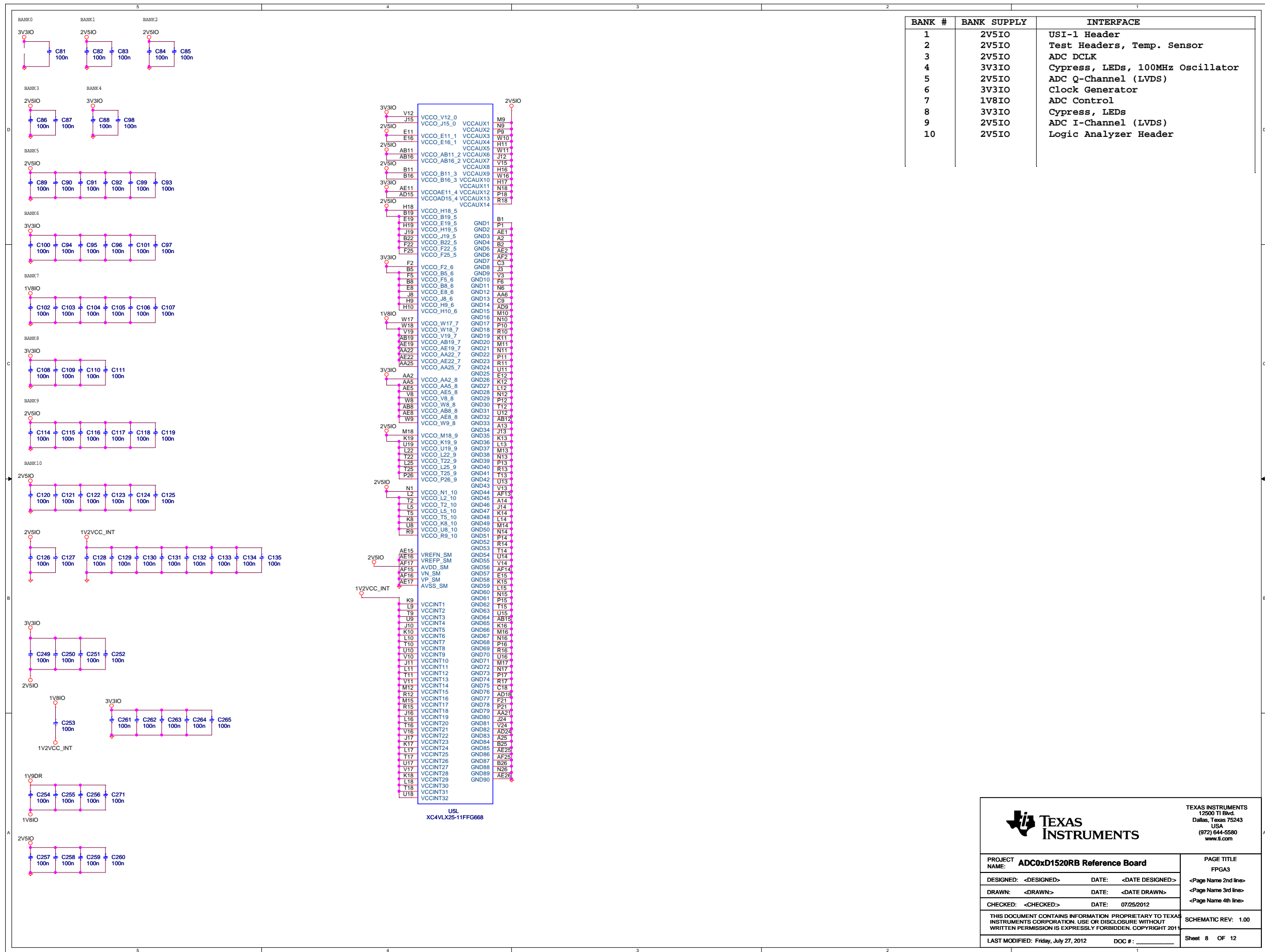
FMC DQ+1 FMC DQ-1

FMC DQ+3 FMC DQ-3



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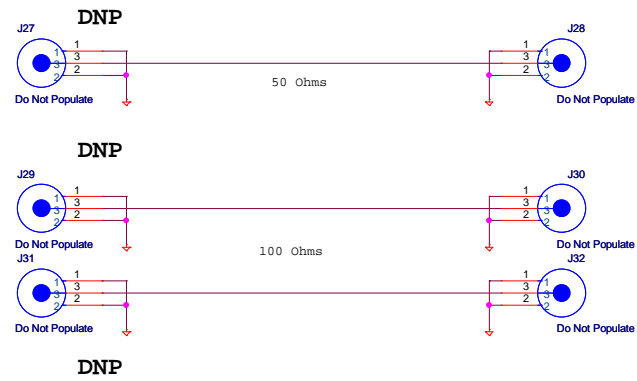
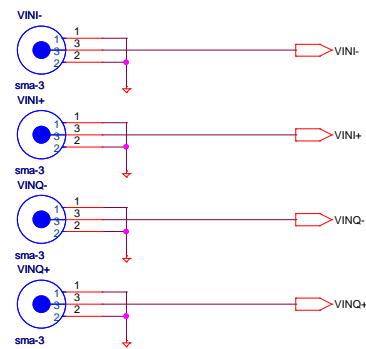
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1	2V5IO	USI-1 Header
2	2V5IO	Test Headers, Temp. Sensor
3	2V5IO	ADC DCLK
4	3V3IO	Cypress, LEDs, 100MHz Oscillator
5	2V5IO	ADC Q-Channel (LVDS)
6	3V3IO	Clock Generator
7	1V8IO	ADC Control
8	3V3IO	Cypress, LEDs
9	2V5IO	ADC I-Channel (LVDS)
10	2V5IO	Logic Analyzer Header

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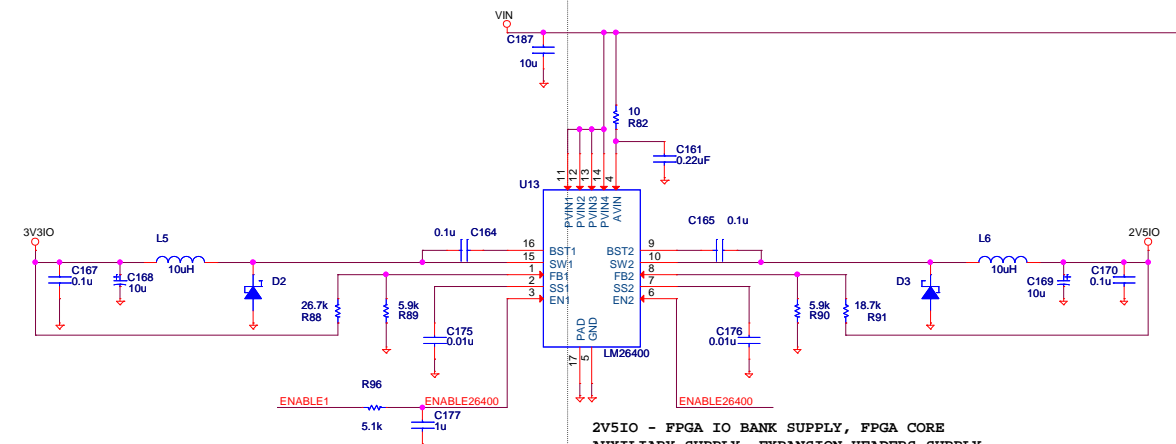
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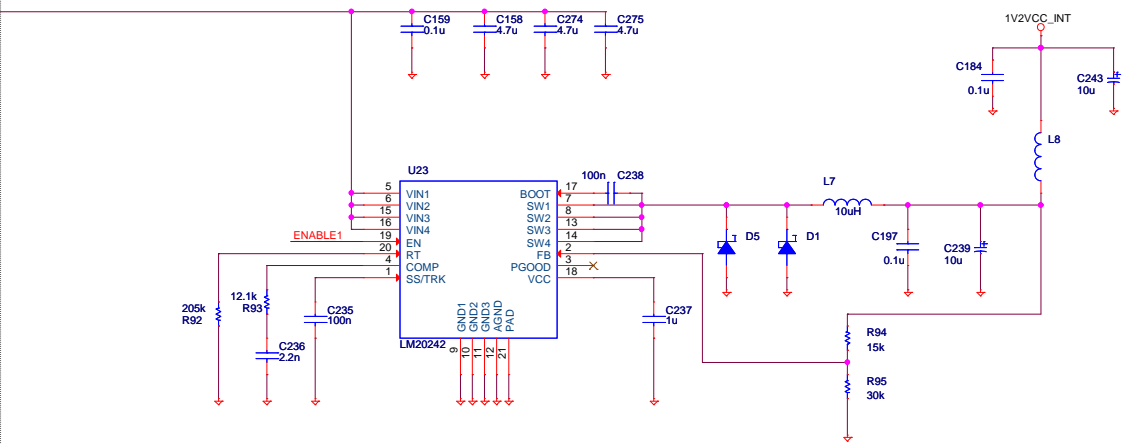
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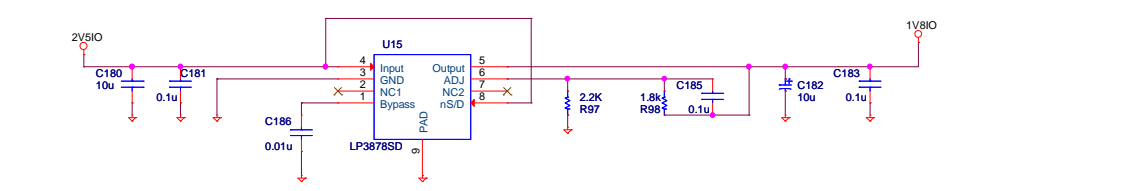


3V3IO - FPGA IO BANK SUPPLY

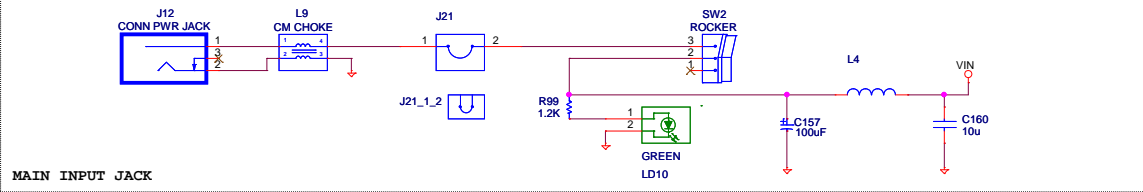
2V5IO - FPGA IO BANK SUPPLY, FPGA CORE AUXILIARY SUPPLY, EXPANSION HEADERS SUPPLY



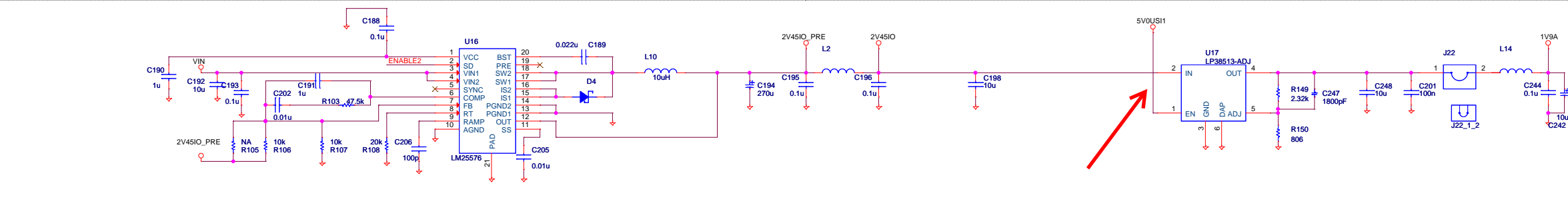
1V2VCC_INT - FPGA CORE SUPPLY



1V8IO - ADC IO SUPPLY, FPGA IO BANK SUPPLY

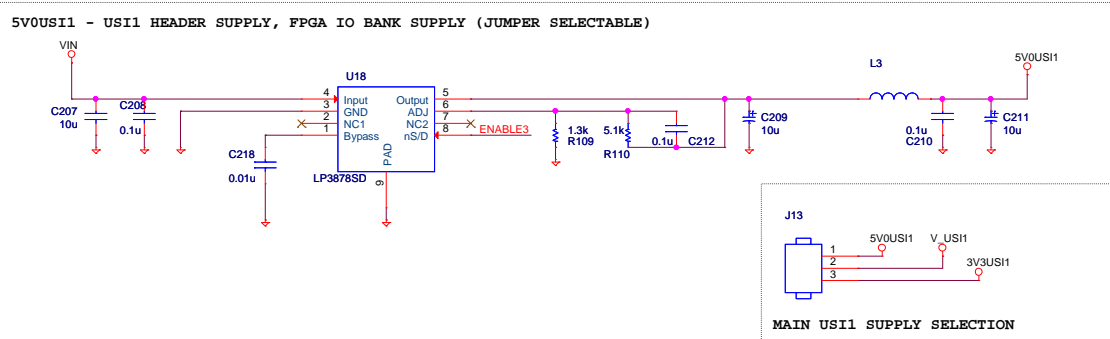


MAIN INPUT JACK



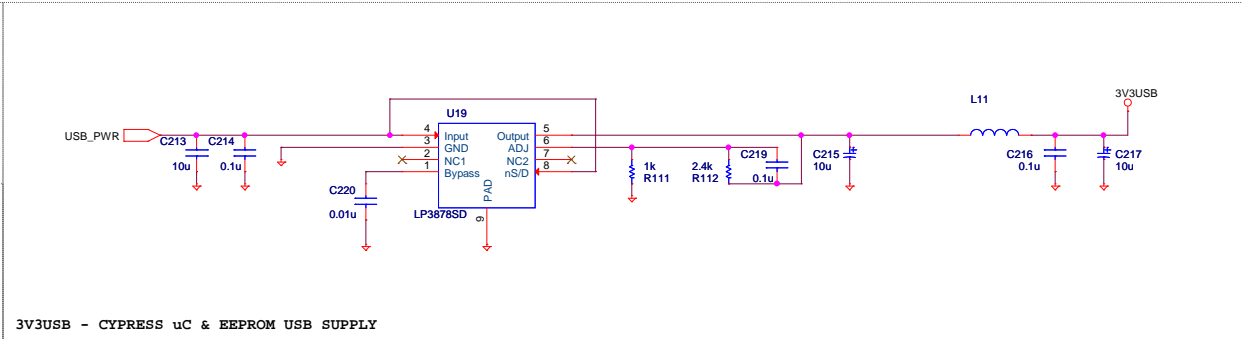
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1V9A - ADC ANALOG SUPPLY

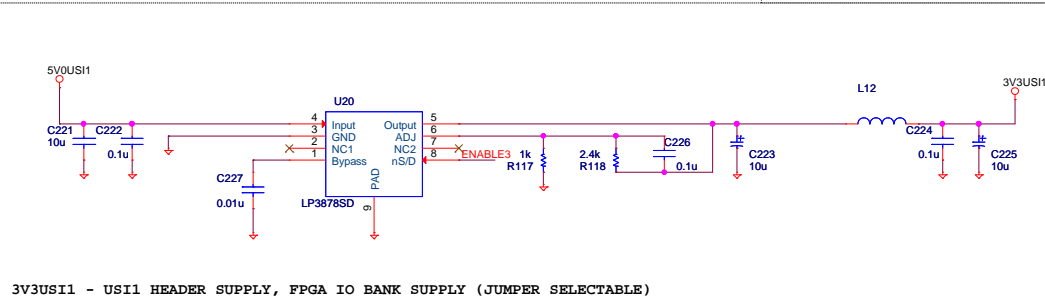


5V0US11 - US11 HEADER SUPPLY, FPGA IO BANK SUPPLY (JUMPER SELECTABLE)

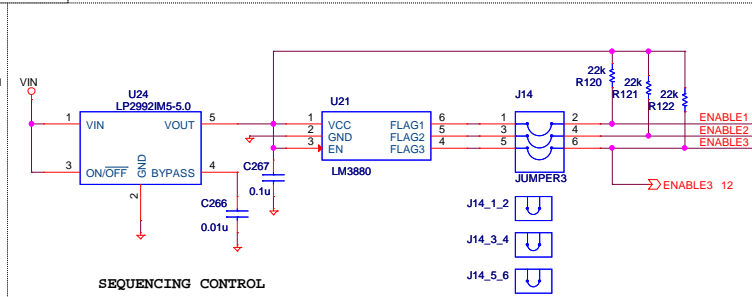
MAIN US11 SUPPLY SELECTION



3V3USB - CYPRESS uC & EEPROM USB SUPPLY



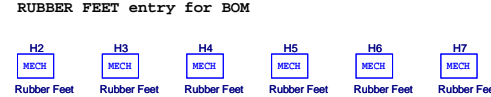
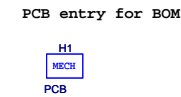
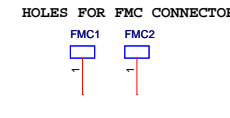
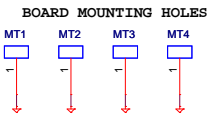
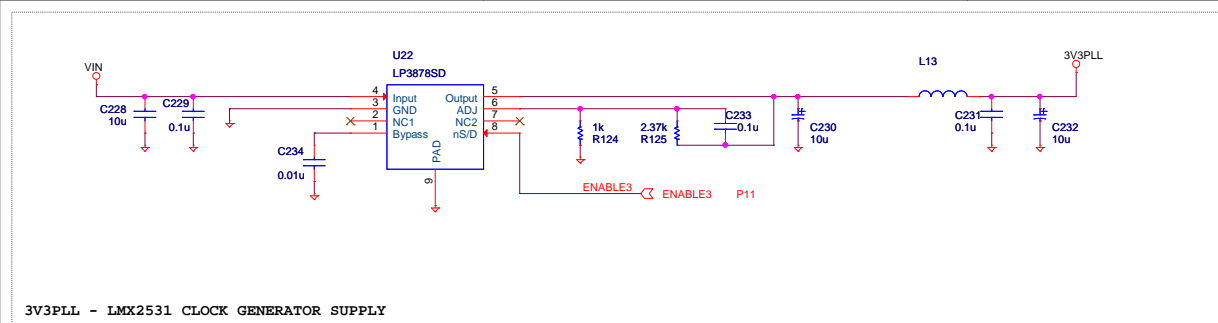
3V3US11 - US11 HEADER SUPPLY, FPGA IO BANK SUPPLY (JUMPER SELECTABLE)



SEQUENCING CONTROL

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