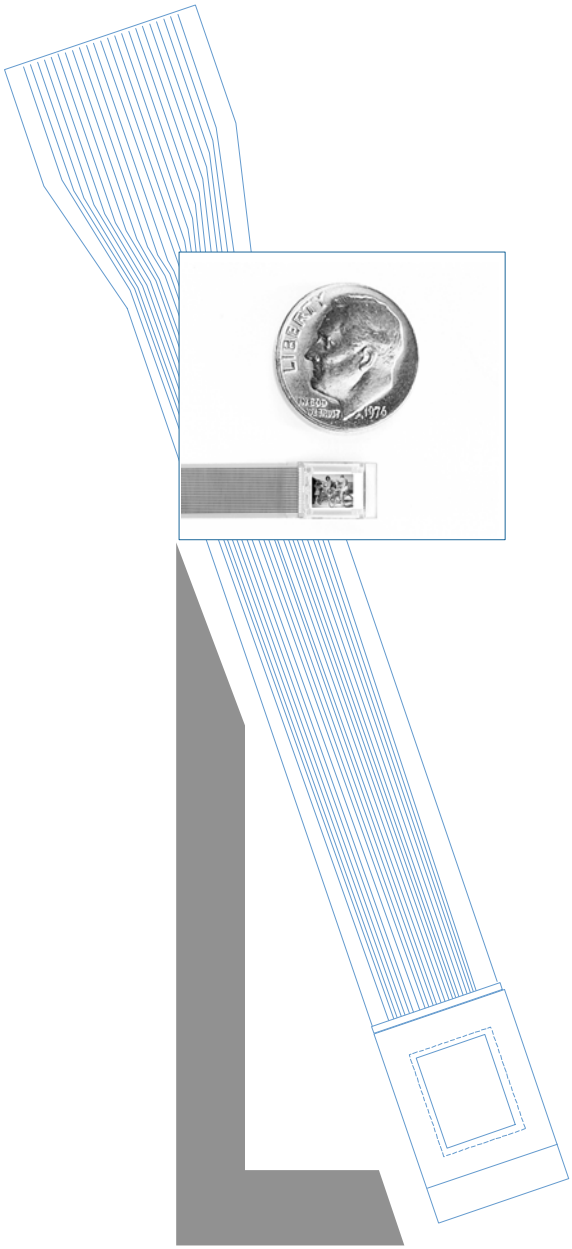
Preliminary

KOPIN

CyberDisplay®



Low Voltage CyberDisplay® WQVGA LVS Color Filter Display / Backlight Module

KCD-QWMS-BB

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PS-0285 Rev. 0.5 2012-09-20

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1. General Description

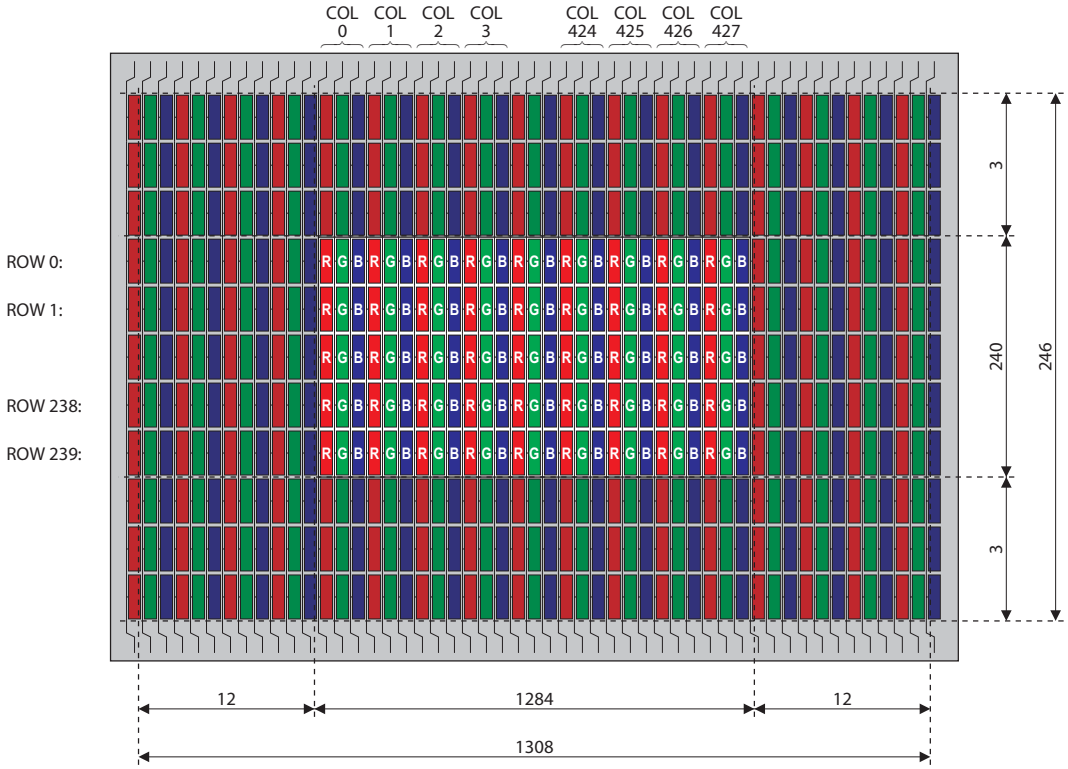
The Low Voltage CyberDisplay® WQVGA LVS color filter display / backlight module is an active-matrix liquid crystal display with 428 × 240 × 3 color dot resolution. It consists of the Low Voltage CyberDisplay® WQVGA LVS Color filter display mated to a white LED backlight. The display is fabricated in a high speed, low power CMOS process utilizing single crystal silicon-on-insulator (SOI) starting material. The display features a low-voltage interface for ompatibility with CMOS driver Ics. Horizontal and bidirectional vertical scanner circuits are integrated. A sleep mode is provided to simplify system power management.

Figure 1-1 shows the pixel array layout. Each square full-color pixel is composed of three pimary color dots. The active array of 1284 × 240 dots is surrounded by opaque dummy pixels, for a total array size of 1308 × 246 dots.

Features

- 436 × 246 × 3 total resolution
- 428 × 240 × 3 active resolution
- 3.5 × 10.5 µm dot pitch (10.5 × 10.5 µm square pixels)
- Simple low voltage interface
- Wide 16:9 format
- Power-saving sleep mode
- Integrated low voltage detect
- Integrated horizontal and vertical scanners
- Bidirectional vertical scanning
- Ultra-compact: Active pixel area 4.494 mm × 2.52 mm (0.20 inch diagonal)

Figure 1-1: Pixel Array

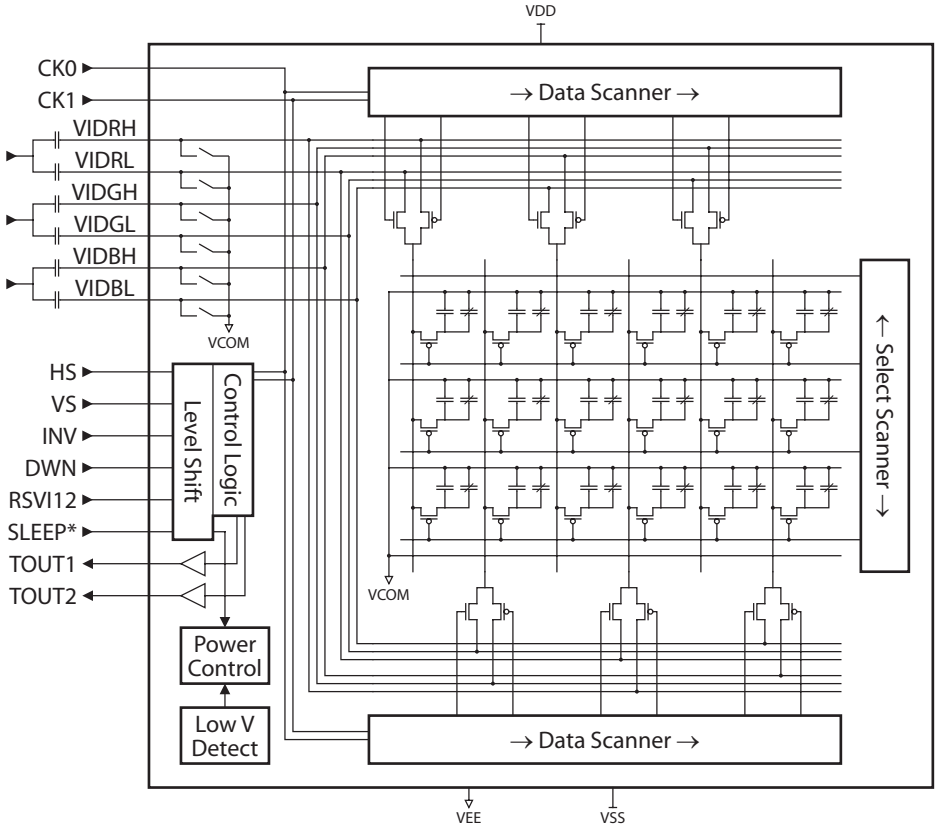


2. Electrical Specifications – LCD

A block diagram of the Low Voltage CyberDisplay® WQVGA LVS is shown in Figure 2-1. External capacitors couple the RGB component signals to the display's six video inputs, with one pair of high and low inputs for each primary color (red, green, and blue). The row inversion drive scheme requires that video polarity be inverted on alternating rows, with the INV signal selecting the high or low inputs.

Integrated scanners drive the active matrix pixel array. The vertical scan direction is controlled by the DWN input.

Figure 2-1: Low Voltage CyberDisplay® WQVGA LVS Block Diagram



2.1 Interface signals

A 21-pin flex cable provides electrical connection to the Low Voltage CyberDisplay® WQVGA LVS. The interface signals are listed in Table 2-1.

Table 2-1: Interface Pin List

Pin	Symbol	Description
1	VEE	Supply = 0V
2	VIDRH	High red video input
3	VIDGH	High green video input
4	VIDBH	High blue video input
5	VIDRL	Low red video input
6	VIDGL	Low green video input
7	VIDBL	Low blue video input
8	HS	Horizontal sync
9	VS	Vertical sync
10	INV	Inversion polarity
11	DWN	Vertical scan direction (H = top-to-bottom)
12	RSVI12	Reserved input. Must be digital input high.
13	SLEEP*	Sleep mode
14	CK0	Clock
15	CK1	Clock
16	VDD	Supply
17	VSS	Supply = –5V
18	RSVO18	Reserved output
19	RSVO19	Reserved output
20	VEE	Supply = 0V
21	RSVI21	Reserved (tied to Pin 20)

* Signal is active low

2.2 Electrical characteristics

Permanent damage to the display may result if the Absolute Maximum Ratings in Table 2-2 are exceeded. The Absolute Maximum Ratings are not typical operating conditions.

Table 2-2: Absolute Maximum Ratings

Note: All voltages relative to V_{EE}=0.

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage — source	V_{DD}	– 0.5	5.5	V
Supply voltage — sink	V_{SS}	– 7.0	0.5	V
All inputs	V_I	V_{SS}– 0.5	V_{DD}+ 0.5	V

Table 2-3: Recommended DC Operating Conditions

Notes: All voltages relative to V_{EE}=0.
The relationships of $V_{HK} = -V_{LK}$ and $V_{HW} = -V_{LW}$ must be maintained.

Parameter	Symbol	Min	Typ	Max	Units
Supply voltage — source	V_{DD}	3.5	4.0	5.0	V
Supply voltage — sink	V_{SS}	– 6.0	– 5.5	– 5.0	V
VID[RGB]H high black level	V_{HK}		V_{DD} – 0.5	V_{DD} – 0.4	V
VID[RGB]H high white level	V_{HW}	– 0.5	0		V
VID[RGB]L low white level	V_{LW}		0	0.5	V
VID[RGB]L low black level	V_{LK}	Vss + 1.8	V_{SS} + 2.0		V
Digital input high	V_{IH}	0.9 V_{DD}			V
Digital input low	V_{IL}			0.1 V_{DD}	V

Table 2-4: Electrical Characteristics

Notes: Under nominal conditions of Table 2-3.

Parameter	Symbol	Min	Typ	Max	Units
Operating current — source	I_{DD}		0.8	1.5	mA
Operating current — sink	I_{SS}		0.8	1.5	mA
Operating current	I_{EE}	– 100		100	µA
Input current	I_I	– 10		10	µA
Input capacitance: video inputs	C_{VID}		30	40	pF
Input capacitance: CK0 & CK1	C_C		10	20	pF
Input capacitance: other inputs	C_I		5	10	pF

2.3 Timing specification

The parameters of Table 2-5 are defined in the timing diagrams of this section.

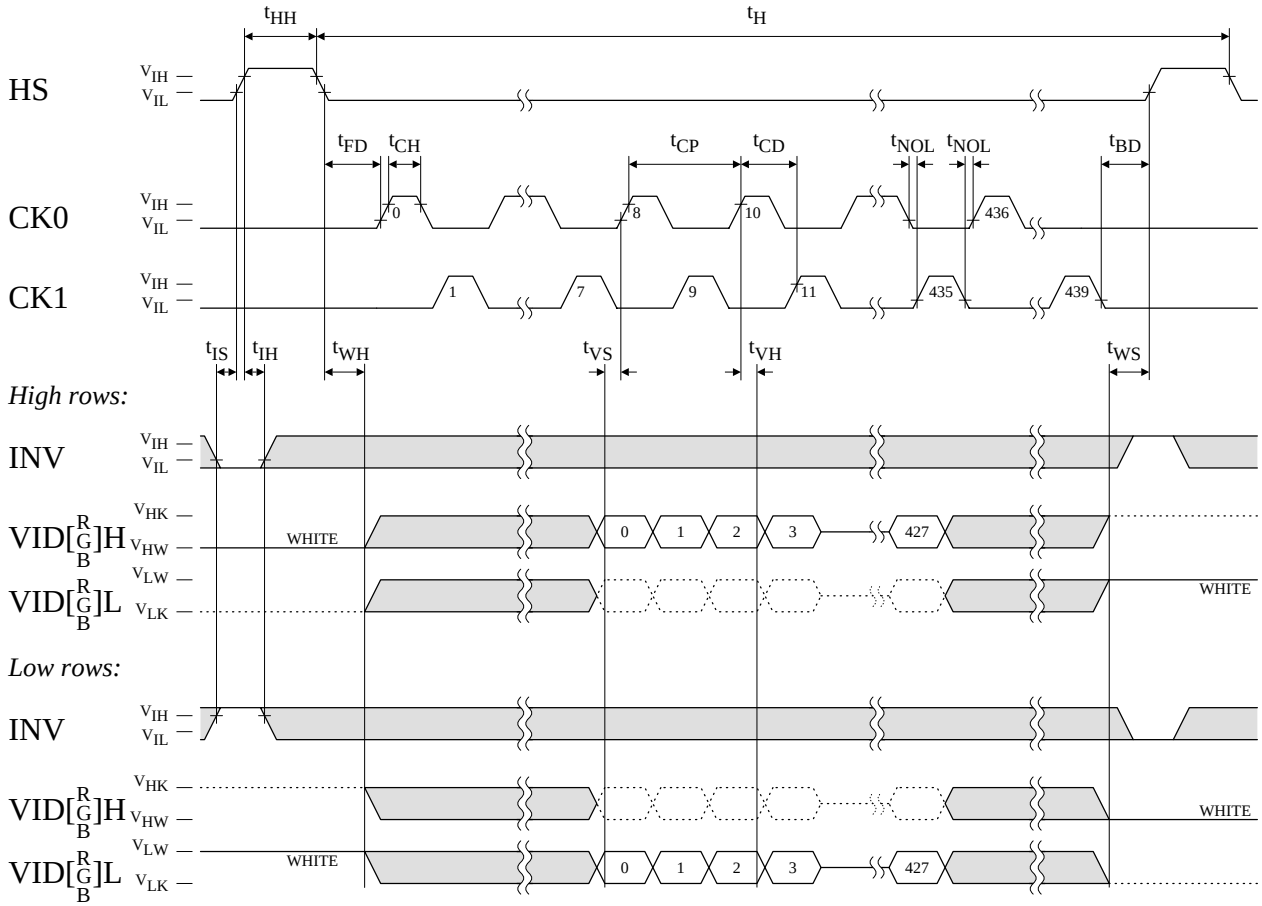
Table 2-5: Recommended AC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Field period	t_V		16.7–20.0		ms
Field rate	$1/t_V$		50–60		Hz
Line period	t_H		64		µs
Line rate	$1/t_H$		15.6–15.7		kHz
Clock period	t_{CP}	220	244	1000	ns
HS high pulse width	t_{HH}	5			µs
HS to CK0 pulse 0 delay	t_{FD}	1			µs
CK1 pulse 439 to HS delay	t_{BD}	1			µs
Clock high pulse width	t_{CH}	100			ns
CK0 to CK1 delay	t_{CD}	$(t_{CP}/2)–5$	$t_{CP}/2$	$(t_{CP}/2)+5$	ns
CK0 and CK1 non-overlap	t_{NOL}	0	5		ns
White hold after HS	t_{WH}	400			ns
White setup before HS	t_{WS}	200			ns
Video setup	t_{VS}	80			ns
Video hold	t_{VH}	50			ns
INV setup before HS	t_{IS}	TBD			ns
INV hold after HS	t_{IH}	TBD			ns
VS high pulse width	t_{VSH}	1			µs
VS low pulse width	t_{VSL}	1			µs
VS to HS delay	t_{VHD}	1			µs
HS to VS delay	t_{HVD}	1			µs

2.4 Horizontal timing

The horizontal timing diagram for left-to-right scan is presented in Figure 2-2. Video is input on either the VID*H or VID*L inputs. The active video inputs are sampled on rising edges of CK0 and CK1, with the first pixel sampled on CK0 edge 8 and the last on CK1 edge 435. The inactive video is driven to the white level in preparation for DC restore.

Figure 2-2: Horizontal Timing, Left-to-Right Scan (TBD)



2.5 Vertical timing

Vertical timing is illustrated in Figure 2-3 and Figure 2-4. Rows will be selected sequentially from top to bottom or bottom to top for DWN=1 or DWN=0, respectively. Most video formats also include some number of inactive rows during a vertical retrace interval.

When the horizontal frequency is not an integer multiple of the frame rate, it may be necessary to extend one inactive row by a fractional row period. As shown in Figure 2-5, the additional time should be added between the end of the clock burst and the rising edge of HS.

Figure 2-3: Vertical Timing, Top-to-Bottom Scan

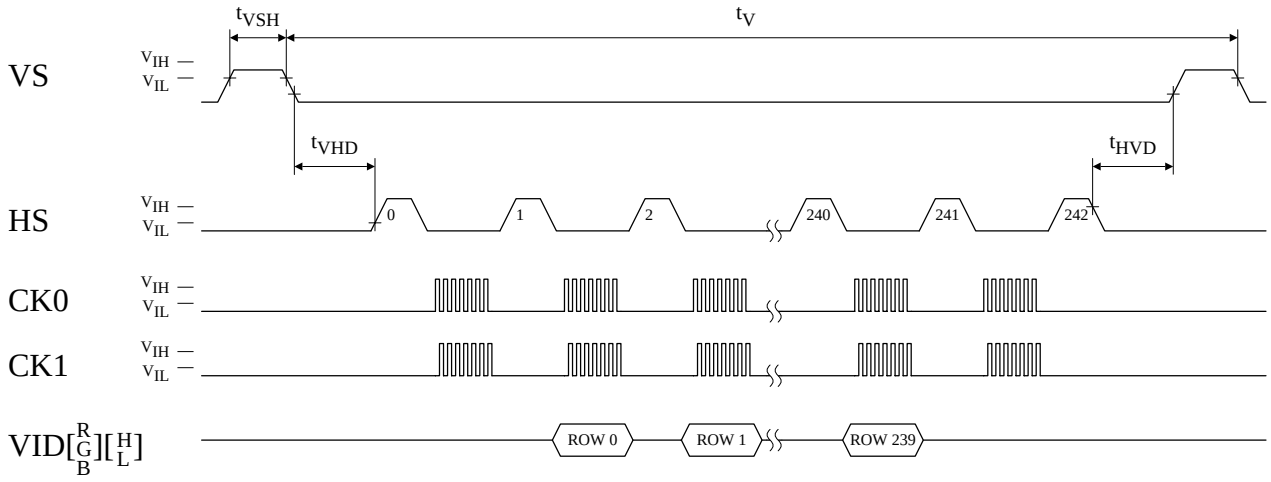


Figure 2-4: Vertical Timing, Bottom-to-Top Scan

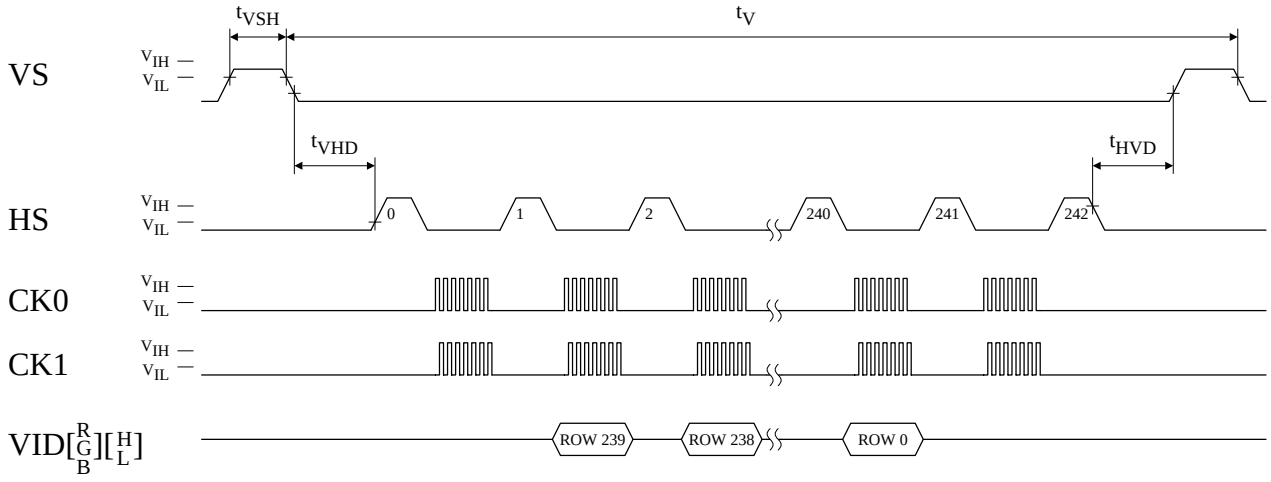
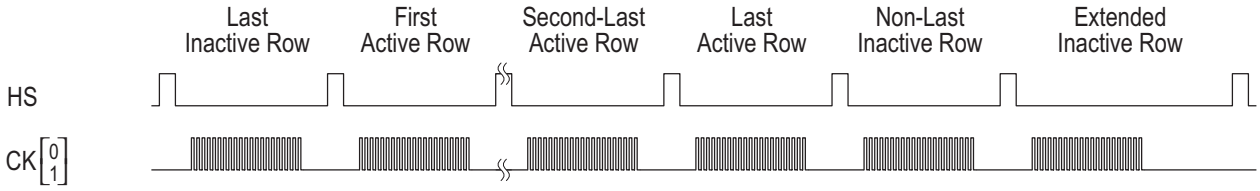


Figure 2-5: Vertical timing



2.6 Inversion

To preserve DC balance in the liquid crystal, each pixel must be driven with alternating high and low video. The Low Voltage CyberDisplay® WQVGA LVS uses row inversion, in which all pixels of each row have the same polarity, but successive rows have alternating polarity. The INV signal indicates the polarity of each row (see timing diagrams of §2.4). The row inversion phases must be inverted with successive fields. For example, if one field is driven with row 0 low, row 1 high, and row 2 low, then the following field must have row 0 high, row 1 low, and row 2 high.

2.7 Sleep mode

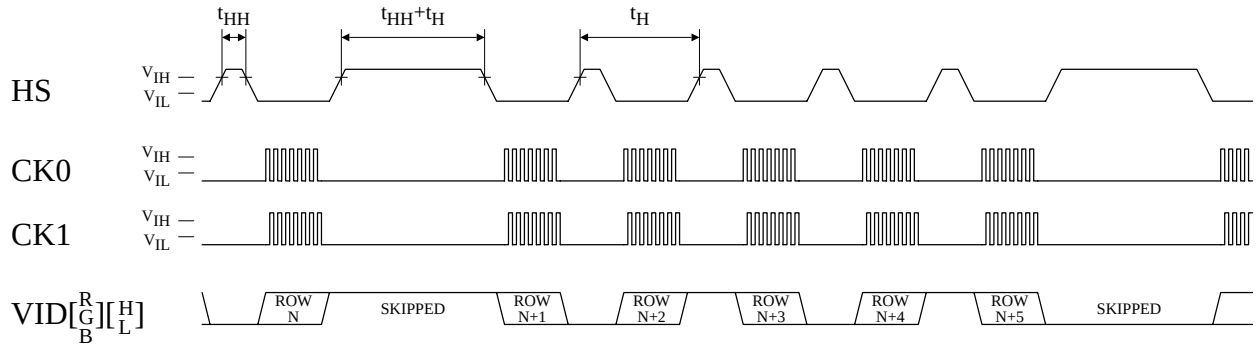
The Low Voltage CyberDisplay® WQVGA LVS features a sleep mode to simplify system power management. When the SLEEP* pin is driven low, all scanners are disabled and the pixel array is driven to the white state. The display may remain powered and will draw minimal current while in sleep mode. The backlight may be turned off.

The display will also enter sleep mode when the integrated low voltage detect circuit determines that power has been removed.

2.8 Line skipping

Simple vertical scaling may be accomplished by line skipping. For example, to display PAL video with the correct aspect ratio, one of every six lines should be skipped. As illustrated in Figure 2-6, the HS pulse should be extended to remain high during the skipped line. This technique mimimizes visible artifacts by preserving the same HS-video timing in the rows before and after the skipped line.

Figure 2-6: Line Skipping Timing Diagram



3. Electrical Specifications – Backlight

3.1 Interface Signals

A 4-pin flex cable provides backlight electrical connection to the backlight. The interface signals are listed in Table 3-1.

Table 3-1: Interface Pin List

Pin	Symbol	Description
1	BL-	LED Cathode
2	BL-	LED Cathode
3	BL+	LED Anode
4	BL+	LED Anode

3.2 Electrical Characteristics

Permanent damage to the backlight may result if the Absolute Maximum Ratings in Table 3-2 are exceeded. The Absolute Maximum Ratings are not typical operating conditions. Typical electrical drive conditions are provided in Table 3-3.

Table 3-2: Backlight Absolute Maximum Ratings

Item	Symbol	Max.	Unit
Forward Current	I_f	30	mA
Reverse Voltage	V_r	5	V
Peak Pulse Current [(1)]	I_{FP}	100	mA
Power Dissipation	P_d	102	mW

[(1)] Duty ratio = 1/10, pulse width = 10msec

Table 3-3: Backlight Typical Electrical Drive Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Forward Current	I_f	-	15	20	mA
Forward Voltage	V_f	-	3.1	3.4	V

4. Optical Specifications

4.1 Optical Characteristics

Table 4-1: Optical Characteristics

Item			Symbol	Notes	Min	Typ.	Max	Unit
Contrast ratio	Vsig = 0 ± 3.5V		$CR_{3.5}25$	1	60	100	--	--
Center Brightness (I_f = 15 mA)		θ=0	L	2	1,000	1,350		cd/m^2
Chromaticity	W	X	Wx	3	0.280	0.320	0.360	CIE standards
		Y	Wy		0.280	0.320	0.360	
	R	X	Rx		0.530	0.570	0.610	
		Y	Ry		0.290	0.330	0.370	
	G	X	Gx		0.250	0.290	0.330	
		Y	Gy		0.510	0.550	0.590	
	B	X	Bx		0.120	0.160	0.200	
		Y	By		0.070	0.110	0.150	
V-T characteristics	V_{90}	25°C	V_{90-25}	4	0.4	0.7	1.0	V
	V_{50}	25°C	V_{50-25}		1.1	1.4	1.7	
	V_{10}	25°C	V_{10-25}		1.7	2.1	2.5	
Response time	ON time	25°C	ton_{25}	5	--	5	10	ms
	OFF time	25°C	$toff_{25}$		--	40	60	
Flicker			F	6	--	--	-40	dB

Notes On Measurement Conditions:

1. $CR_{3.5}25$ = (Luminance White)/(Luminance Black). System I.
2. Measured at the center of powered display under proper image condition. System I.
3. CIE Standard 1931. System I. Reference backlight (x=0.300, y=0.300)
4. V-T is relationship of signal amplitude to transmittance. System I.
5. VESA 2.0 standard. System I + Oscilloscope
6. 20log(AC/DC) @ 50% transmittance. System I + Spectrum Analyzer

System I: Equipment: PR-670 @ 2 mm spot size. Reference backlight <15° collimation.

5. Environmental Specifications

5.1 Flex Cable Interconnect

The flexible PC cable is strain relieved, but tugging forces should be limited to less than 0.5 kg perpendicular to the display and less than 1 kg parallel to the display. The minimum inside bend radius for the cable is 0.75 millimeters. Repeated reformings are not recommended.

5.2 Display Reliability

Table 5-1: CyberDisplay® WQVGA LVS Display Environmental Specification

Storage Temperature	–20°C to 70°C
Operating Temperature	0°C to 60°C
Humidity – Storage	40°C at 80% humidity for 240 hours
Vibration	20 to 2,000 Hz, 6G's RMS maximum 3 axes 10 minutes each axis

6. Mechanical Specifications

6.1 Mechanical drawings

Figure 6-1: Low Voltage CyberDisplay® WQVGA LVS Display and Pixel Array Area

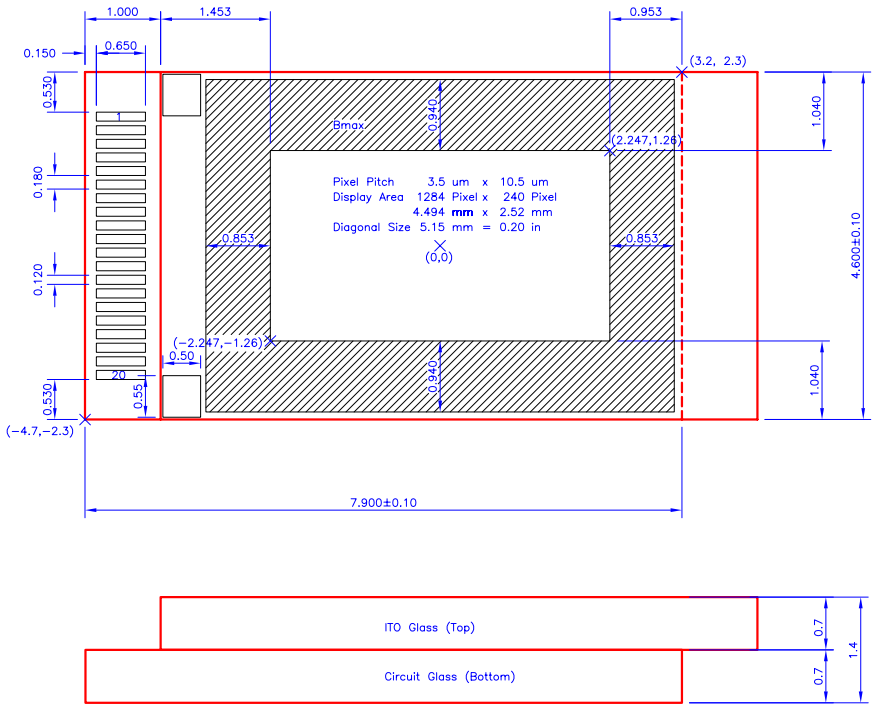


Figure 6-2: Low Voltage CyberDisplay® WQVGA LVS Display / Backlight Module

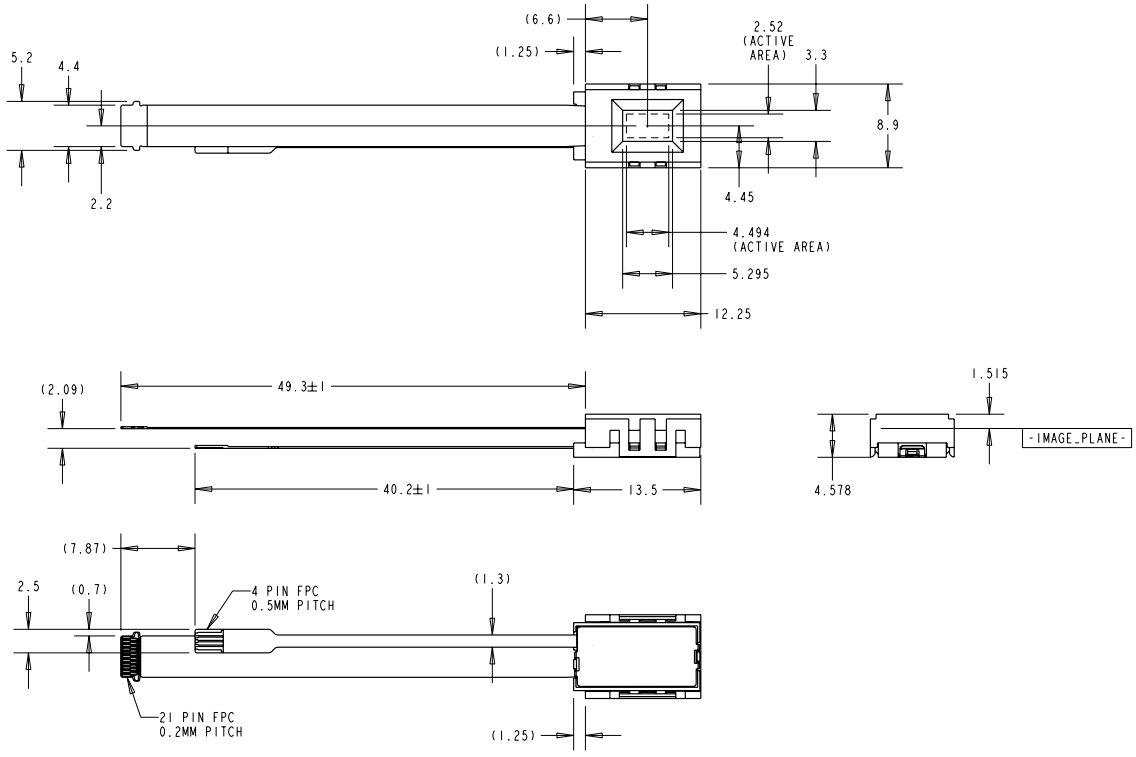


Figure 6-3: Display FPC Interconnect – Contact Pad Area

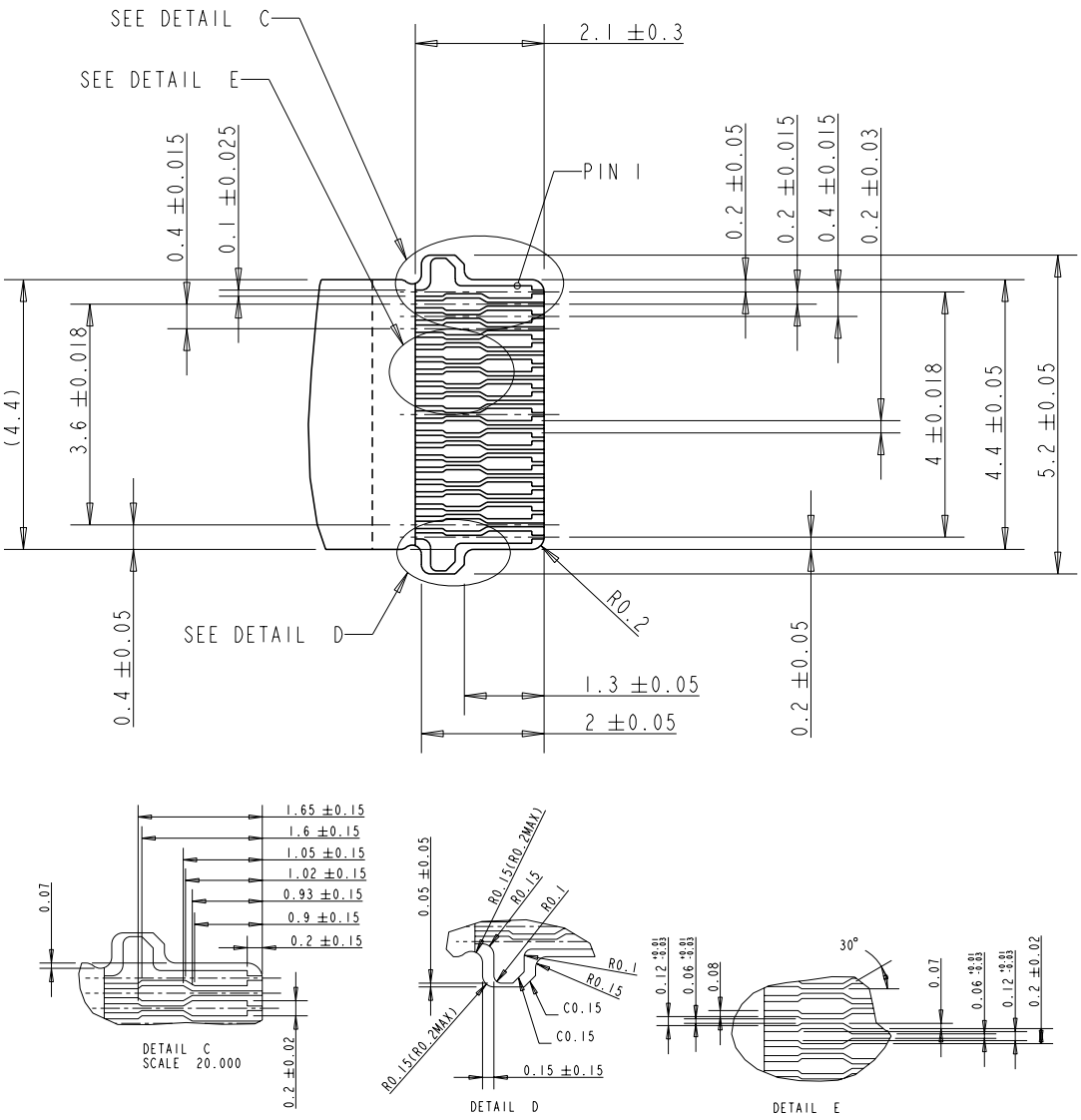
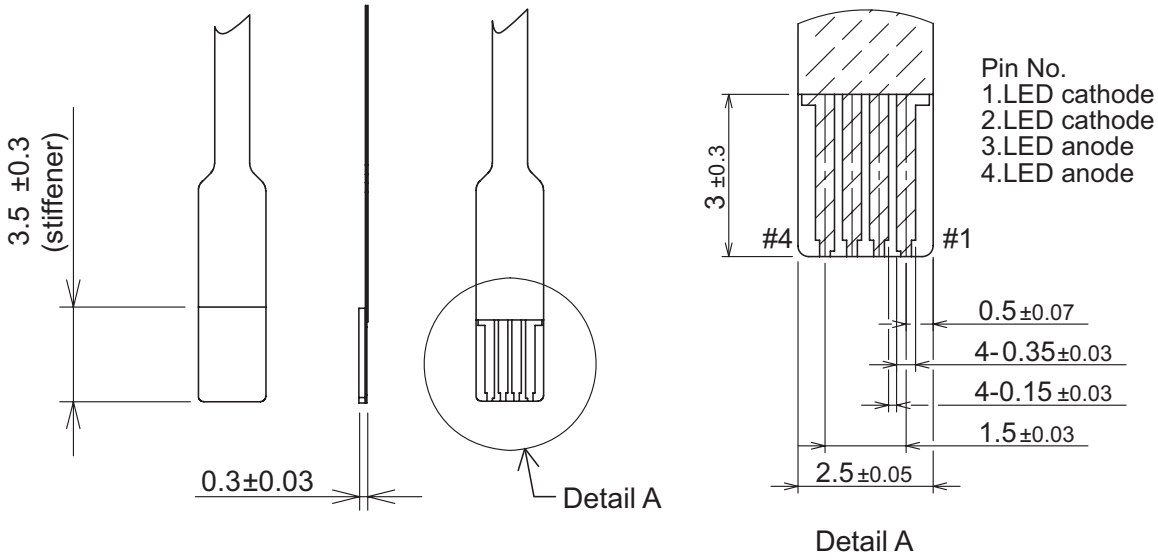


Figure 6-4: Backlight FPC Interconnect – Contact Pad Area



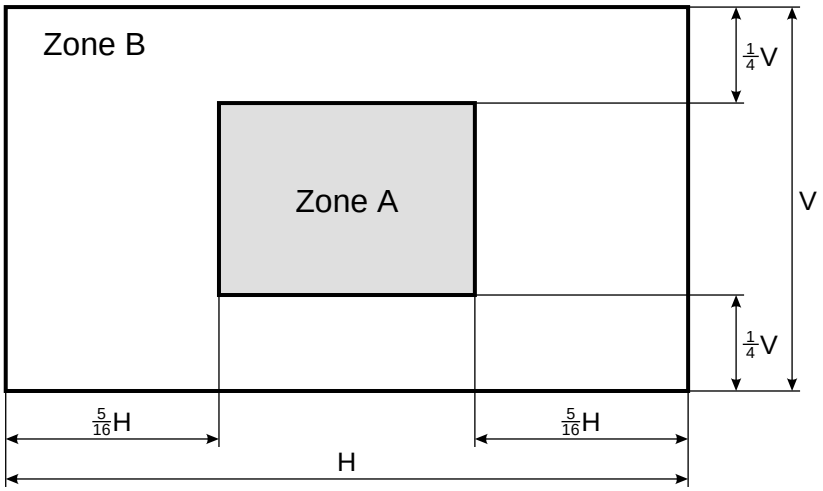
7. Display Appearance

Table 7-7-1: Display Appearance

Defect Type	Defect Criteria
Circuit	No obvious partial or faded image, streaking or shadow, unstable image, or alternating columns or rows
Line	No lines out Very faint lines allowable based on limit samples
Pixel	See Figure 7-1
Adjacent pixels	Two : Same criteria as for pixel defects, based on aggregate brightness (See Figure 7-1) Three or more: Not allowed

Test Conditions: Test board runs in row inversion at 60 Hz frame rate. Visual focal plane is on the pixel array.
Limit Samples: Limit samples to be used for pixel and other cosmetic defects as required.

Figure 7-1: Display Appearance Specification



ZONE	DEFECT	NUMBER
A	S, M, or L	1
B	S or M	4
	L	1

where:

Small (S) defect differs from nominal pixel brightness by 10–25%.
Medium (M) defect differs from nominal pixel brightness by 25–75%.
Large (L) defect differs from nominal pixel brightness by ≥ 75%.
Defect can be black or white spot.