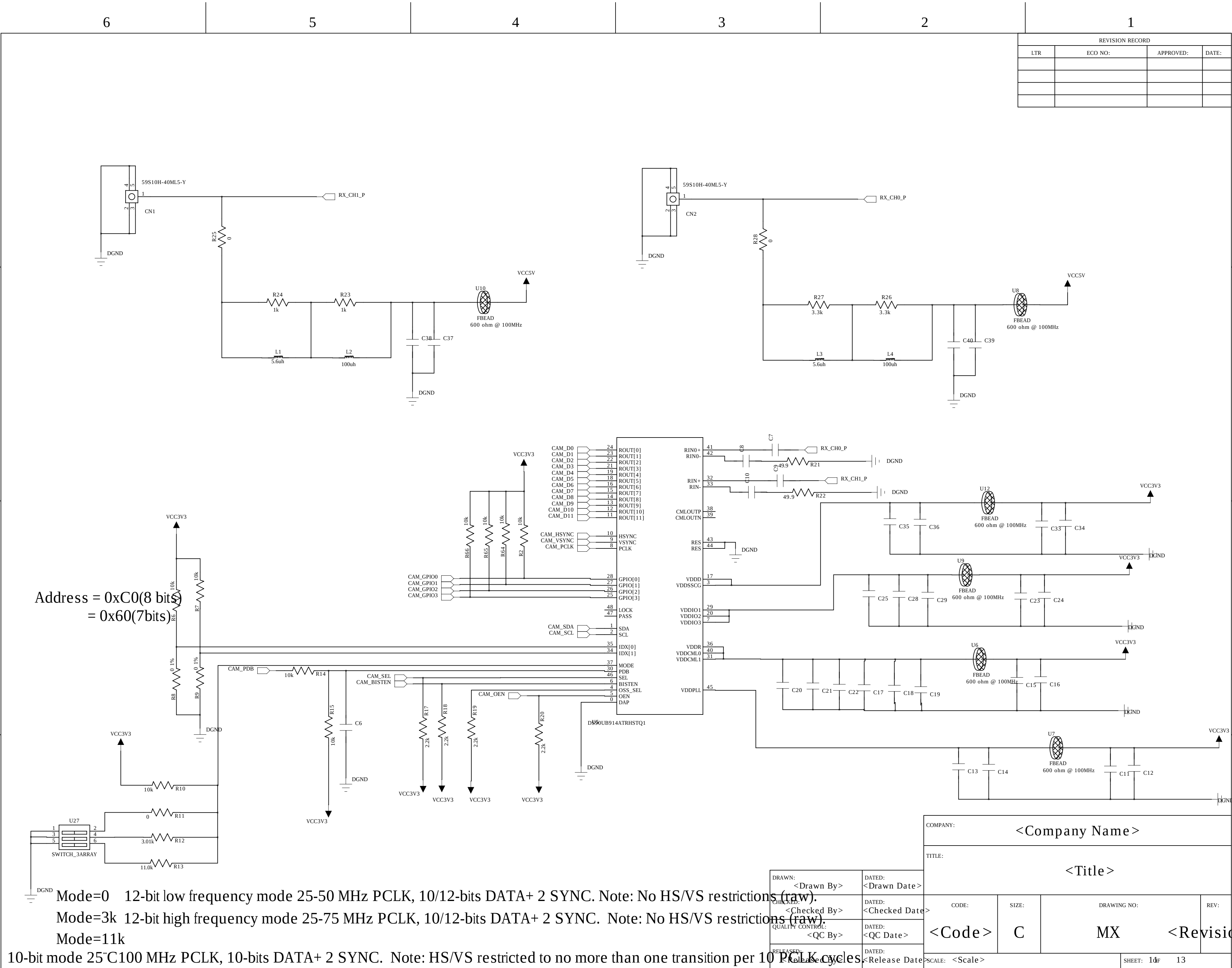




REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

Address = 0xC0(8 bits)
= 0x60(7bits)

Mode=0 12-bit low frequency mode 25-50 MHz PCLK, 10/12-bits DATA+ 2 SYNC. Note: No HS/VS restrictions (raw).
Mode=3k 12-bit high frequency mode 25-75 MHz PCLK, 10/12-bits DATA+ 2 SYNC. Note: No HS/VS restrictions (raw).
Mode=11k 10-bit mode 25-100 MHz PCLK, 10-bits DATA+ 2 SYNC. Note: HS/VS restricted to no more than one transition per 10 PCLK cycles.

DRAWN: <Drawn By>	DATED: <Drawn Date>
CHECKED: <Checked By>	DATED: <Checked Date>
QUALITY CONTROL: <QC By>	DATED: <QC Date>
RELEASED: <Release By>	DATED: <Release Date>

COMPANY: <Company Name>			
TITLE: <Title>			
CODE: <Code>	SIZE: C	DRAWING NO: MX	REV: <Revision>
SCALE: <Scale>			SHEET: 1 of 13