



Table 2. EQ Boost Control Table

Control Via SMBus BC_2, BC_1, BC_0 (FEB = 0)	Control Via Pins BST_2, BST_1, BST_0 (FEB = 1)	EQ Boost Setting at 825 MHz (dB) (TYP)
000	000	9
001	001	14
010	010	18
011	011	21
100	100	24
101	101	26
110	110	28
111	111	30

50R on chip terminator
TMDS output CML, OC

SD: active high signal is detected

CS: IPD
H: I2C enable
L: I2C disable

FEB: IPU
H: BST control boost
L: I2C control boost

EN: IPU
H: normal mode
L: standby mode

BST_0
BST_1 BST0/1/2: IPD
BST_2

SCL SDA

DS16EV5110ASQE/NOPB

FEB拉低且cs拉高, 使能I2C配置