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## ***Demystify DSI I/F***

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### **ABSTRACT**

The purpose of this Application Note (APN) is to demystify the DSI I/F by presenting different configuration and their impact on the DSI protocol. The document is illustrated by numerous waveforms probe on an OMAP platform.

This APN covers the DSI protocol in video mode (Non-frame buffer display) and in command mode (frame buffer display).

A section dedicated to debugging tips is enumerating different method to measure various parameters and decode LP and HS packets.

However the APN does not contain programming model and complete DSI protocol standard, for more details on programming model refer to the OMAP Technical Reference Manual and the MIPI DSI protocol standard.

### **Document History**

<b>Version</b>	<b>Date</b>	<b>Author</b>	<b>Notes</b>
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## 1 MIPI DSI protocol

Two modes are supported in the MIPI DSI protocol standard, **Command mode and Video mode**. This section details briefly these modes but for complete details refer to *MIPI Alliance Specification for Display Serial Interface Version 1.02.00*.

### 1.1 Command mode

Command mode is used when the panel integrates a display controller and a frame buffer (FB). Transfer usually takes place in a form of a command followed by data pixels and/or parameters. The Host can write to and read from the panel registers and FB.

The start of the frame transfer can be controlled by the panel using the Tearing Effect (TE) either by an external pin, TE line, or via the DSI lanes using the TE trigger message.

As data could be transmitted from panel to host, the host I/F have a bidirectional lane.

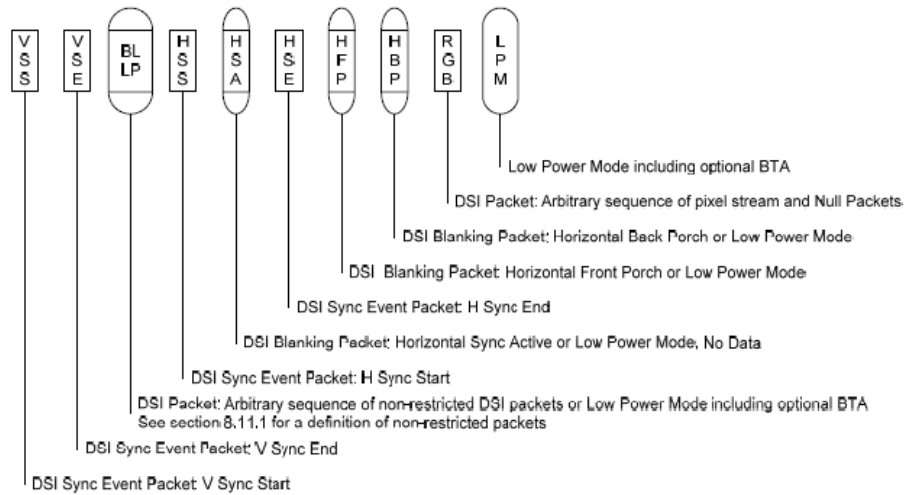
### 1.2 Video mode

During a **Video mode** transfer, pixel data are transferred from Host to panel in real-time. Panels may include simple timing controller and partial FB.

Within the video mode, 3 different sub-modes are present:

- **Non-burst Mode Sync pulses:** In this mode, based on the various synchronization packets sent, it is possible to reconstruct, time-accurate, the pixel streaming and also the synchronization timings as defined in the DPI standard. Refer to Figure 2.
- **Non-burst Mode Sync event:** It is similar to Non-burst Mode Sync pulses, except that the accurate reconstruction of sync timings is not possible. Only single start sync event packets are sent. Refer to Figure 3.
- **Burst mode:** The DSI speed link is increased to the maximum speed supported by the panel while maintaining same horizontal timings. RGB pixel packets are time-compressed. In this case it leaves more time for a LP transition or for other transmission on the link during the scan line. Refer to Figure 4.

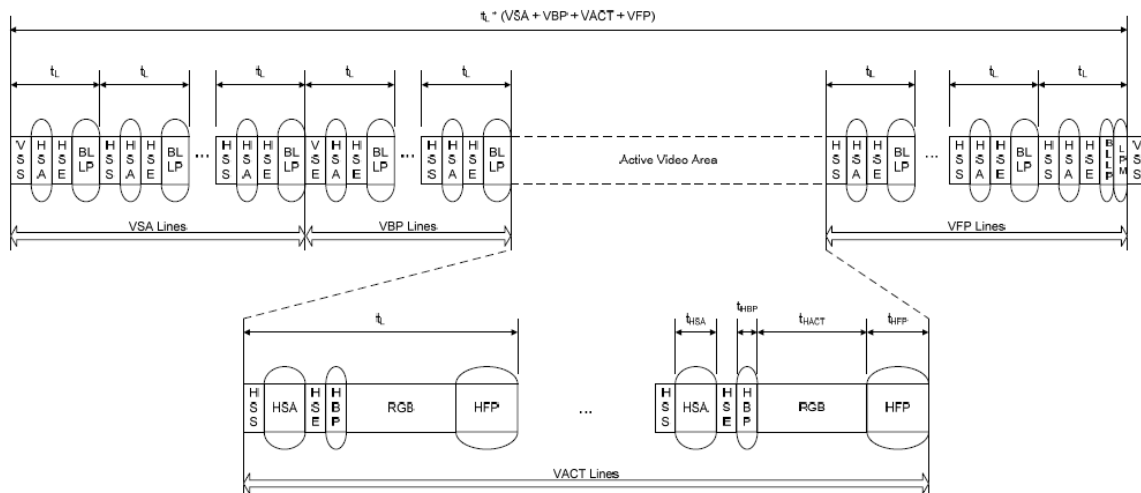
To enable such synchronization, different packets are sent to panels to indicate start and end of porch. Figure 1 presents all packets used for the different sub-video mode.



**Figure 1: Video mode - packets definitions**

In Figure 2 to Figure 4, **BLLP** indicates blanking (BL) or low power (LP) periods. During these periods, the following could happen on the DSI link:

- Host and panel remain in Idle Mode. Lanes are in LP-11 state.
- Host transmits one or more non-video packets to the peripheral using Escape mode (low-power Tx).
- Host transmits one or more non-video packets to the peripheral using HS Mode, for example transmit blanking packets or DCS commands.
- If the previous processor-to-peripheral transmission ended with BTA, panel transmits one or more packets to the host processor using Escape Mode.
- Host Transmit one or more packets to a different peripheral using a different virtual Channel ID (VC).



**Figure 2: Non-burst mode Sync pulses**

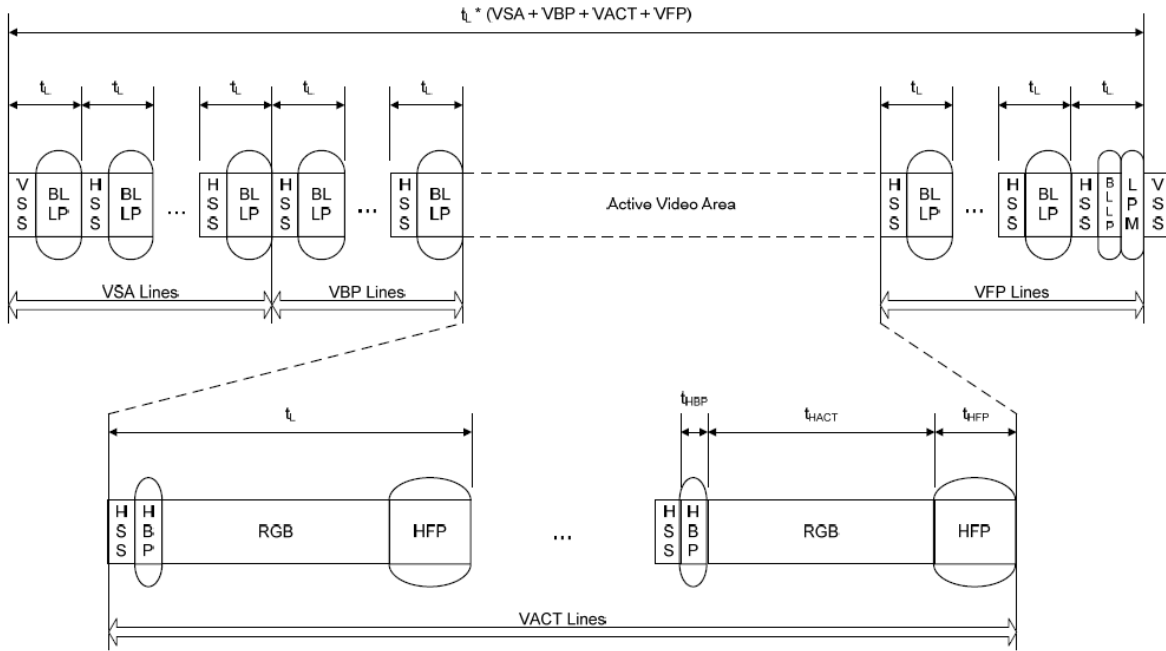


Figure 3: Non-burst mode Sync event

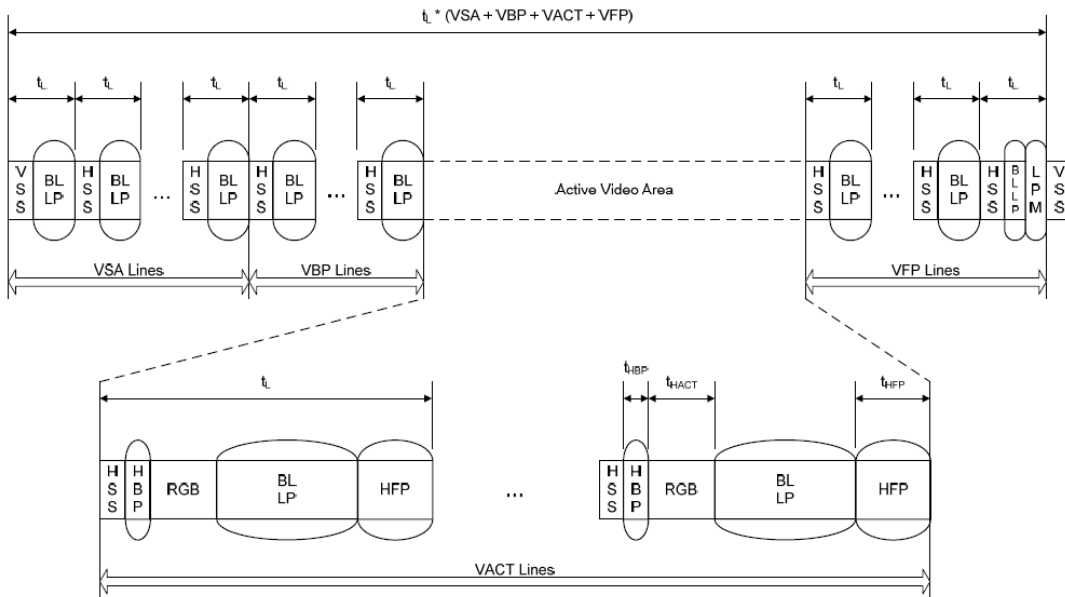


Figure 4: Burst mode

## 2 DSI video mode

### 2.1 Blanking mode.

As explained in section 1.2, during periods of non-transmission of pixel stream (BLLP periods), the DSI link could be in 2 states, low power or HS transmission of blanking packets. OMAP allows user to define the states to be adopted for each horizontal porches and overall vertical porch by configuring HSA\_BLANKING\_MODE, HBP\_BLANKING\_MODE, HFP\_BLANKING\_MODE and BLANKING\_MODE bits in DSI\_CTRL [23:20].

When configuring LPS during blanking, it is the user responsibility to verify that enough time is available to transit from HS to LP and back to HS during the blanking period, specifically for the horizontal period as it is a short period. No HW check is done in the DSI subsystem.

Figure 5 represents the 2 last VACT before a vertical blanking starts. HSS packet is preceded by a period of HFP blanking and then followed by the HBP blanking.

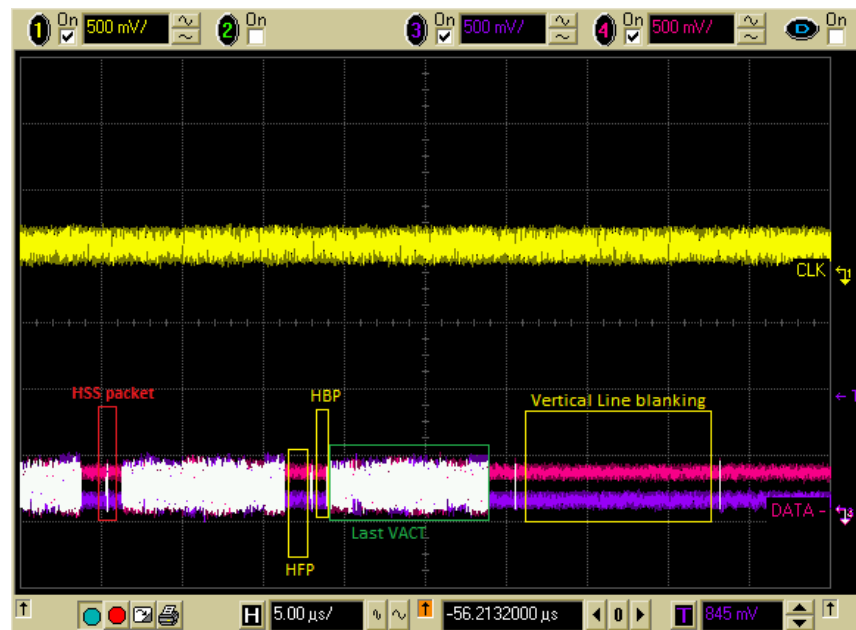


Figure 5: Horizontal blanking of last VACT and vertical blanking

Figure 6 shows a setting with all blanking mode done with blanking packets in HS transmission, all blanking modes are set to default values 0x1. As mentioned in MIPI DSI standard, at least once per frame, OMAP drives the data lanes to LP state. In this configuration, LP transition is done every 16.6ms (60 FPS).

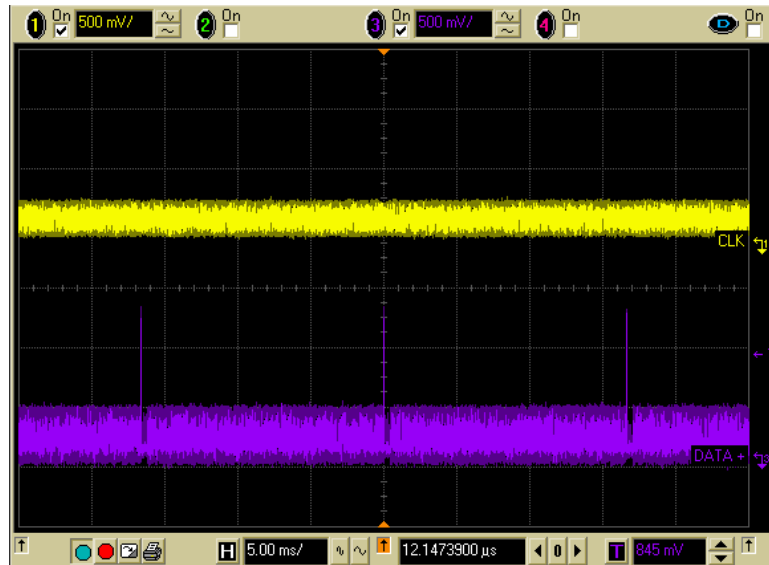


Figure 6: All blanking done in HS blanking packets.

Figure 7 represents a zoom of the vertical blanking period when all blanking mode are set to 0x1. The single LP transition will occur at the first VSA line blanking during vertical blanking. The HSS sync packets followed by the long blanking packets (only 0s) are clearly identified.

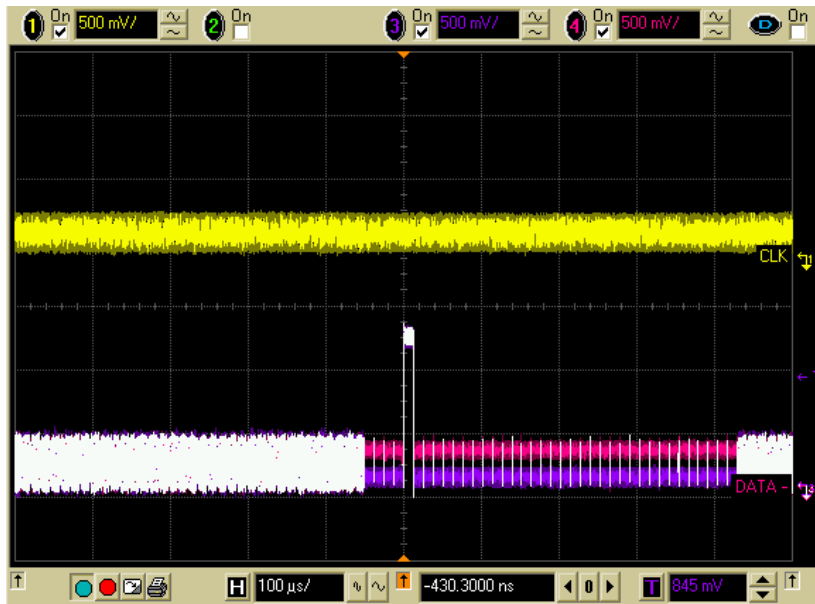


Figure 7: Single LP transition per frame

Figure 8 shows a sync event configuration where BLANKING\_MODE (vertical blanking) is set to 0x0. In this configuration, data lanes transit into LP state during blanking. HSS packets are sent at every beginning lines blanking. The total number of lines blanking set in DSI\_VM\_TIMING2 (VSA+VFP+VBP) can be counted.



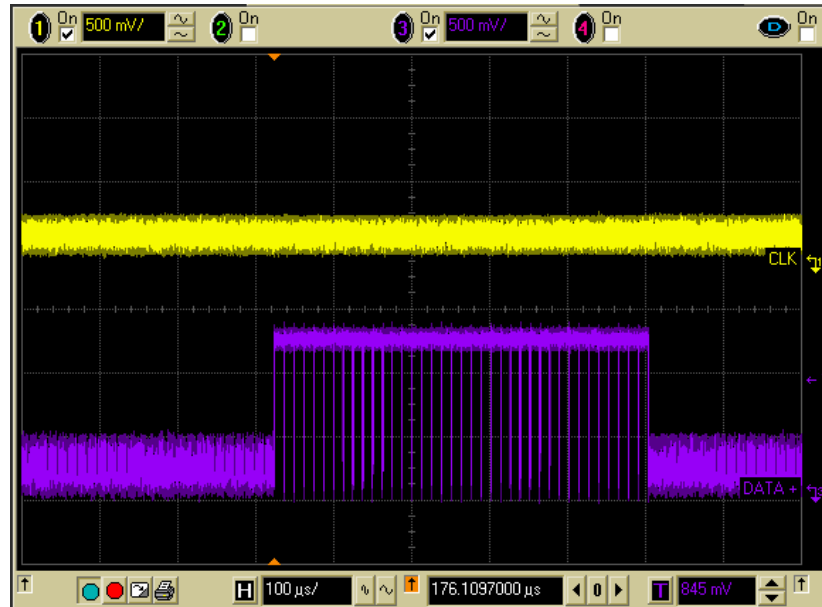


Figure 8: **BLANKING\_MODE= 0x0**

Figure 9 represent the lasts VACT lines transmitted before starting the vertical blanking in LP.

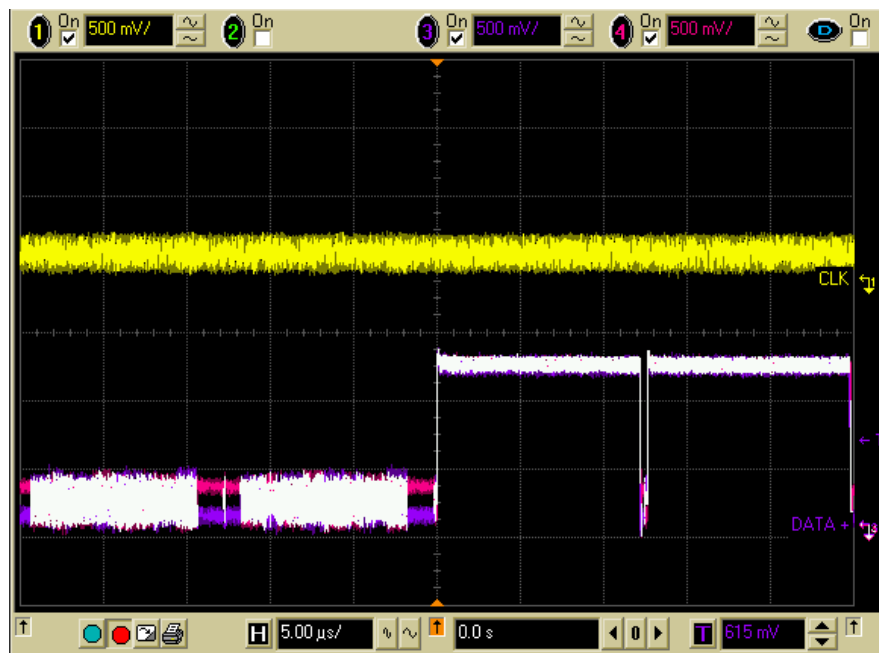


Figure 9: last lines transmitted before vertical blanking when **BLANKING\_MODE=0x0**

## 2.2 Non-continuous clock mode.

As mention in MIPI Alliance Specification for Display Serial Interface Version 1.02.00 “All DSI transmitters and receivers shall support continuous clock behavior on the Clock Lane, and optionally may support non-continuous clock behavior. A DSI host processor shall support continuous clock for systems that require it, as well as having the capability of shutting down the serial clock to reduce power.”

Figure 8 and Figure 9 show a continuous clock, not stopped even if data lanes transit in LP. In this configuration, DDR\_CLK\_ALWAYS\_ON bitfield in DSI\_CLK\_CTRL[13] is set to 0x1.

OMAP supports non-continuous clock by setting to 0x0 the bitfield DDR\_CLK\_ALWAYS\_ON in DSI\_CLK\_CTRL[13]. This setting allows the DDR\_CLK to be cut when no HS transmission is needed. In a video mode configuration with all blanking mode set to 0x1, the DDR\_CLK will be cut at least once per frame as shown in Figure 10 and Figure 11.

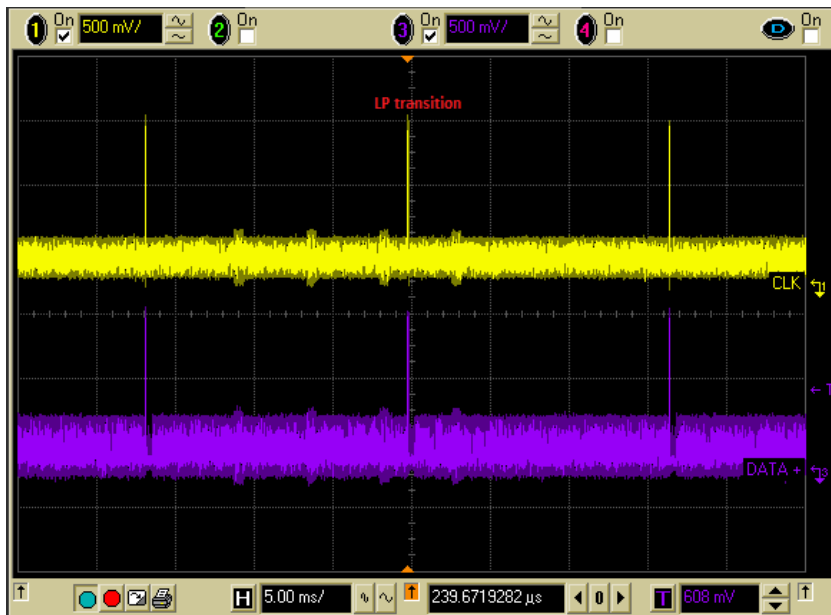


Figure 10: DDR\_CLK\_ALWAYS\_ON = 0x0 and all Blanking mode set to 0x1

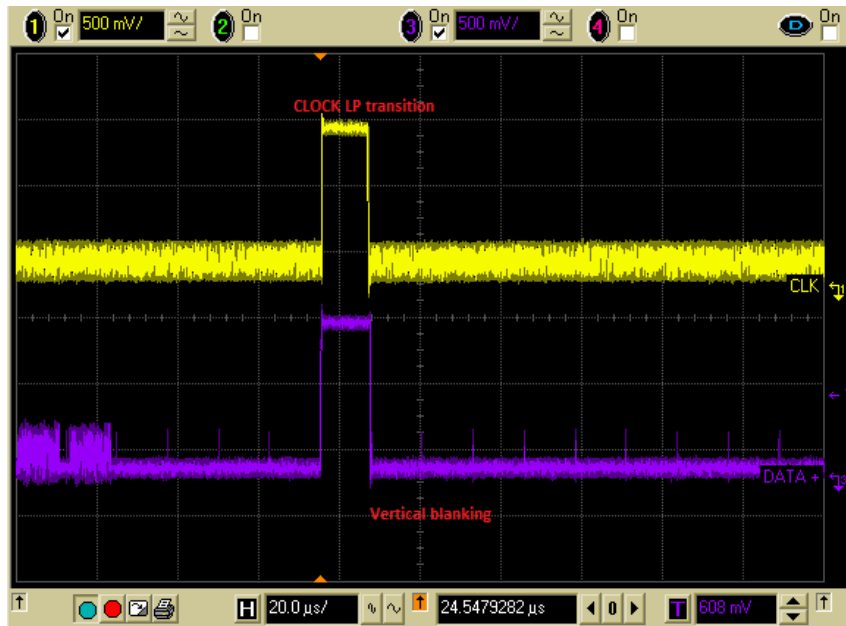


Figure 11: Zoom on vertical blanking when `DDR_CLK_ALWAYS_ON = 0x0` and all Blanking mode set to `0x1`

However, extra `DDR_CLK LP11` state can be achieved if the vertical and horizontal blanking mode are set to `LPS`, as shown in Figure 12, for more details on blanking mode refer to section 2.1.



Figure 12: `DDR_CLK_ALWAYS_ON = 0x0` and `BLANKING_MODE = 0x0`

It is the user responsibility to verify that enough time is available to transition from `HS` to `LP` back to `HS` for both data and clock lanes.

## 2.3 Interleaving.

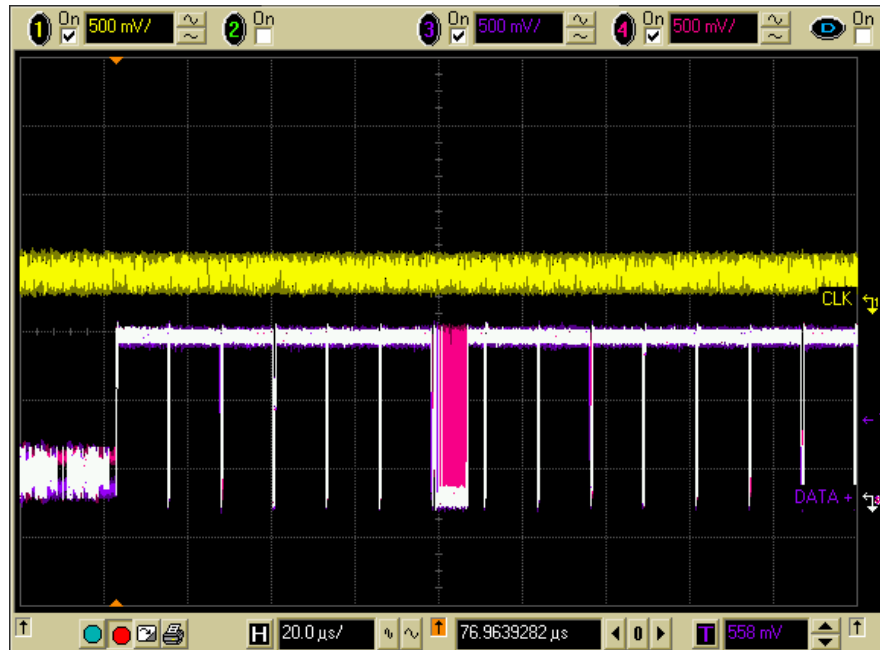
It is possible to interleave DCS write and/or read command, BTA during the blanking period using a different VC than the video one (usually VC0). The minimum interleaving period is one line blanking as the data lanes will transit at least once per frame in LP. To increase the interleaving periods, user should set `BLANKING_MODE` to 0x0. Interleaving during horizontal periods is not recommended as period is short. In the case LP transition is possible during horizontal periods and interleaving is considered for the vertical period then it is necessary to lock interleaving during the horizontal period, the user should set `HSA_HS_INTERLEAVING`, `HFP_HS_INTERLEAVING` and `HBP_HS_INTERLEAVING` `DSI_VM_TIMING4[23:0]`, `HSA_LP_INTERLEAVING`, `HFP_LP_INTERLEAVING` and `HBP_LP_INTERLEAVING` `DSI_VM_TIMING5[23:0]` to 0x0.

To control the duration of interleaving, the user can limit the number of packet sent in LP or HS during a vertical blanking period by setting `BL_HS_INTERLEAVING` and/or `BL_LP_INTERLEAVING` `DSI_VM_TIMING6[31:0]`.

The next figures show a NOP DCS command sent, in LP or HS, interleaved into the vertical blanking. The write into the VC1 TX FIFO does not occur at a specific time, meaning the packet is sent on the next line blanking available.

Figure 13 shows a DCS NOP command interleave during a LP vertical blanking.

As shown in Figure 14, once the HSS packet is sent DSI lanes transit into LP11 and a Low Power Data Transmission (LPDT) command is sent then followed by the short packet NOP DCS command.



**Figure 13: DCS NOP command sent in LP during vertical line blanking**

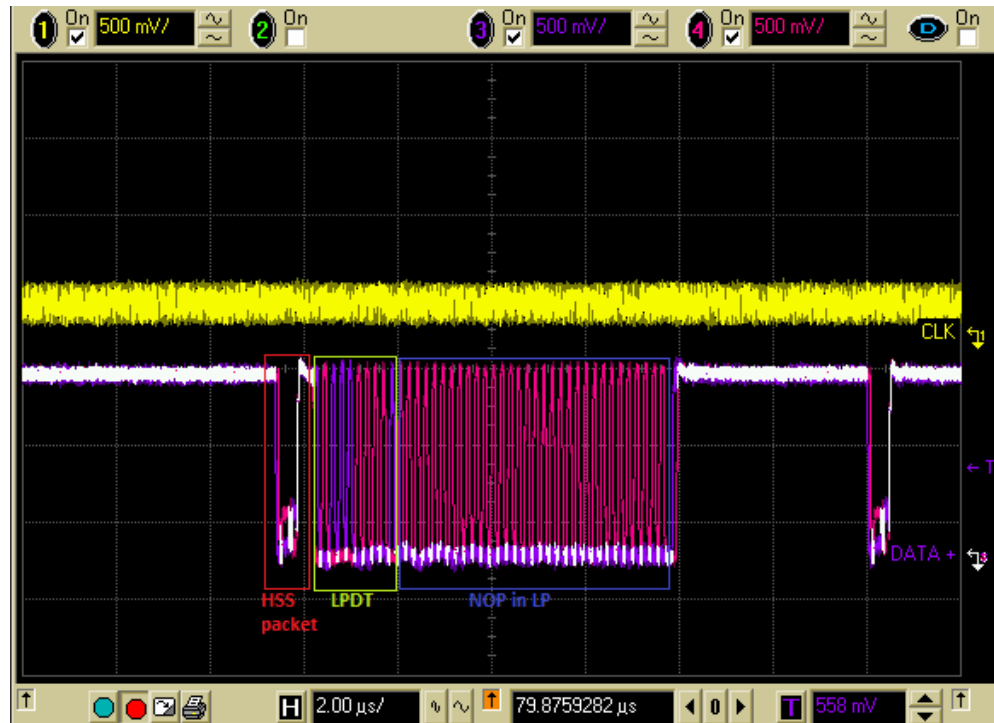


Figure 14: Zoom of DCS NOP command sent in LP during vertical line blanking

Figure 15 demonstrates a NOP DCS command sent in HS interleaved followed by a BTA in the LP vertical blanking. OMAP checks the presence of packets in the TX FIFO at the beginning of the blanking period, this results in NOP DCS command sent back to back with the HSS sync packet. There is no transition to LP between the 2 packets.

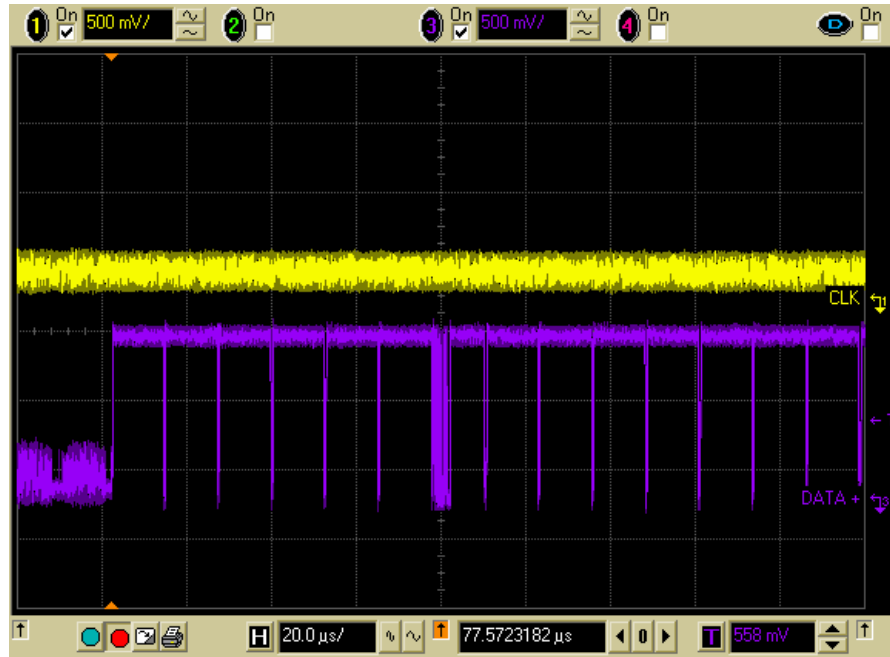


Figure 15: HS NOP DCS command followed by BTA during a vertical line blanking

Once DCS NOP packet is sent a BTA is done to obtain an ACK message from the panel. Following the ACK trigger, the panel returns DSI link to host by a BTA as shown in Figure 16.

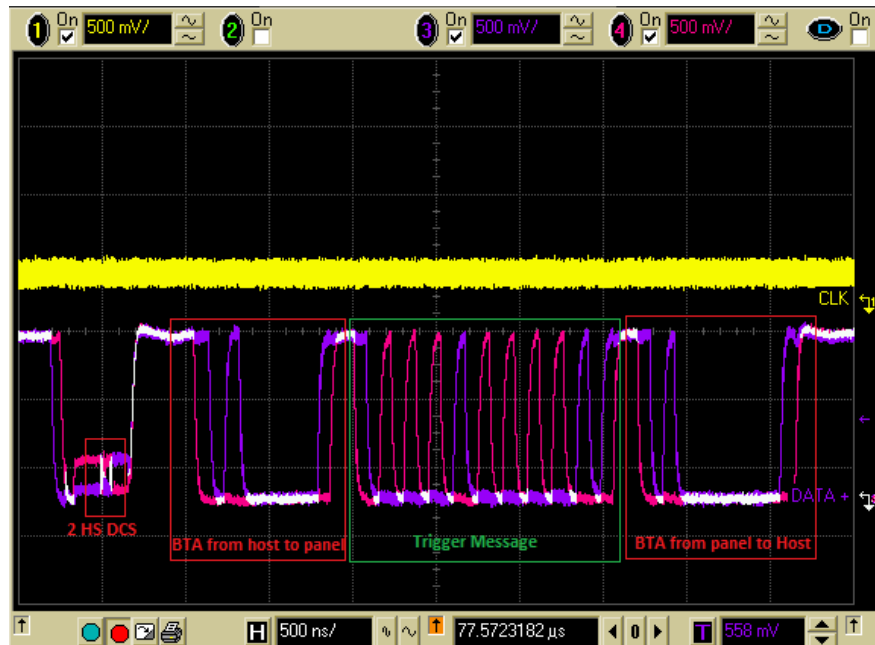


Figure 16: Zoom of HS NOP DCS command followed by BTA during a vertical line blanking

A BTA will end the transmission from host to panel during the current line blanking, meaning no other packets will be sent on DSI link after the BTA until the next line blanking starts, even if time is available in the current blanking. Only ACK trigger or read packet from panel to host could happen after the BTA. Figure 17 represents 2 HS commands wrote back to back in the TX FIFO followed automatically by a BTA once sent (BTA\_SHORT\_EN bit DSI\_VC\_CTRL\_i[2]set to 0x1).

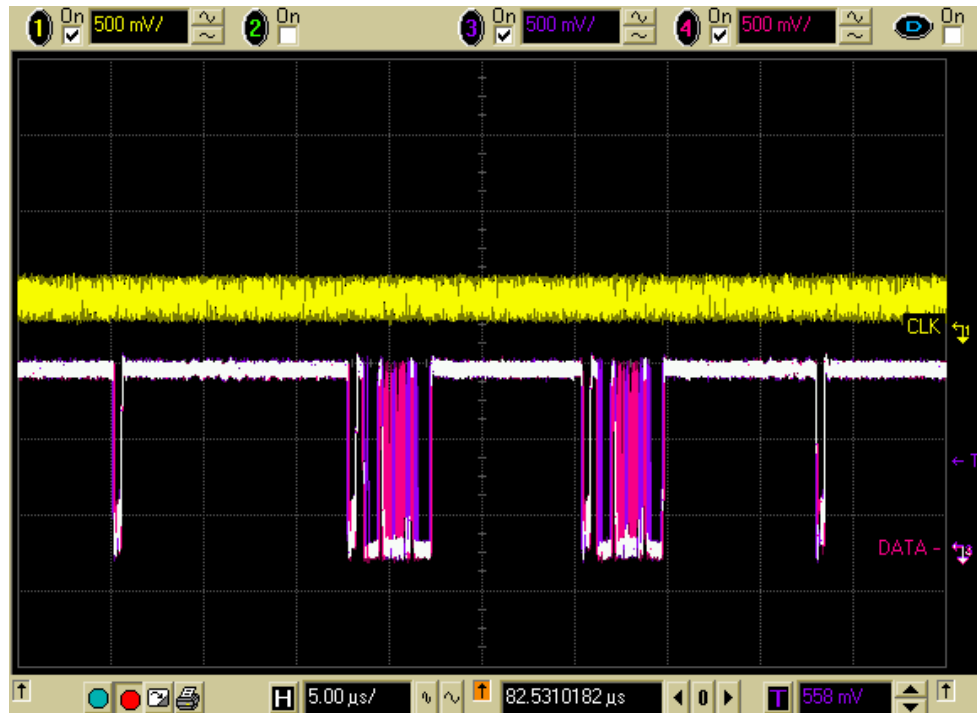


Figure 17: 2 HS DCS command with BTA

When performing a DCS read on the panel, It is the user responsibility to ensure that there is sufficient time to sent the DCS read command (HS or LP), perform a BTA, receive short or long packet from panel (LP only) and restore the DSI link to host by a final BTA within the same line blanking. The overall protocol when performing a read request on the panel is resumed in Figure 18.

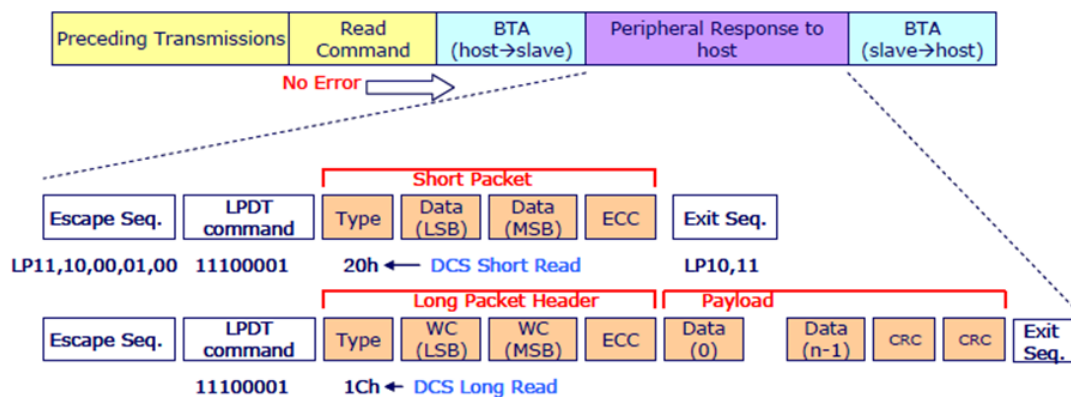


Figure 18: Protocol view of a read request when no error

Figure 19 and Figure 20 illustrate a working read with a DCS short read as feedback from panel.

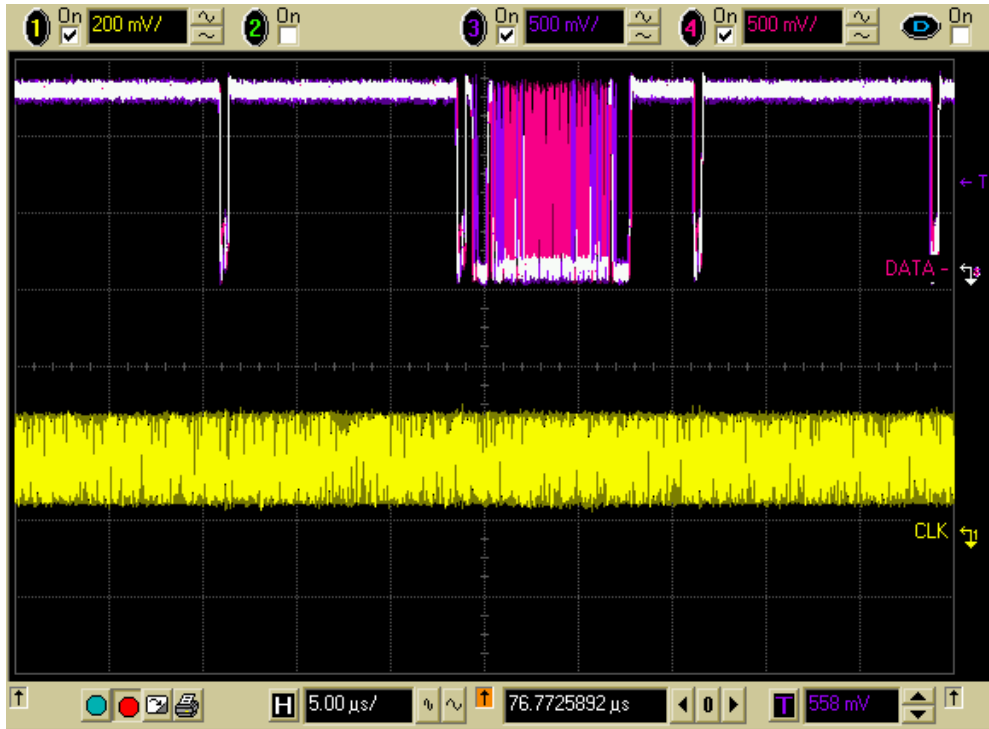


Figure 19: Read request perform during vertical line blanking

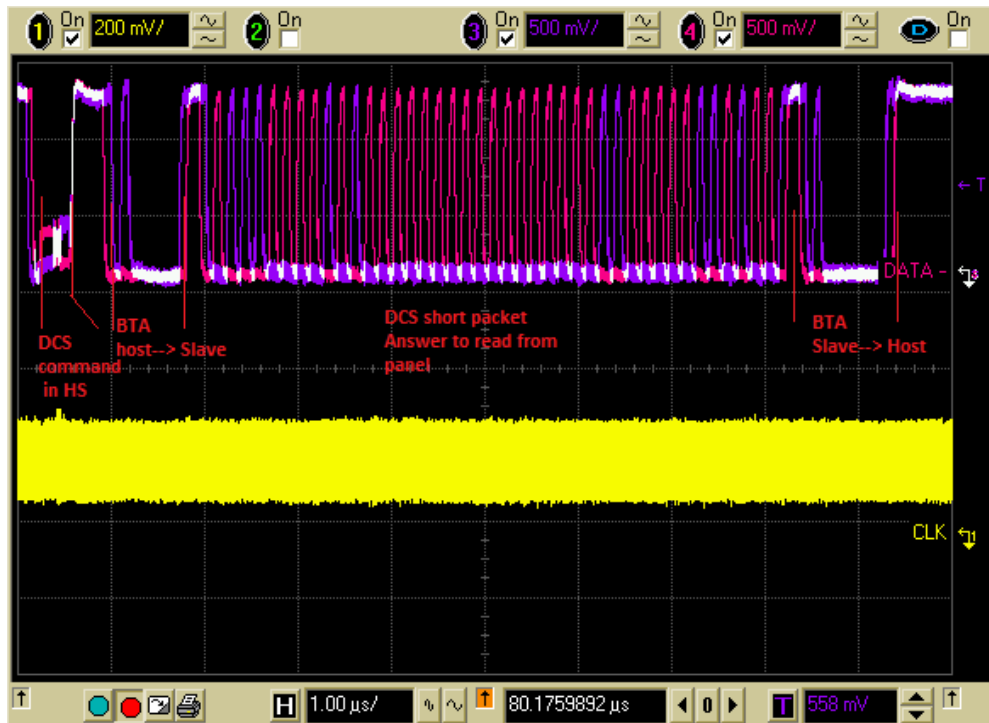


Figure 20: Zoom on a Read request perform during vertical line blanking



Figure 21 shows a configuration where Host send in LP a read request on the ROM panel and data return from panel is a long packet. This overall read request exceeds the duration of a line blanking (approx 12.5us) causing the override of the next HSS sync packet. OMAP recovers this misalignment however this configuration is violating the MIPI DSI standard and could cause a lost of synchronization on panel side. It is the user responsibility to ensure that there is sufficient time to perform the read request within a line blanking, if not possible then the read access should be perform with video mode disable.

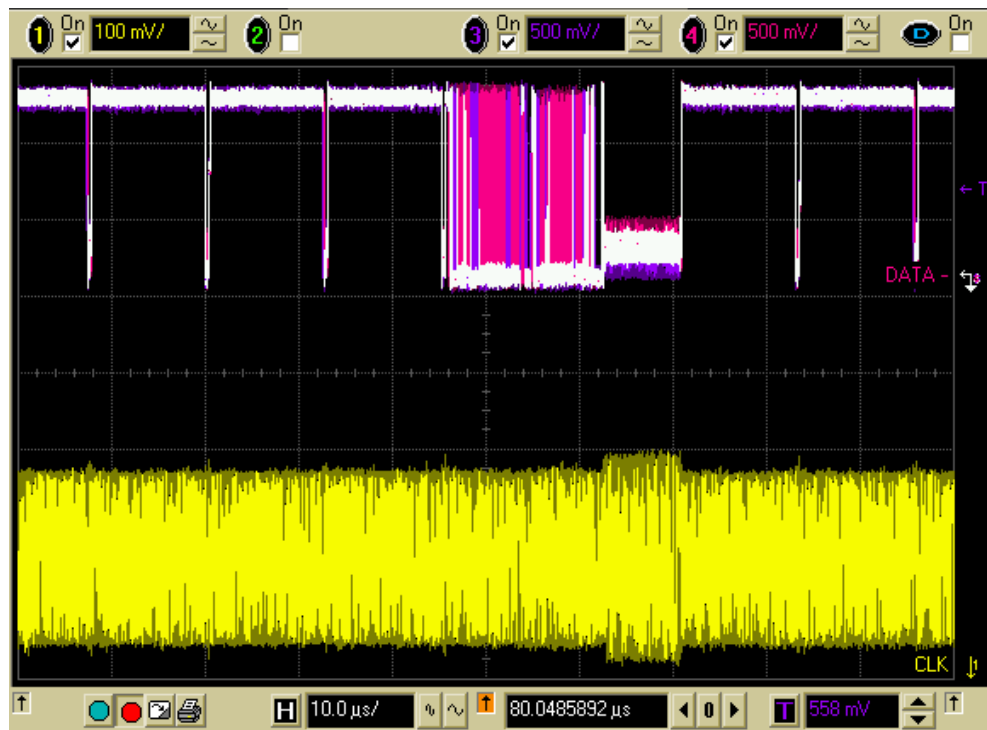


Figure 21: Read request exceeding vertical line blanking

### 3 DSI command mode

#### 3.1 Tearing Effect (TE) control

A command mode display has its own timing controller and memory frame buffer. In order to avoid tearing effect it is needed to notify the host of timing events on the panel. The sending of the pixel data in a command mode can be achieved in 3 different manners:

- Automatic mode: The SW starts the transfer when it is needed by setting to 0x1 the TE\_START bit in DSI\_VC\_TE\_i[31](TE\_EN should be set to 0x0 in DSI\_VC\_TE\_i[30]). TE\_START is HW cleared once transfer is finished. It lets SW start the transfer manually based on application events or based on the TE trigger interrupt (TE\_TRIGGER\_IRQ). If no synchronization is done, then some tearing effect could appear.

- DSI PHY TE trigger: MIPI DSI standard defines a TE trigger message which is conveying from panel to host through the DSI link. Once the trigger is received the pixel data is automatically started.
- CMOS TE line: This synchronization method is not part of the MIPI DSI standard but it is supported by OMAP. The pixel data transfer will start automatically when the pre-defined event will happen on the TE CMOS line. 2 TE CMOS lines are available on OMAP. One TE CMOS line can start a transfer onto 1 or more VC channels.

For a complete description of the programming sequence of each mode, please refer to the OMAP Technical Reference Manual.

### 3.1.1 DSI-PHY TE trigger

At host side, to enable DSI-PHY TE trigger, DSI\_VC\_TE\_i[30] TE\_EN bit is set and DSI\_VC\_TE\_i[29] TE\_LINE bit is reset. In this configuration the hardware must use the TE PHY trigger to start the transfer of the data from the related VC. TE\_EN is reset when all the data are sent to the peripheral. Other parameters need to be configured before trigger message occurs like size of packet, headers, all details are available in the OMAP Technical Reference Manual.

On the panel side, set\_tear\_on and set\_tear\_scanline DCS commands are sent to the panel to enable DSI-PHY TE trigger.

At protocol level once configuration is done, the Host should give the bus possession to the panel in order to perform the TE-reporting. This is done by performing a BTA, refer to Figure 22. After the sending of the TE trigger, the panel returns bus possession to the Host to convey the pixel data, refer to Figure 23 and Figure 24.

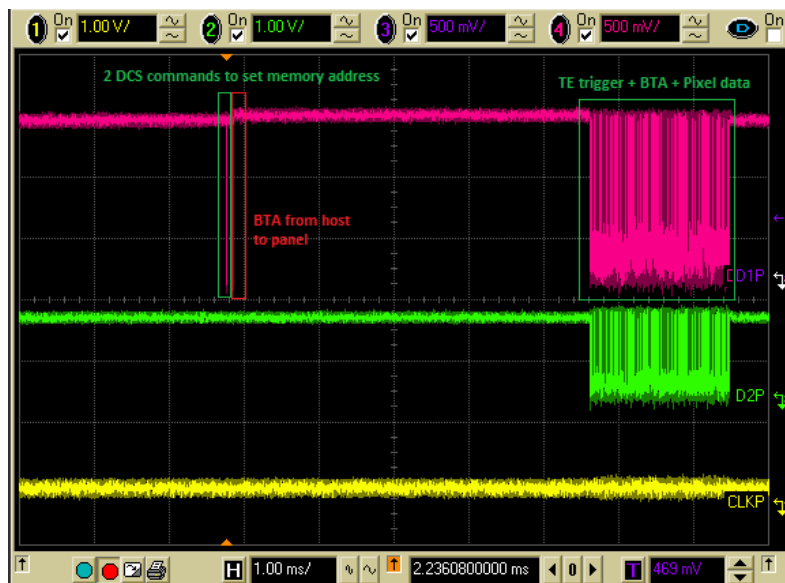


Figure 22: Complete sequence of DSI-PHY TE trigger

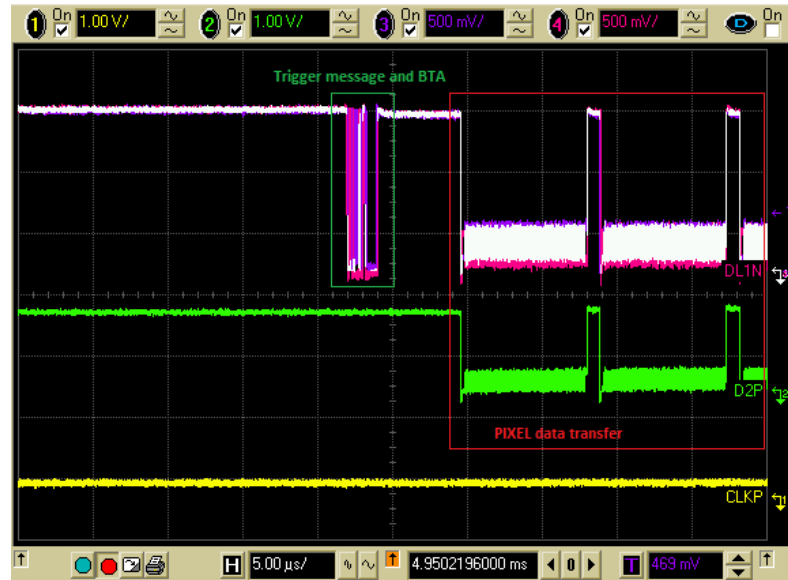


Figure 23: Start of transfer after TE trigger message

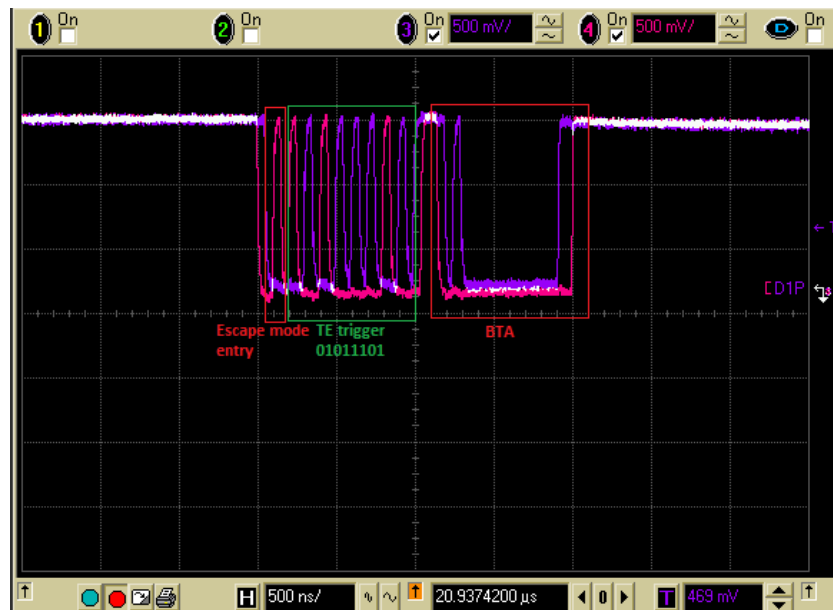


Figure 24: TE trigger message from panel and BTA from panel to Host

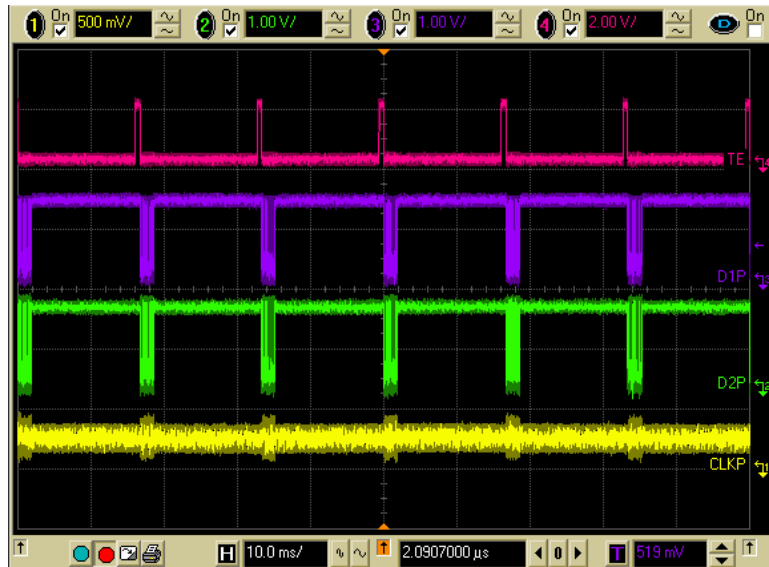
### 3.1.2 CMOS TE line

This mode is not part of the MIPI DSI standard and available on OMAP.

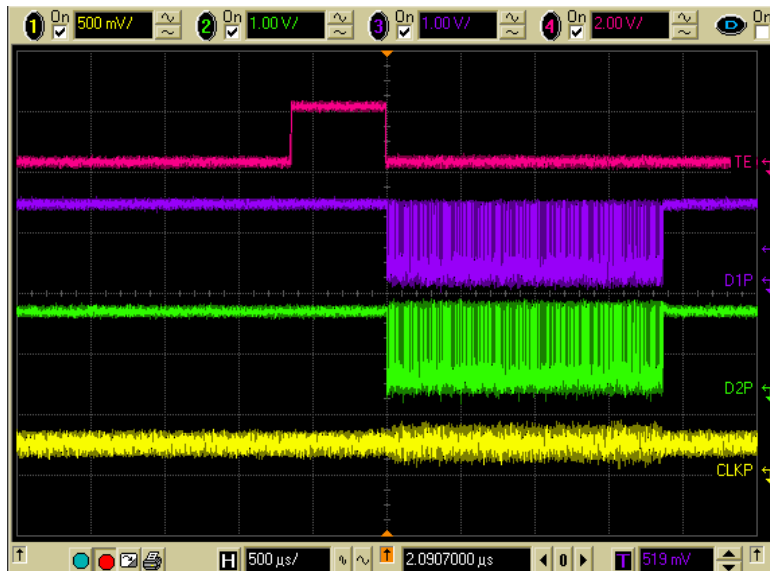
At host side, DSI\_VC\_TE\_i[31:30] TE\_EN and TE\_LINE bit are set to enable CMOS TE line. Then based on the feature available on the panel, it is possible to start a transfer on a vertical synchronization event or on a number of horizontal synchronization event using DSI\_TE\_VSYNC\_WIDTH\_j, DSI\_TE\_HSYNC\_WIDTH\_j, and DSI\_TE\_HSYNC\_NUMBER\_j registers, for more details refer to the OMAP Technical Reference Manual.

At the panel side, depending on the type of feature available, SW should enable the TE line and configure the type of event generated on this TE line (vertical or horizontal synchronization event) by sending DCS command as stipulated in the panel specification.

Figure 25 illustrates a CMOS TE line configuration. Panel is configured to generate a positive pulse on each vertical synchronization and host is set to start the transfer on it. Frame rate is approximately 60 Hz (16ms) and driven by the panel.



**Figure 25: TE line trigger at 60Hz**



**Figure 26: Full frame transfer after TE line trigger**

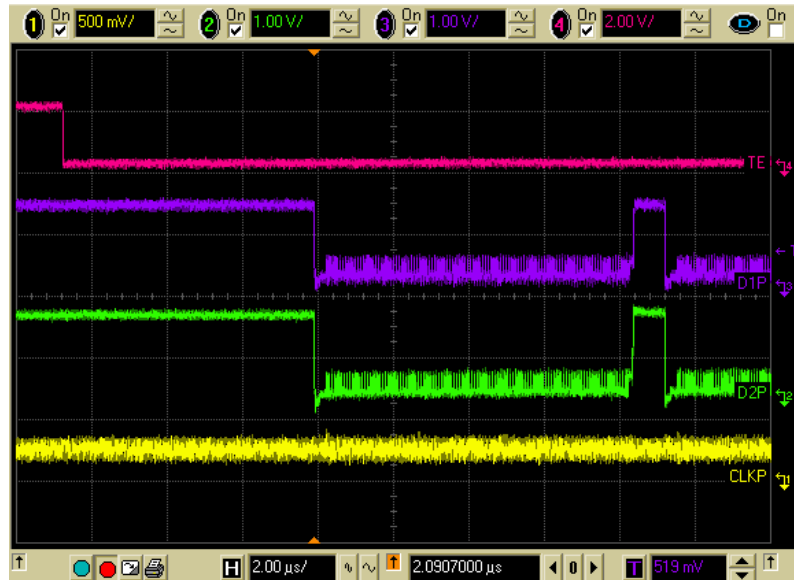


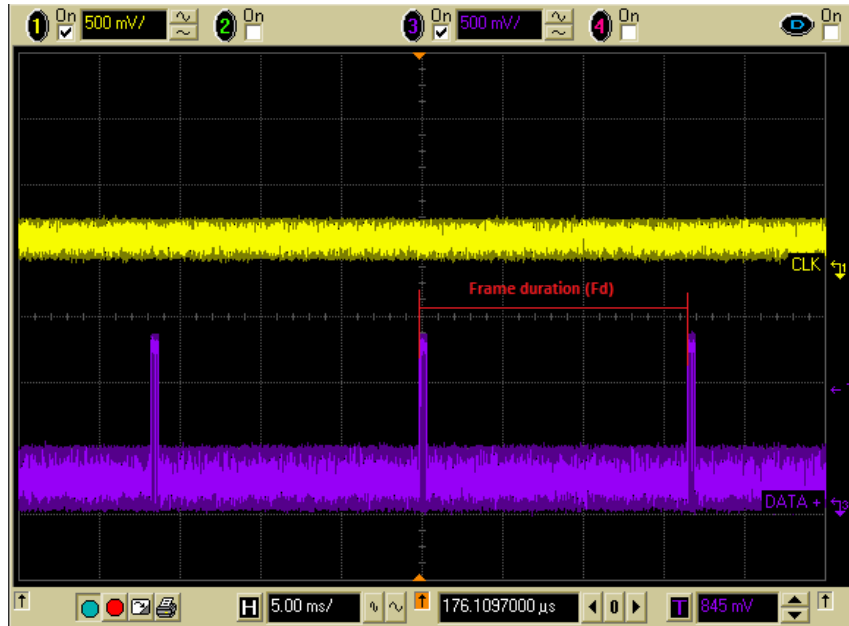
Figure 27: Delay between TE trigger and 1st line transfer

## 4 Tips and debug

### 4.1 Basic measurements

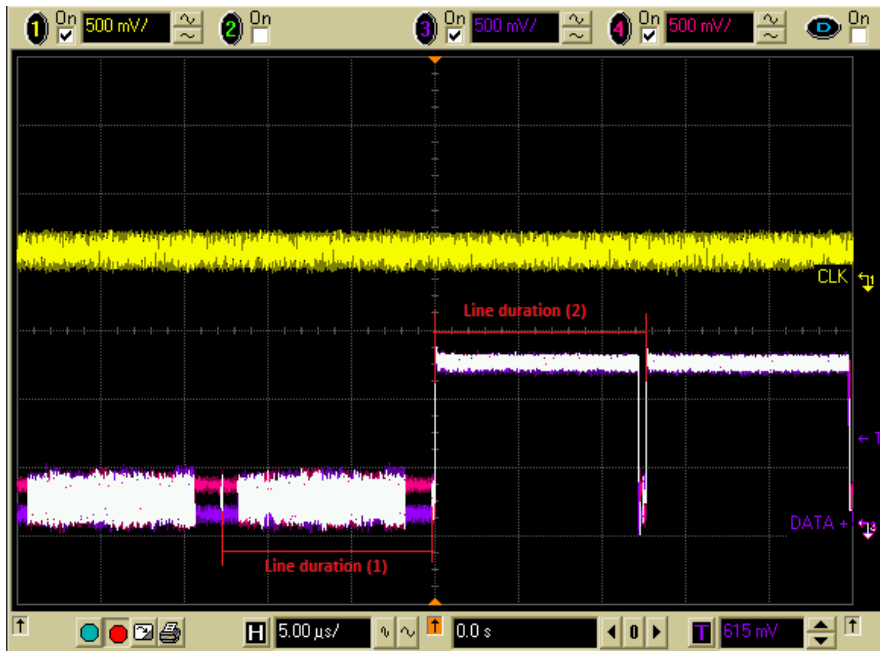
- Frame rate (FPS) or frame duration (Fd): To measure exact frame rate on a DSI video mode panel, you must measure the duration Fd between 2 vertical blanking period as shown in

$$FPS = \frac{1}{Fd}$$



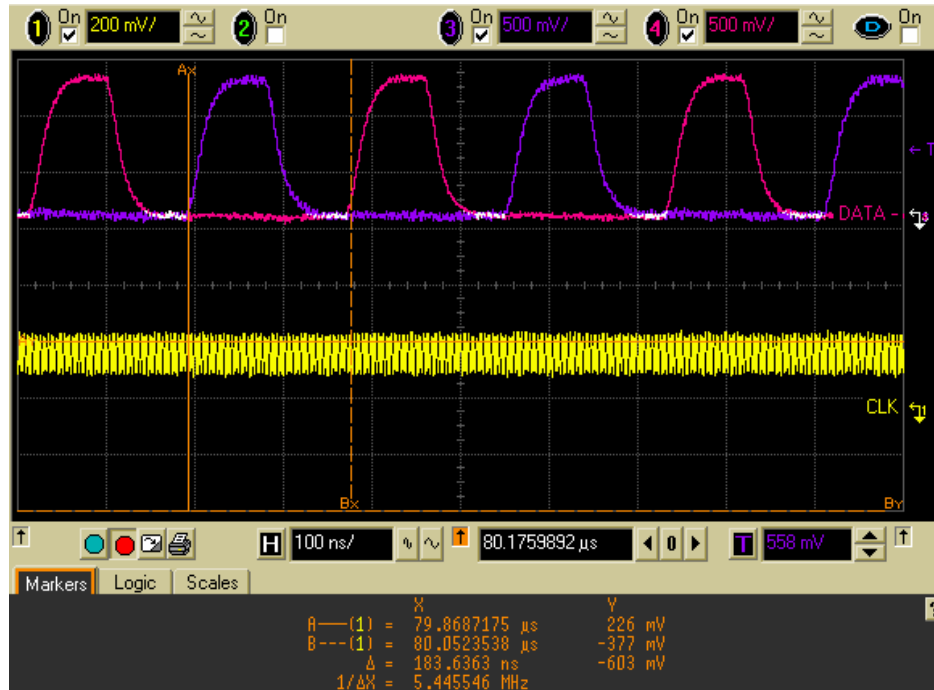
**Figure 28: Frame duration measurement**

- Line duration (TL): To measure a line duration, 2 options are available:
  - Measure the duration of an active line (VACT) as shown in (1) of Figure 29.
  - Measure the duration of line blanking period during vertical blanking as shown in (2) of Figure 29.



**Figure 29: Line duration measurement**

- LP clock (LP CLK): The LP clock can be reconstructed by doing an EXOR of the Dp and Dn. To measure it you will need a LP period either by performing a BTA for trigger message or by sending a DCS command in LP. Both Dp and Dn signal are superposed to reconstruct the clock as shown Figure 30. Figure 30 is a zoom of a LPDT between Host and Panel.



**Figure 30: LP clock measurement**

- HS clock (HS CLK): HS clock is approximately measured by performing a probing of CLKp or CLKn signals, as shown in Figure 31.

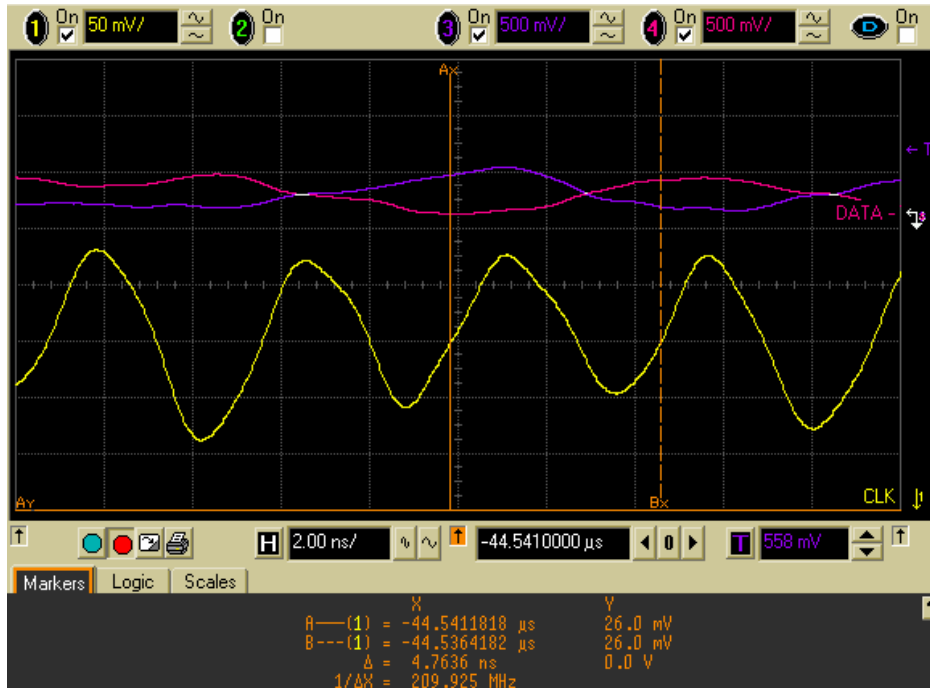


Figure 31: HS measurement

## 4.2 Basic decoding using an oscilloscope

### 4.2.1 LP transfer Decoding using an oscilloscope

LP transfer is done using the Escape mode. Escape mode is a special mode of operation for data lanes using low power-states.

Escape mode is supported in forward direction (from host to panel) and optionally in the reverse direction (from panel to host). Data lanes are in escape mode as soon as the escape mode entry procedure is executed (LP-11, LP-10, LP-00, LP-01, LP-00). Once in escape mode, an entry command, as defined in the MIPI DSI standard, is sent by the Tx. The PHY in Escape mode shall apply Spaced-One-Hot bit encoding for asynchronous communication. Therefore, operation of a Data Lane in this mode does not depend on the HS Clock.

Figure 32 shows a complete LPDT procedure.



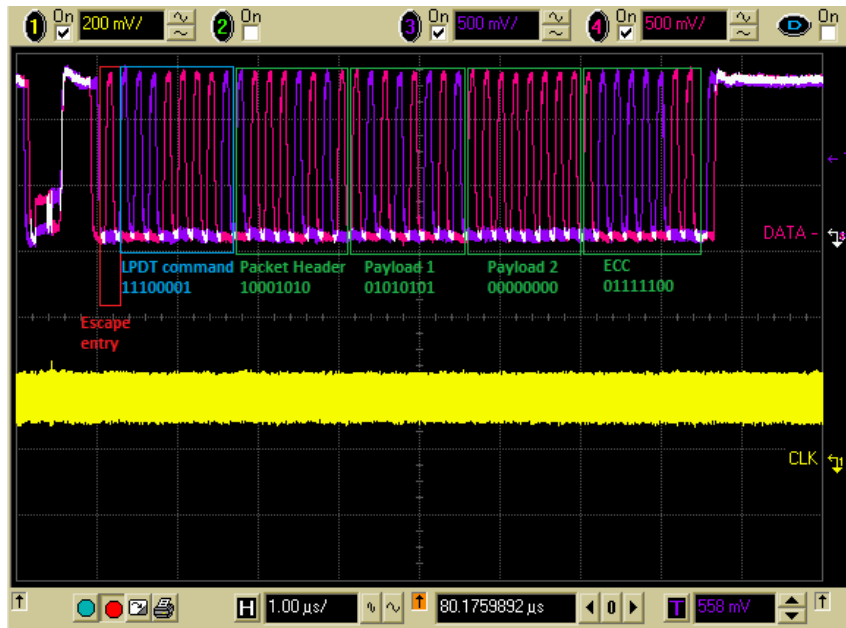


Figure 32: LP data transmission

Figure 16 shows a LP transfer from panel to host; the escape mode entry is included in the trigger message and the command is a trigger message, ACK.

#### 4.2.2 HS transfer Decoding using an oscilloscope

This section presents basic method to decode a HS packet or verify DSI timing for HS transmission. This approach is not meant to decode a complete frame line, as you will need numerous channels, be able to capture a complete line with a good resolution and be very precise in your sampling. This technique allows you to verify approximately HS timings, synchronization packets, presence of SoT and EoT packets and beginning of a pixel data in a line.

To perform the decoding a 4 channels oscilloscope is necessary, 2 for Dp and Dn and 1 for the clock. The oscilloscope should have a channel subtract mathematical function to determine the differential output.

Figure 33 illustrates a HS transmission, a HSS sync packet done during a vertical line blanking. The figure legend indicates the state and line condition of the Host as define in the MIPI standard. A zoom of the HS packets is provided in Figure 34. The green signal represents Dp minus Dn signal. The sampling of the data is done on peak+ and - of the clock signal as it is a Dual Data Rate (DDR) transmission. Once all bits values are identified, to reconstruct a byte you will need to swap LSB and MSB. LSB of a byte is first (on the left). For example HSS sync packet once sampled is 10000100, see Figure 33. After swapping LSB and MSB, byte becomes 00100001 where the 1<sup>st</sup> two bits represent the VC, VC0, and the last 6bits are the data type, 100001 HSS sync packet.

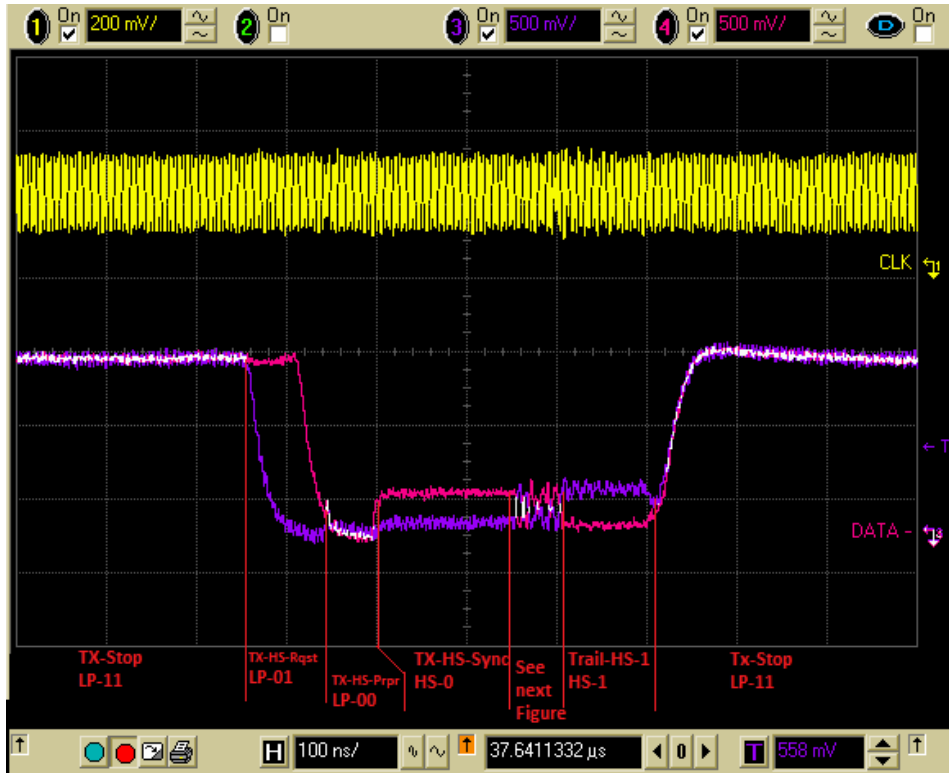


Figure 33: High-Speed Data Transmission

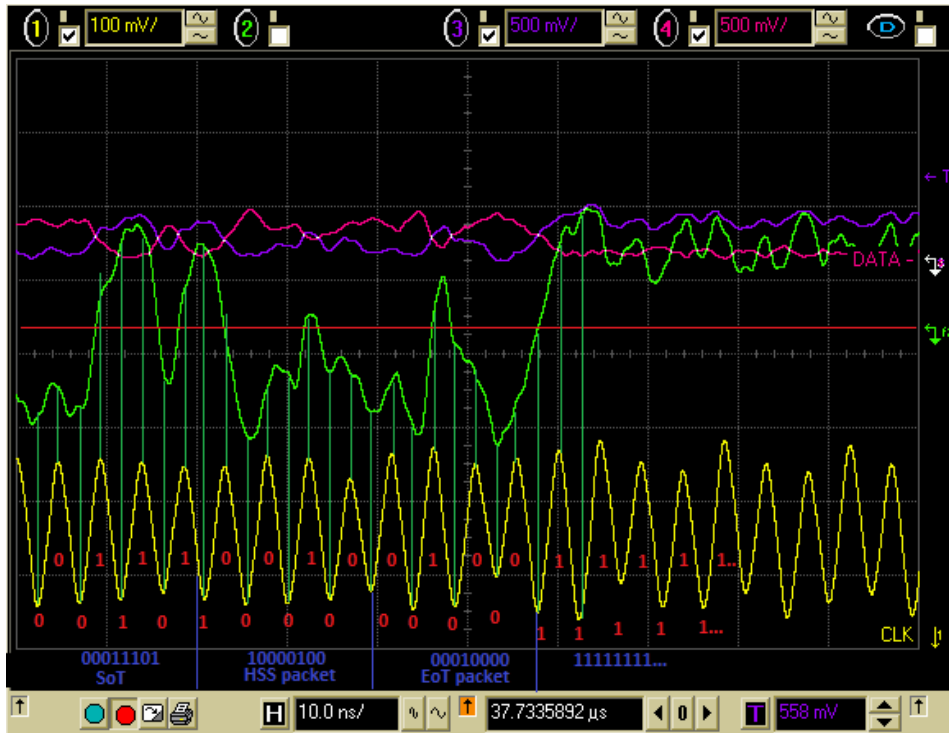


Figure 34: Decoding of HS packet (HSS sync packet)

### **4.2.3 Determine all clocking and timings of the Display subsystem**

2 excel sheets, DSI timings extractor OMAPx.xlsx, are attached to the APN through the paper clip to help user determine all DSS timings and clocking values. User should enter all register settings in the OMAPx DSI configuration sheet and check the result of the timings and clock values in sec or MHz in the Timings and clocks settings.

## Appendix A. Display Subsystem configuration

### Video mode:

The following configuration was used on OMAP5 Test Evaluation Board (TEB). The registers in setting of the DSI PE, PHY, PLL and DISPC are available in the excel sheet attached in the paper clip.

### Command mode:

The configuration used is identical to the blaze with an android release, except it was migrated on an OMAP4 TEB.

## References

1. *MIPI Alliance Specification for Display Serial Interface Version 1.02.00 – 28 June 2010*
2. *MIPI Alliance Specification for D-PHY Version 1.02.00 – 28 June 2010*
3. *OMAP543x ES1 Technical Reference Manual version K*

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