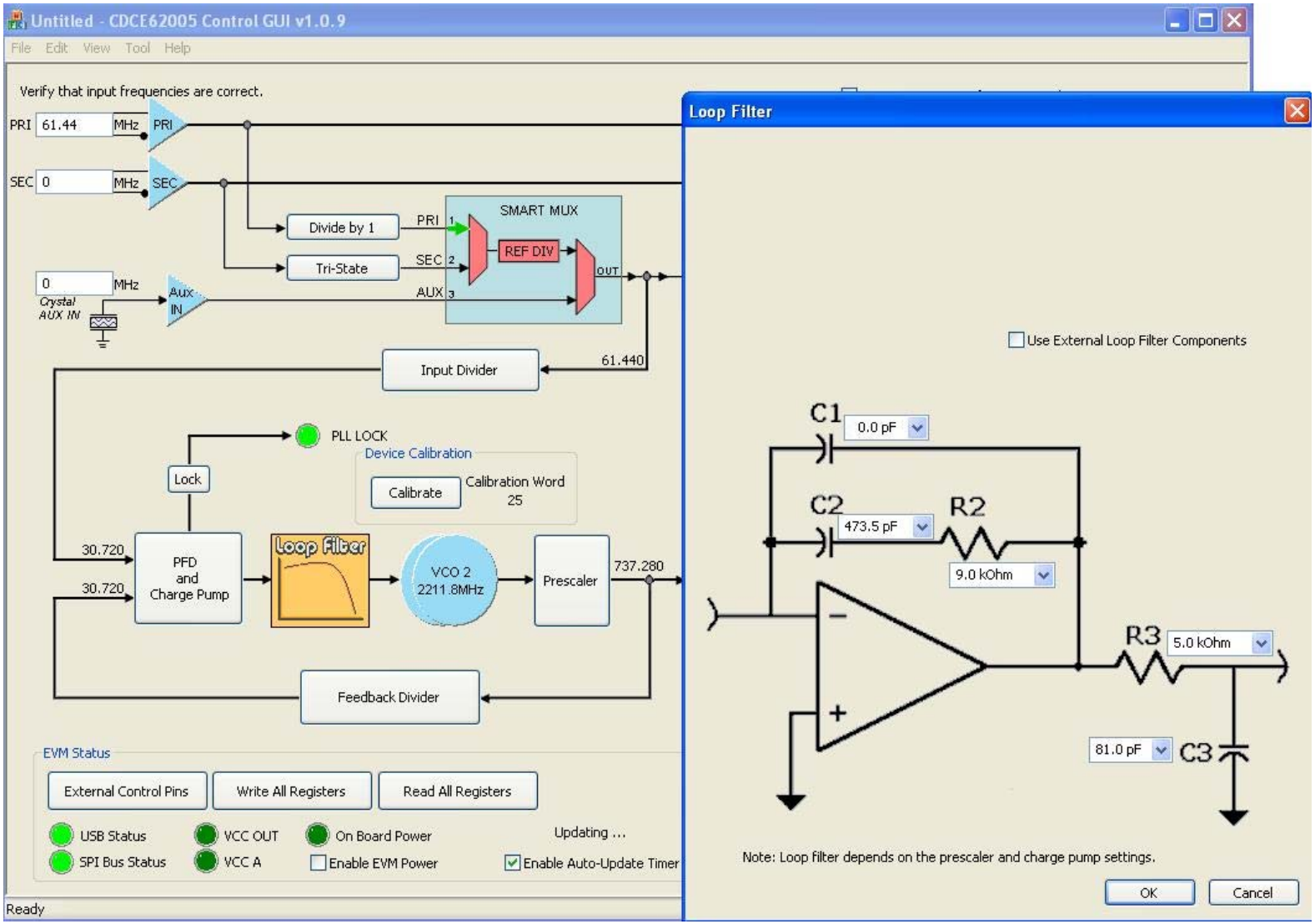
CDCE62005 Test Results

CDCE62005 Configuration

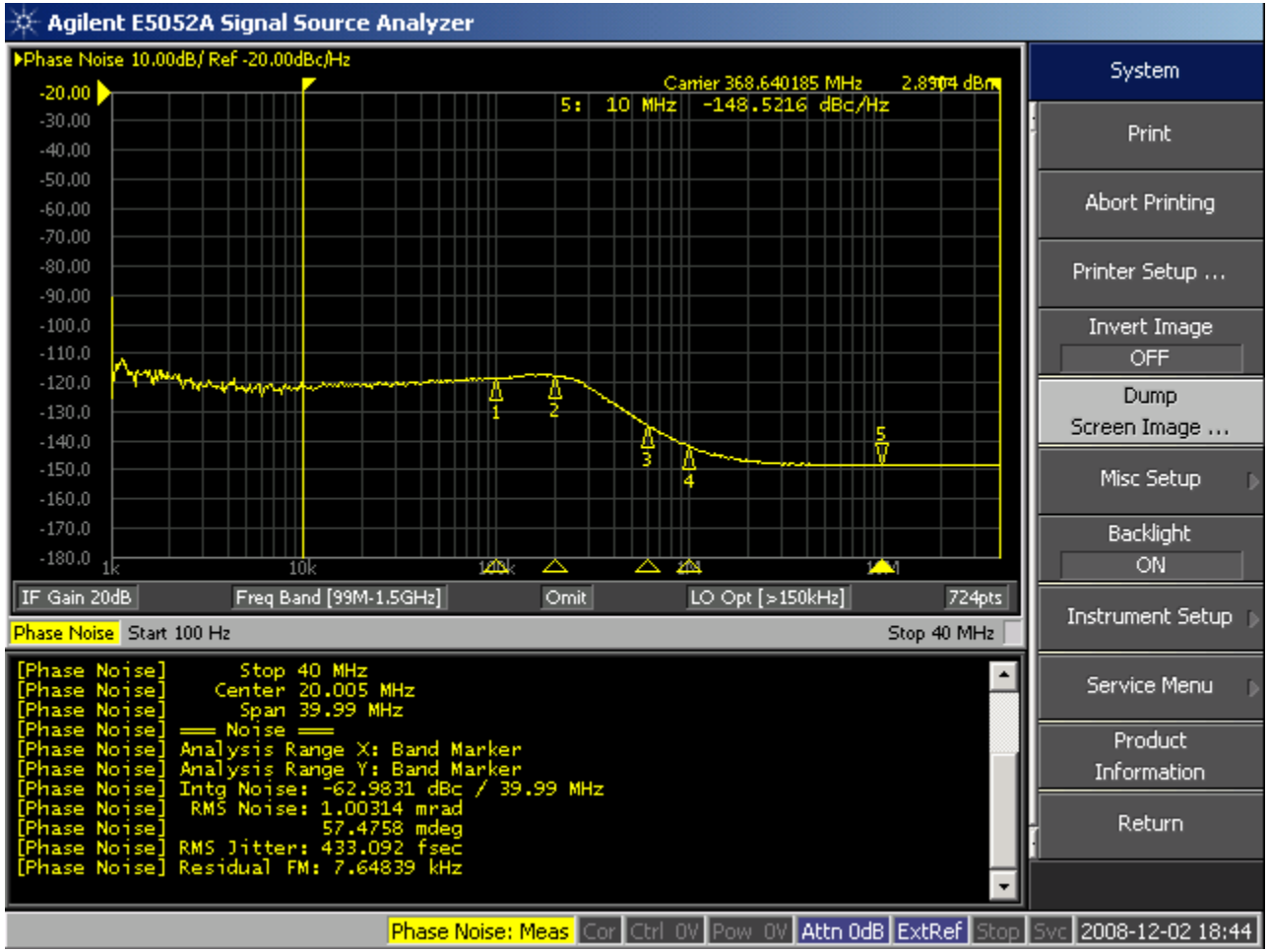
- Input = 61.44MHz LVPECL
- Output = 368.64MHz LVPECL (U2), 184.32MHz LVPECL (U1), 122.88MHz LVPECL (U0)
- Loop Filter = Internal (see next page for topology)
- Charge Pump = 300uA
- VCO Frequency =2211.84MHz (VCO2)
- PLL Settings: Input Divider = 2, Prescaler Divider = 3, Feedback Divider = 24, Output Divider0 = 6, Output Divider1 = 4, Output Divider2 = 2
- Target Phase Noise: < -145dBc/Hz at 1MHz offset

CDCE62005 Configuration



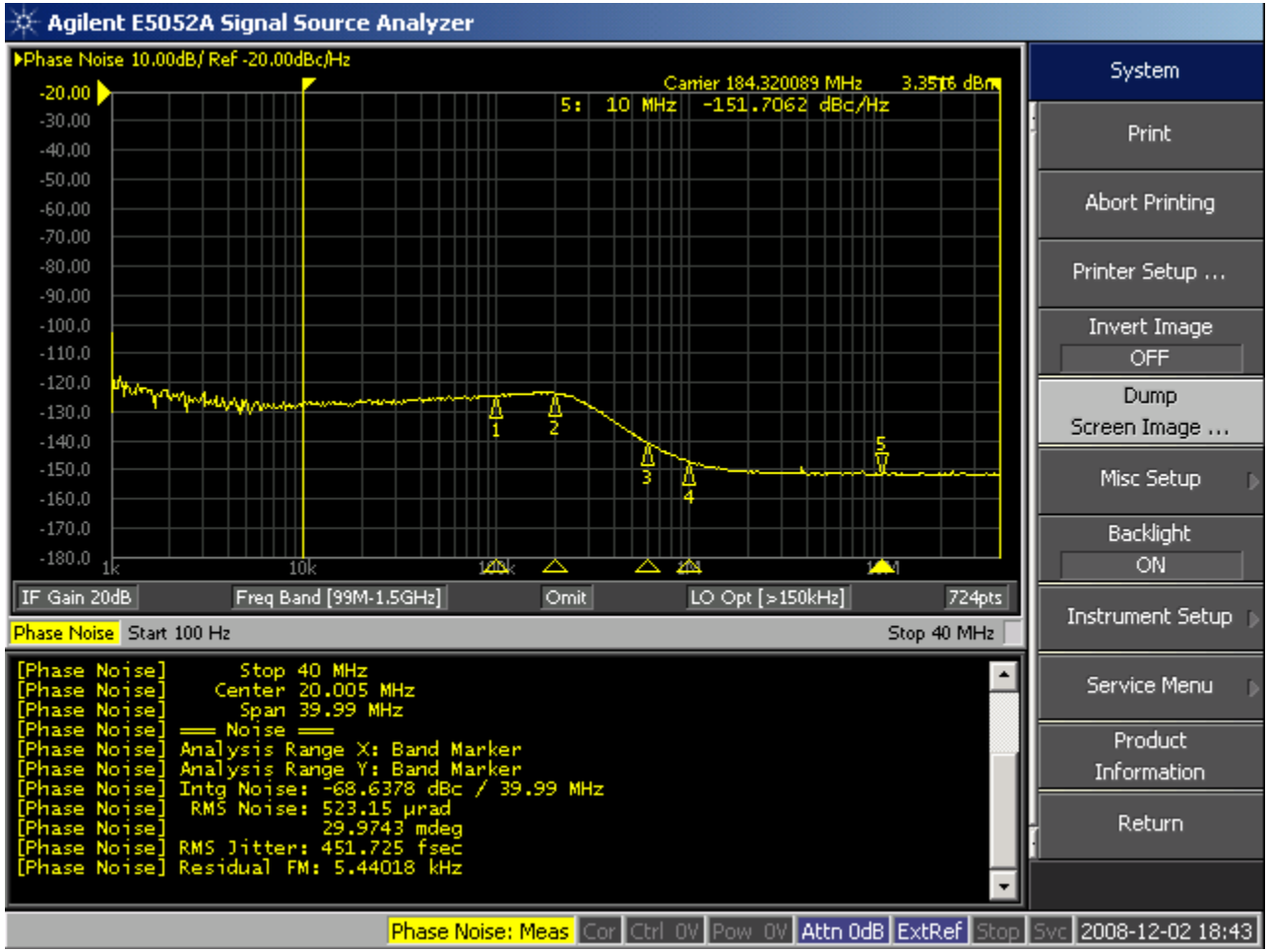
368.84MHz Output Phase Noise

Phase Noise = -143dBc/Hz at 1MHz offset



184.32MHz Output Phase Noise

Phase Noise = -148dBc/Hz at 1MHz offset



122.88MHz Output Phase Noise

Phase Noise = -150dBc/Hz at 1MHz offset