Board Layout & Design for EMI

EMI Best Practices

- **PCB Design Guidelines**
  - Minimize ground loop areas
  - Route differential pairs close together
  - Use 100ohm coupled differential pairs
  - Minimize impedance discontinuities
  - Minimize skew within the pair
  - Keep stubs as short as possible
  - Minimize the number of vias
  - Solid ground and power planes
  - Sufficient decoupling capacitors on chip power supplies
  - Keep digital and analog lines separate

- **Signal Integrity**
  - Reduce crosstalk noise and jitter
  - Minimize Power/Ground bounce (noise)
  - Controlled edge rate of 2ns for single-ended signals to minimize signal reflections
  - Optimize Host to Serializer signal drive strength (low drive) to avoid over/undershoot and extremely fast edge rates; maintain only clock fast edge for low jitter

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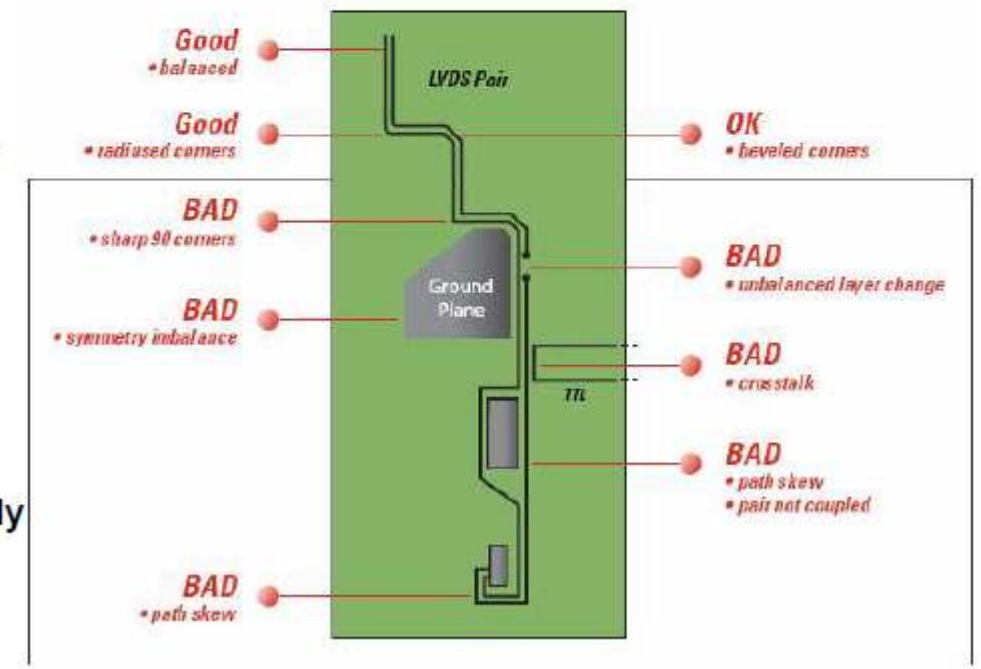
PCB Guidelines

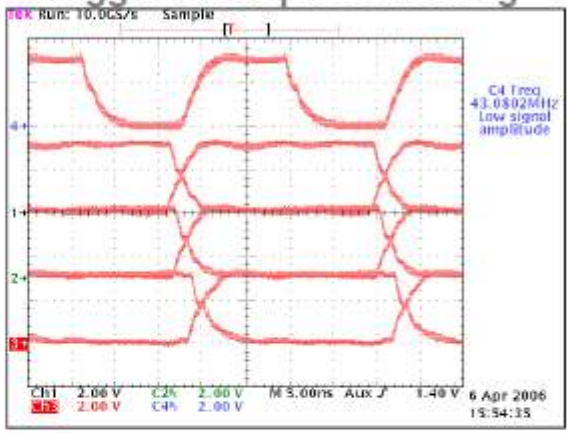
- ✓ Use at least a four-layer board with dedicated power and ground planes
- ✓ Use surface-mount components to minimize parasitics
- ✓ Separate a single-ended signal from a differential signal by at least three times the differential spacing
- ✓ Separate adjacent differential pairs by three times the intra-pair trace spacing
- ✓ If vias are required for high-speed data lines, be sure to place vias to ground next to the signal via for a constant return path for the signal
- ✓ Route all differential traces as 100Ω differential impedance transmission lines
- ✓ Route all single-ended signals as 50Ω impedance lines
- ✓ Route all power signals as wide as reasonably possible to minimize inductance
- ✓ Use connectors and cables that are designed for high-speed differential data
- ✓ Follow the typical connection diagrams found in the datasheet for power-supply filtering recommendations



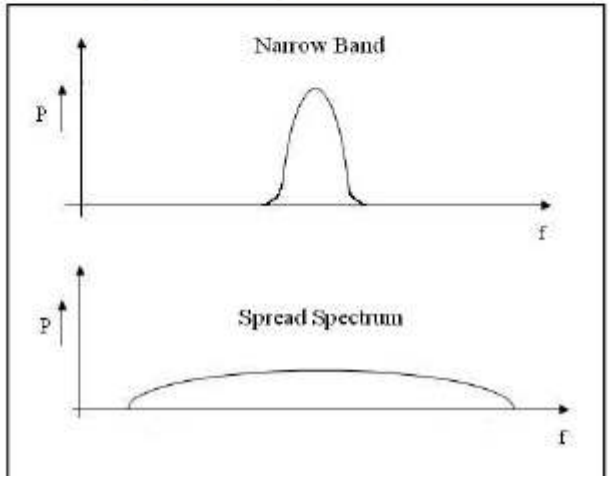
EMI Mitigation

- SER VOD select option
- Randomized, scrambled data on serial link
- DES Output is a wide Parallel Bus
  - RDS Feature (Receiver Drive Strength)
  - 1.8V VDDIO option
  - Staggered output switching (PTO)
- Configurable Spread Spectrum EMI reducing DES output feature
  - low freq spreading
    - Programmable mod rate
  - Center Spread
    - ±0.5%, ±1.0%, or ±2.0%

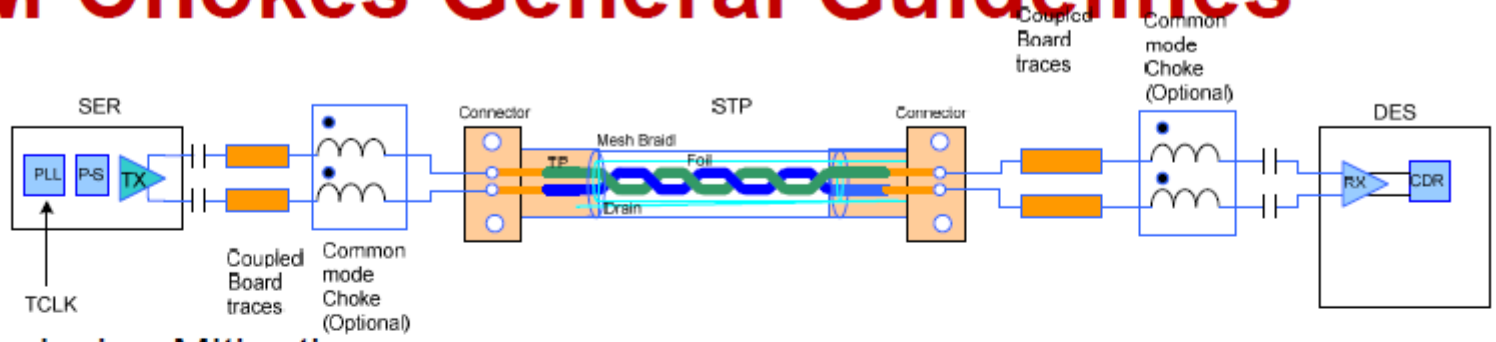
Staggered Output Switching



Spread Spectrum Effect



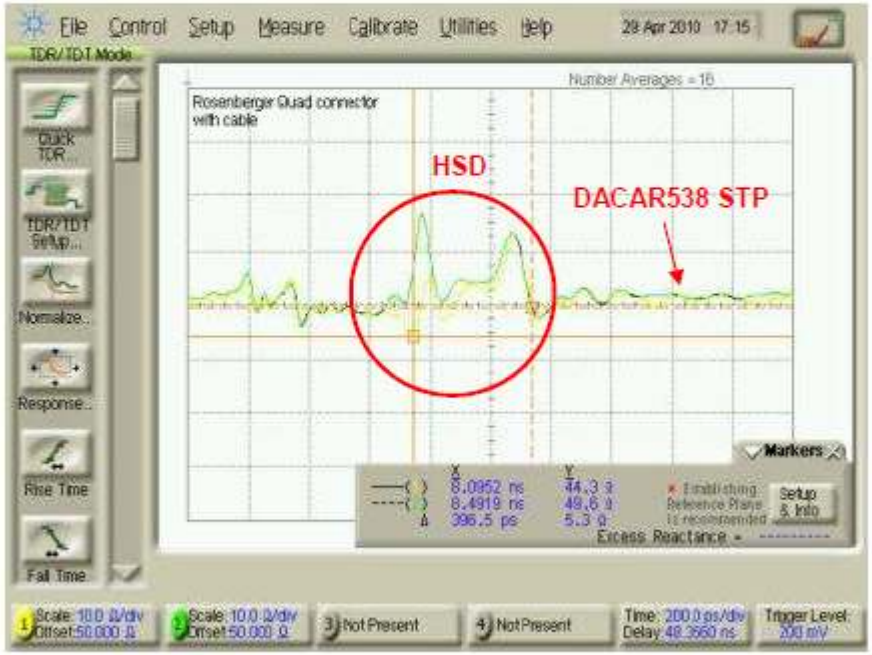
CM Chokes General Guidelines



- Emission Mitigation
  - Use TX CM Filter
- Cable Un-Balance Mitigation
  - Use RX CM Filter
- Select CM Filter with Highest CM Attenuation and Adequate Differential Bandwidth to support the Target Data Rate
  - 1.5 - 3Gb/s: DLW21SN121HQ2 or Equivalent
  - 0.5 – 1.5Gb/s: DLW21SN261XQ2 or Equivalent
  - <0.5Gb/s: DLW21SN491XQ2 or Equivalent
- Feedback from Murata
  - AEC-Q200 planned for above components
  - Please check with Murata for details

Impedance Profiles Examples

Rosenberger HSD® Connector: 4-position connector
with Leoni Dacar® 538 STP



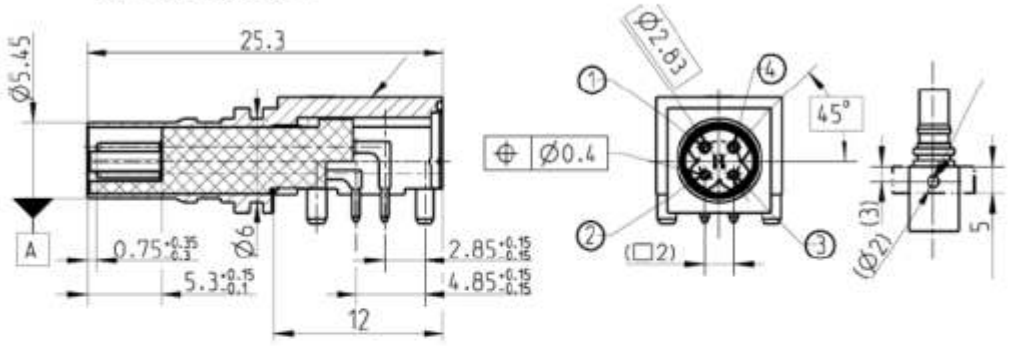
Diagonal Data pins, need careful layout to achieve symmetry

Honda TAK-A4 : 4-position connector
with Leoni Dacar® 522 STP

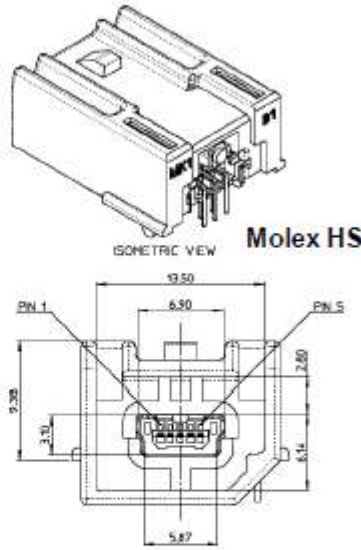
Data pins on the same row
– layout symmetry with small impedance mismatch

Examples of Connectors

Rosenberger HSD®



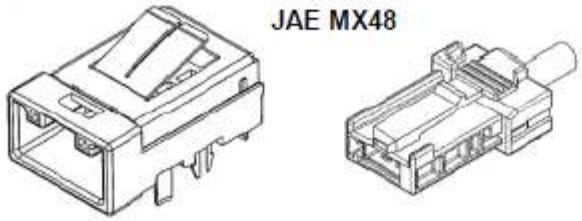
Molex HSAutoLink™



Hirose GT17

Honda TAK-A4

JAE MX48



FAKRA (SMB-A)