

# ***System Design Guidelines for Stellaris Microcontrollers***

---

## **ABSTRACT**

Stellaris<sup>®</sup> microcontrollers are highly integrated system-on-chip (SOC) devices with extensive interface and processing capabilities. Consequently, there are many factors to consider when creating a schematic and designing a circuit board. By following the recommendations in this design guide, you will increase your confidence that the board will work the first time it is powered it up.

---

## **Contents**

1	Introduction .....	1
2	Using This Guide .....	1
3	General Design Information .....	2
4	Feature-Specific Design Information .....	9
5	PCB Layout Examples .....	19
6	System Design Examples .....	21
7	Conclusion .....	22
8	References .....	22

## **1 Introduction**

The General Design Information section of the guide contains design information that applies to most designs (see “[General Design Information](#)”). Topics include important factors in the schematic design and layout of power supplies, oscillators, and debug accessibility . The Feature-Specific Design Information section describes specific peripherals and their unique considerations, allowing you to select the information that is relevant to your design (see “[Feature-Specific Design Information](#)”).

To further assist you with the design process, Texas Instruments provides a wide range of additional design resources, including application notes and reference designs. These designs and documents are an important reference. See “[System Design Examples](#)” for links to these resources.

## **2 Using This Guide**

The information in this design guide is intended to be general enough to cover a wide range of designs by describing solutions for typical situations. However, because every system is different, it is inevitable that there will be conflicting requirements and potential trade-offs. This is especially true in designs that include high-performance analog circuits, radio frequencies, high voltages, or high currents. If your design includes these features, then special considerations, beyond the scope of this application note, may be necessary.

Where possible, the distinction is made between preferred practice and acceptable practice. This distinction addresses the reality that constraints such as size, cost, and layout restrictions might not always allow for best-practice design.

When considering which practices to apply to a design, one of the most important factors is the I/O switching rate and current. If there is only low-speed, low-current switching on the Stellaris peripheral pins, then acceptable-practice rules are likely sufficient. If high-speed switching is present, particularly with simultaneous transitions (for example, the EPI module), then best-practice rules are recommended.

**Note:** Some of the information in this guide comes directly from the individual Stellaris microcontroller data sheets. The microcontroller data sheets are the defining documents for part usage and may contain specific requirements that are not covered in this design guide. You should always use the most

current version of the data sheet and also check the most recent errata document for the part number you have selected. Visit [www.ti.com/stellaris](http://www.ti.com/stellaris) to sign up for e-mail alerts specific to a Stellaris part number.

### 3 General Design Information

This section contains design information that applies to most Stellaris microcontrollers including:

- “Power”
- “Reset”
- “Oscillators”
- “JTAG Interface”
- “System”
- “All External Signals”

#### 3.1 Power

This section describes design considerations related to the microcontroller's power supply.

##### 3.1.1 Microcontroller Power Supply

Description	Classification	Applies to...	For more information, see:
Stellaris microcontroller power supply requirements	Schematic recommendations	All Stellaris microcontrollers	Microcontroller data sheet

Stellaris microcontrollers require only a single +3.3 V power supply. Other supply rails are generated internally by on-chip LDO regulators. The most visible internal supply rail is the core voltage ( $V_{DDC}$  or  $V_{DD25}$ ) because it has dedicated power pins for filter and decoupling capacitors.

Some Stellaris microcontrollers allow  $V_{DDC}$  to be provided from an external power source, see the Power Control section of the System Control chapter in the data sheet to determine if a specific device allows an external regulator. In certain applications, a designer might wish to use a switching power supply to reduce power loss in the  $V_{DDC}$  supply. A typical switching regulator has an efficiency of 85% compared to 36% for a 1.2-V linear regulator operating from 3.3 V.

The easiest way to avoid potential power sequencing issues when using a  $V_{DDC}$  switching supply is to use  $V_{DD}$  (+3.3 V) as the switcher's input source. For specific sequencing requirements, see the corresponding microcontroller data sheet.

If an external  $V_{DDC}$  source is used, the on-chip LDO regulator must still have a filter capacitor on its output. See “[LDO Filter Capacitor](#)” for details.

An external linear regulator offers no advantage over the on-chip linear regulator other than a small reduction in power dissipation within the Stellaris microcontroller.

During normal microcontroller operation, the power supply rail must remain within the electrical limits listed in the microcontroller data sheet ( $V_{dd}$  (min) and  $V_{dd}$  (max)). For optimal performance of the on-chip analog modules, the supply rail should be well regulated and have minimal noise. Noise sources such as audio transducers, relays, and other power-switching circuits should have their own supply rails, especially if ADC performance is a factor.

The microcontroller's internal power on reset (POR) circuit releases once the  $V_{DD}$  power supply rail reaches the POR threshold  $V_{th}$ . The BOR circuit is a more precise supply rail monitor and is normally used to hold in the microcontroller in reset if the supply rail drops out of operating range. On some Stellaris devices, the default BOR action is to generate a system reset. However, on other Stellaris devices, the software must configure the BOR to generate a reset rather than just an interrupt. Use of the BOR function is highly recommended.

External supervisors may also be used to assert the external reset signal RSTn under Power-On, Brown-out, or watchdog expiration conditions.

### 3.1.2 LDO Filter Capacitor

Description	Classification	Applies to...	For more information, see...
Information on selecting the right capacitor for the on-chip LDO voltage regulator	Schematic recommendations	All Stellaris microcontrollers	Microcontroller data sheet

All Stellaris microcontrollers have an on-chip voltage regulator to provide power to the core. On most parts, the LDO output must be connected to the  $V_{DDC}$  power pins. The voltage regulator requires a filter capacitor to operate properly (see the  $C_{LDO}$  parameter in the corresponding microcontroller data sheet for acceptable capacitor values).

The LDO capacitance is the sum of capacitor values on the LDO and  $V_{DDC}$  pins. Typically, the LDO pin capacitor is 1-2.2  $\mu\text{F}$  with additional 0.1 $\mu\text{F}$  capacitors distributed on the  $V_{DDC}$  pin(s). Use of capacitors outside of the CLDO range might prevent the regulator from starting or achieving regulation.

The recommended main LDO capacitor is 2.2  $\mu\text{F}$  10-25V X5R/X7R with 20% tolerance or better. Z5U dielectric capacitors are not recommended due to wide tolerance over temperature.

If an external  $V_{DDC}$  source is used, the on-chip LDO regulator must still have a filter capacitor on its output. The filter capacitance must be within the specified range to maintain regulator stability even though its output is otherwise not connected.

### 3.1.3 Decoupling Capacitors

Description	Classification	Applies to...	For more information, see...
Information on selecting the right power-rail decoupling capacitors.	Schematic recommendations	All Stellaris microcontrollers	Microcontroller data sheet

Ideally, Stellaris microcontrollers should have one decoupling capacitor in close proximity to each power supply pin. Decoupling capacitors are typically 0.01 $\mu\text{F}$  or 0.1 $\mu\text{F}$  in value and should be accompanied by a bulk capacitor near the microcontroller. The microcontroller combined  $V_{DD}$  and  $V_{DDA}$  bulk capacitance is typically between 2  $\mu\text{F}$  and 22  $\mu\text{F}$ , with values on the upper end of that range providing measurable ripple reduction in some applications, especially if the circuit board does not have solid power and ground planes. Bulk capacitance is particularly important if the microcontroller is connected to high-speed interfaces or needs to source significant GPIO current (that is, greater than 4mA) on more than a few pins.

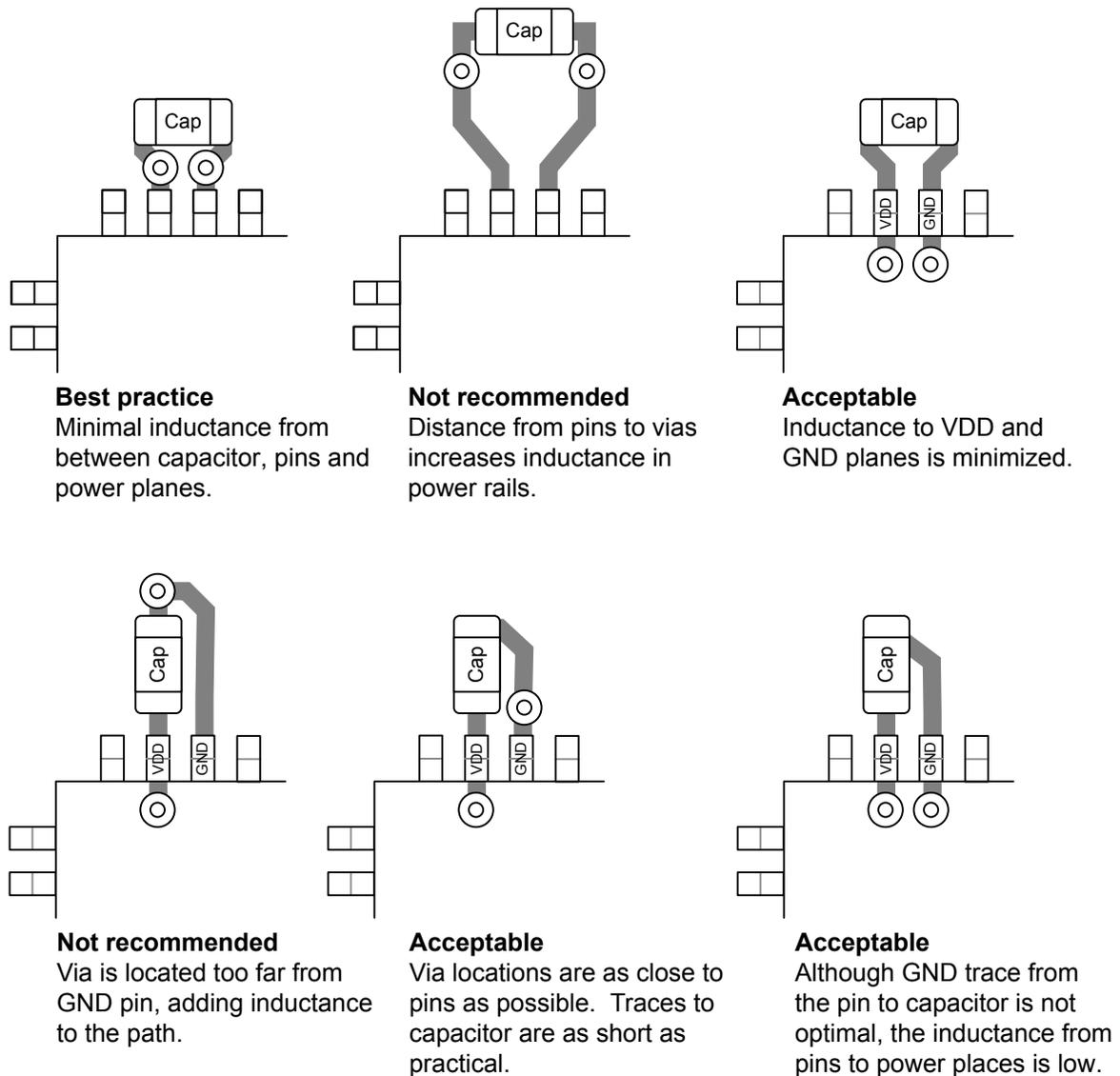
For optimal performance, locate one decoupling capacitor adjacent to each Power/Ground pin-pair. At a minimum, there should be one decoupling capacitor on each side of the microcontroller package.  $V_{DDC}$  pins should always have an adjacent decoupling capacitor.

Decoupling capacitors should be 10-25V X5R/X7R ceramic chip types. Z5U dielectric capacitors are not recommended due to wide tolerance over temperature.

The capacitance of most ceramic capacitors decreases with increasing voltage. Avoid using capacitors at close to their rated voltage unless reduced capacitance is acceptable. X7R capacitors may lose 15-20% of their capacitance at rated voltage while Y5V capacitors may drop 75-80%. [(Cain, Jeffrey, Comparison of Multilayer Ceramic and Tantalum Capacitors, AVX Technical. Bulletin.)]

Description	Classification	Applies to...	For more information, see...
Optimal layout practices when placing and routing power vias and decoupling capacitors	Layout recommendations	All Stellaris microcontrollers	Microcontroller data sheet

Figure 1 show different options for routing PCB traces between the Stellaris microcontroller power pins and a decoupling capacitor.



**Figure 1. PCB Routing Options**

### 3.1.4 Splitting Power Rails and Grounds

Description	Classification	Applies to...	For more information, see...
Factors to consider when deciding how to connect $V_{DD}$ , $V_{DDA}$ , GND, and GNDA pins	Schematic recommendations	All Stellaris microcontrollers	Microcontroller data sheet

Stellaris microcontrollers are designed to have  $V_{DD}$  and  $V_{DDA}$  pins connected directly to the same +3.3-V power source. Some applications may justify separation of  $V_{DDA}$  from  $V_{DD}$  to allow insertion of a filter to improve analog performance. Before deciding to split these power rails, the power architecture of the part should be reviewed to determine which on-chip modules are powered by each supply. The part data sheet contains a drawing that shows power distribution.

Filter options include filter capacitors in conjunction with either a low-value resistor or inductor/ferrite to form a low-pass filter.

If the  $V_{DD}$  and  $V_{DDA}$  pins are split, the circuit must ensure that power is applied and removed at the same time. For this reason, separate voltage regulators are not recommended.

The GND and GNDA pins should always be connected together - preferably to a solid ground plane or copper pour.

## 3.2 Reset

This section describes design considerations related to reset.

### 3.2.1 External Reset Pin Circuits

Description	Classification	Applies to...	For more information, see...
Guidelines for determining the optimal connection to the $\overline{RST}$ pin	Schematic and PCB layout recommendations	All Stellaris microcontrollers	Microcontroller data sheet

A special external reset circuit is not normally required. Stellaris microcontrollers have an on-chip Power-On-Reset (POR) circuit with a delay to handle power-up conditions.

$\overline{RST}$  can be connected to +3.3 V. For flexibility and noise-immunity, a resistor (1K $\Omega$ ) to +3.3 V and a capacitor (0.1 $\mu$ F) to GND are recommended. The latter also allows the signal to be driven from the JTAG debug connector.

Because the  $\overline{RST}$  signal routes to the core as well as most on-chip peripherals, it is important to protect the  $\overline{RST}$  signal from noise. This is particularly important in applications which involve power switching where fast transitions can couple into the reset line. The reset PCB trace should be less than 2" and routed away from noisy signals. Do not run the reset trace close to the edge of the board or parallel to other traces with fast transients.

The capacitor should be located as close to the pin as possible.

If the  $\overline{RST}$  signal source is another board, it is recommended to add a buffer IC on the Stellaris board to filter the signal.

A simple push-switch can be used to provide a manual reset. To avoid ringing on the  $\overline{RST}$  signal caused by switch bounce and stray inductance, add a low-value resistor (100  $\Omega$ ) in series with the switch.

Reset circuit options are shown in the microcontroller data sheets.

## 3.3 Oscillators

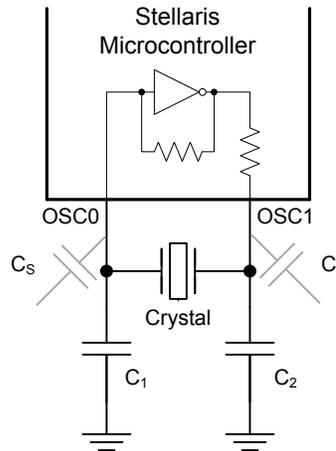
This section describes design considerations related to the microcontroller's oscillators.

### 3.3.1 Crystal Oscillator Circuit Components

Description	Classification	Applies to...	For more information, see...
Select criteria for the oscillator circuit components	Schematic recommendations	All Stellaris microcontrollers	Microcontroller data sheet

All Stellaris microcontrollers have a main oscillator circuit to provide a clock source for the device. Some parts also have similar clock circuits for the Ethernet PHY and/or the Hibernation module.

The on-chip parallel-resonant oscillator circuit requires an external crystal (see [Figure 2](#)) and two load capacitors to complete the circuit (the low-power Hibernation module oscillator on some devices may also require a 1 M $\Omega$  series resistor – see microcontroller data sheet for details).



**Figure 2. Oscillator Circuit**

Capacitors  $C_1$  and  $C_2$  must be sized correctly for reliable and accurate oscillator operation. Crystal manufacturers specify a load capacitance ( $C_L$ ) which should be used in the following formula to calculate the optimal values of  $C_1$  and  $C_2$ .

$$C_L = (C_1 * C_2) / (C_1 + C_2) + C_s$$

$C_s$  is the stray capacitance in the oscillator circuit. Stray capacitance is a function of trace lengths, PCB construction, and microcontroller pin design. For a typical design,  $C_s$  should be approximately 2-4pF. Because  $C_1$  and  $C_2$  are normally of equal value, the calculation for a typical circuit simplifies slightly to:

$$C_{1\&2} = (C_L - 3pF) * 2$$

For example, the DK-LM3S9B96 Development Kit uses a 16-MHz NX5032GA crystal from NDK with a  $C_L$  of 8 pF. Using that information and nominal stray capacitance,  $C_1$  and  $C_2$  calculate to 10 pF each.

Capacitors with an NP0/C0G dielectric are recommended and are almost ubiquitous for small value ceramic capacitors.

### 3.3.2 Crystal Oscillator Circuit Layout

Description	Classification	Applies to...	For more information, see...
PCB layout guidelines for the Stellaris oscillator circuits	PCB layout recommendations	All Stellaris microcontrollers	Microcontroller data sheet

The key layout objectives should be to minimize both the loop area of the oscillator signals and the overall trace length. A poor oscillator layout can result in unreliable or inaccurate oscillator operation and can also be a noise source. Ideal trace length is less than 0.25"/6mm. Do not exceed 0.5"/12mm.

Figure 3 shows a preferred layout for a small surface-mount crystal. The GND side of each capacitor routes directly to a via which provides a low-impedance connection to the GND plane.

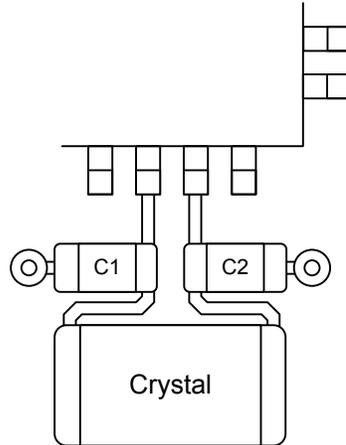


Figure 3. Recommended Layout for Small Surface-Mount Crystal

### 3.4 JTAG Interface

This section describes design considerations related to the microcontroller's JTAG interface.

#### 3.4.1 Debug and Programming Connector

Description	Classification	Applies to...	For more information, see...
Helpful information on connector and signal options for JTAG/SWD connections	Schematic recommendations	All Stellaris microcontrollers	Microcontroller data sheet

When designing a board that uses a Stellaris microcontroller, it is preferable to provide connections to all JTAG/SWD signals. In pin-constrained applications, SWD can be used instead of JTAG. SWD only requires two signals (*SWCLK* and *SWDIO*), instead of the four signals that JTAG requires, freeing up two additional signals for use as GPIOs. Check that your preferred tool-chain supports SWD before choosing this option. The LM Flash Programmer utility for Stellaris can program devices using SWD.

The most common ARM debug connector is a 2x10-way 0.1"-pitch header. Although it is robust, the 0.1" header is too large for many boards. An alternate connector definition, which is now quite popular, uses a 0.05" half-pitch 2x5 connector. The applicable assignments for both connectors are shown in [Table 1](#).

Table 1. Applicable Debug Connector Pin Assignments

JTAG/SWD Signal	ARM 20-pin	ARM 10-pin half-pitch
TCK/SWCLK	9	4
TMS/SWDIO	7	2
TDI	5	8
TDO	13	6
RESET	15	10
GND	4,6,8,10,12,14,16,18,20	3,5,9
TVCC	1	1

Some Stellaris microcontrollers have a  $\overline{\text{TRST}}$  signal that can be used to reset the JTAG module. The  $\overline{\text{TRST}}$  signal can be connected to pin 3 of the 20-pin ARM connector, but is not normally connected because a Test reset is normally initiated over the JTAG interface.

While most Stellaris microcontrollers enable a weak internal pull-up on TCK, TDI, TMS and TDO and  $\overline{\text{TRST}}$  (if applicable) out of reset, some devices default to floating inputs. For these devices, at a minimum, TCK, TMS

and  $\overline{TRST}$  (where present) should have pull-up resistors to +3.3 V to provide a safe state when a debug cable is not connected.

### 3.5 System

This section describes design considerations related to the system including unused pins.

#### 3.5.1 Unused Pins

Description	Classification	Applies to...	For more information, see...
Recommendations for any Stellaris microcontroller pins that are not connected	Schematic recommendations	All Stellaris microcontrollers	Microcontroller data sheet

The preferred connection for an unused microcontroller pin depends on the pin's function. Each Stellaris microcontroller data sheet has a table in the Signals chapter that lists the fixed function pins and both the acceptable practice and the preferred practice for reduced power consumption and improved EMC characteristics. If a module is not used in a system, and its inputs are grounded, it is important that the clock to the module is never enabled by setting the corresponding bit in the **RCGCx** register.

### 3.6 All External Signals

This section describes design considerations related to the microcontroller's external signals.

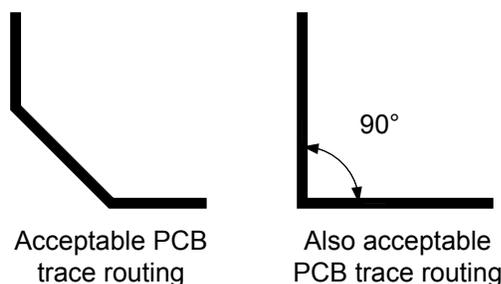
#### 3.6.1 PCB Design Rules: 90° PCB Traces

Description	Classification	Applies to...	For more information, see...
General rules for routing PCB traces on high-speed nets	PCB layout recommendations	All Stellaris microcontrollers	<ul style="list-style-type: none"> <li>Microcontroller data sheet</li> <li>Reference design PCB files</li> </ul>

For many years, it has been common PCB design practice to avoid 90° corners in PCB traces. In fact, most PCB layout tools have a built-in miter capability to automatically replace 90° angles with two 45° angles.

The reality is that the signal-integrity benefits of avoiding 90° angles are insignificant at the frequencies/edge-rates seen in microcontroller circuits (even up to and past 1 GHz/100ps). [Johnson, H and Graham, M, *High-Speed Digital Design: a Handbook of Black Magic*, Prentice Hall: New Jersey, 1993.]

Additionally, a report could find no measurable difference in radiated EMI. [Montrose, Mark I, *Right Angle Corners on Printed Circuit Board Traces, Time and Frequency Domain Analysis*, undated.]



**Figure 4. Acceptable PCB Trace Routing**

**Note:** Loops in PCB traces are not acceptable, despite the references that indicate that the signal-integrity benefits of avoiding 90 angles is negligible. Loops in traces form antennas and add inductance. The data shows that if your layout does have antenna loops, then mitering the angles to 135° is not going to help. Avoid loops in PCB traces.

Despite these conclusions, there are a few simple reasons to continue to avoid 90° angles:

- There is a higher possibility of an acid-trap forming during etching on the inside of the angle (especially in acute angles). An acid trap causes over-etching which can be a yield issue in PC boards with small trace widths.
- Routing at 45° typically reduces overall trace length. This frees board area, reduces current loops, and improves both EMC emissions and immunity.
- It looks better. This is an important factor for anyone who appreciates the art of PCB layout.

## 4 Feature-Specific Design Information

This section contains feature-specific design information and is grouped by function or peripheral:

- [“Ethernet MAC and PHY”](#)
- [“Ethernet and USB”](#)
- [“USB”](#)
- [“EPI”](#)
- [“General Guidelines for All High-Speed Interfaces”](#)
- [“ADC”](#)

### 4.1 Ethernet MAC and PHY

This section describes design considerations related to the microcontroller's Ethernet module.

#### 4.1.1 Ethernet Resistors

Description	Classification	Applies to...	For more information, see...
Selection criteria for Ethernet pull-up and bias resistors	Schematic recommendations	All Stellaris microcontrollers with Ethernet MAC and PHY	<ul style="list-style-type: none"> <li>• Microcontroller data sheet</li> <li>• Evaluation board schematics</li> </ul>

A total of six resistors are required for Ethernet operation.

Four pull-up resistors are required for terminating and biasing the Ethernet transceivers. Resistors should be connected from the TXOP, TXON, RXIP and RXIN signals to +3.3 V. The specified value for these resistors is 50Ω. The recommended, commonly available value is 49.9Ω 1%. Do not use resistors with a tolerance greater than 1%. Resistor power dissipation is low because the peak voltage on the resistor is only about 1 V. Small, 0402 (1005 Metric) surface-mount resistors have an acceptable power rating.

The MDIO pin is a single-wire serial link between the on-chip MAC and PHY. The MDIO pin requires an external 10kΩ pull-up resistor. The resistor type is not critical.

An additional resistor is required on the ERBIAS pin to set the bias voltage for the Ethernet module. See [“Bias Resistors”](#) of this guide for more information.

#### 4.1.2 Ethernet PCB Layout

Description	Classification	Applies to...	For more information, see...
Selecting transformers and associated components	Layout	All Stellaris microcontrollers with Ethernet MAC and PHY	<ul style="list-style-type: none"> <li>• Microcontroller data sheet</li> <li>• Evaluation board schematics</li> </ul>

The Stellaris data sheets list the part number and manufacturer's name for several approved Ethernet transformer (“magnetics”) options. Other parts can be approved by similarity, but it is highly recommended to check with the manufacturer for their assessment of suitability.

Ethernet implementation can use either a connector with integrated transformer or a transformer with a separate connector. Connections from the transformer to the Stellaris microcontroller are straightforward.

One differential pair is named TXOP/TXON and the other RXIP/RXIN. These names reflect the default functions – in fact the RX and TX pairs are identical and can perform either function as the Ethernet PHY supports MDI/MDX.

The center tap of the transformer (microcontroller-side of the transformer) should be connected to +3.3 V. Each connection point to the +3.3 V rail must be adequately filtered with a capacitor. 0.1uF or greater if a solid power-plane is present. For lowest noise, or if the center tap connects to a PCB trace, the capacitor value should be 1uF or greater.

#### 4.1.3 Other Ethernet Components

Description	Classification	Applies to...	For more information, see...
PCB layout guidelines for the Stellaris oscillator circuits	Schematic recommendations	All Stellaris microcontrollers with Ethernet MAC and PHY	<ul style="list-style-type: none"> <li>• Microcontroller data sheet</li> <li>• Reference design PCB files</li> <li>• See <a href="#">“General Guidelines for All High-Speed Interfaces”</a></li> </ul>

Good PCB layout and routing practices are important to ensure reliable Ethernet signalling.

#### Signal Impedance

Both Ethernet signal pairs should be routed as a 100-Ω differential pair.

The optimal way to achieve 100-Ω differential impedance is a two-step process. During PCB layout, the designer should use PCB tools to set the spacing and width of the traces to get close to the target characteristic impedance.

**Note:** The PCB fab notes should include annotation that specifies which traces are to be “impedance controlled.”

The second step is performed by the PCB fab house, which adjusts the trace space and width to match their specific materials and process.

Another key benefit of specifying controlled impedance is that the PCB manufacturer assumes on-going responsibility for maintaining the impedance of those traces. This can be a factor when lot-to-lot differences introduce variation.

While specifying controlled-impedance is preferred, it may be acceptable to skip that step if the trace length is less than approximately 2”. If good design rules are followed during layout, it should be possible to achieve routing that provides good signal integrity. To date, the Stellaris lab has completed six designs with this approach and all boards have passed IEEE compliance tests that perform detailed signal analysis.

A slight variation of this method, which also avoids the additional cost of controlled-impedance PCBs, is sometimes called “controlled dielectric.” This approach involves the PCB designer using a dielectric specification that is either supplied or agreed-to by the board fab house. The material and dielectric constant should be added to the PCB fab notes.

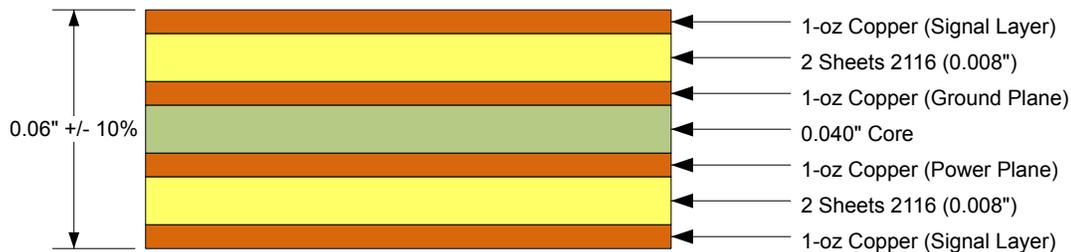
#### Achieving 100Ω Impedance

Some PCB design tools have an integrated trace impedance calculator that factors in trace geometry, trace length, board stack-up, and the board material's dielectric constant. There are also several free programs that can perform similar calculations. When using these tools, ensure that the differential impedance (impedance between the signals in the pair) is 100 Ω. If a ground plane is present, the single-ended impedance (Zo) should be 50 Ω.

The typical dielectric constant (Er) for FR-4 material is about 4.3. The following examples use this parameter to generate some typical PCB geometries. They are intended as a starting-point for PCB designs. You should

repeat the calculations for your own design because even small changes in the PCB stack-up can significantly change the impedance.

A typical configuration for an FR-4, 0.062" circuit board with 4-layers of 1-oz copper (no plating) is shown in [Figure 5](#).



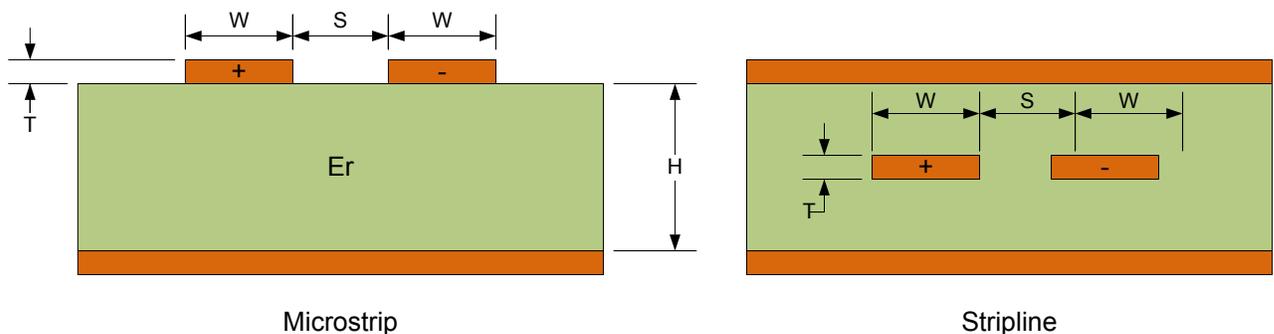
**Figure 5. Typical Four-Layer PCB Stack with Routing Assignments**

For this example, we place a solid ground plane on layer 2. The 1-oz copper plane is 1.4mils thick. The height of traces above the ground plane is defined by the thickness of the PCB prepreg material – in this case 0.008" thick. Therefore, total thickness is:

$$\text{Total thickness} = 0.062" = 4 \times 0.0014" + 0.040" + 2 \times 0.008"$$

Before calculating the trace width and spacing needed for 100-Ω impedance, we need to determine the type of transmission line model to use.

A PCB with a conductor bounded by a single ground reference plane is known as a microstrip as shown in [Figure 6](#).



**Figure 6. Transmission Lines for Ethernet Signalling**

Microstrip transmission lines are most common on boards with 2-6 layers and are entirely suitable for Ethernet signalling. A more advanced configuration, known as Stripline, uses two ground-reference planes which are typically stitched together with vias to form a coaxial cable-like transmission path.

Using the free PCB ToolKit calculator from Saturn PCB Design, Inc., results in the following values for the board stack shown in [Figure 7](#).

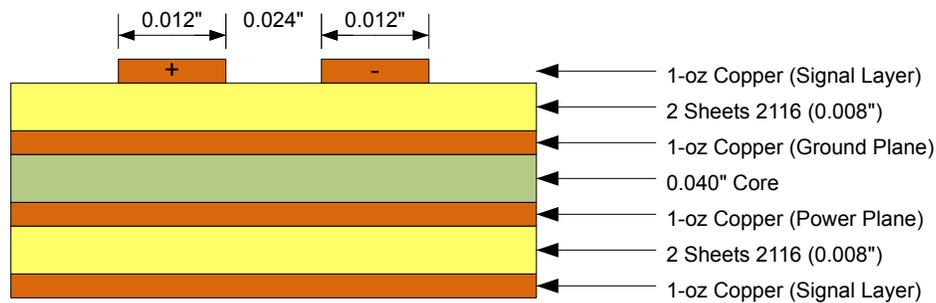
Conductor width (W) = 0.012"  
 Conductor spacing (S) = 0.024"  
 Substrate Thickness (H) = 0.008"  
 $Z_{\text{differential}} = 100.1 \Omega$   $Z_0 = 54 \Omega$

HyperLynx from Mentor graphics gives the following, similar, results:

```

Conductor width (W) = 0.012"
Conductor spacing (S) = 0.024"
Substrate Thickness (H) = 0.008"
Zdifferential = 100.1 Ω ZO = 54.2 Ω
    
```

The HyperLynx model is more complete as it also factors in the Er of the soldermask as shown in [Figure 7](#).



**Figure 7. 100-Ω Microstrip Differential Pair on a Four-Layer 0.06" FR-4 PCB Stack**

For a 2-layer board, the height of the substrate is now the full thickness of the FR-4 PCB material. This makes it difficult to achieve anything close to 50-Ω single-ended impedance (ZO). However, because the ZO parameter is less critical, we can still solve dimensions for the differential impedance. The following analysis was performed with HyperLynx because the dimensional aspect ratio is not supported by the free Saturn PCB Design tool.

```

Conductor width (W) = 0.018"
Conductor spacing (S) = 0.007"
Zdifferential = 100.5 Ω ZO = 100.7 Ω
    
```

### **Other Design Rules and Considerations**

Follow these additional design rules and recommendations for best results:

- Apply the rules for high-speed signal routing listed elsewhere in this application note.
- Maintain symmetry when routing differential pairs. Some PCB layout tools can assist with this kind of routing.
- Avoid vias if possible. If it is necessary to switch layers, then both signals in the pair should pass through a via at the same distance on the trace.
- Avoid stubs.
- Route differential signal pairs on the same layer.
- Separate Ethernet signal pairs from each other by at least 0.050". This is necessary to avoid cross-coupling between the RX and TX pair.
- Place Ethernet resistors as close as possible to the Stellaris microcontroller.
- Do not extend a ground plane under the transformer, if using an unshielded transformer.
- Place 10pF capacitors close to the Ethernet transformer.

### **Ethernet and Power Planes**

A continuous ground plane is a good PCB design practice, however, there are special considerations when using planes and copper pours near Ethernet signals. The following restrictions apply only to Ethernet; general information on the recommended attributes of power planes are covered elsewhere in this application note.

Strict requirements for planes near Ethernet circuits:

- Do not extend the power plane (that is, the  $V_{DD}$  plane) under the Ethernet signals unless there is a solid ground plane between the differential Ethernet signals and the power plane.
- Make sure there are no ground plane discontinuities under or near the differential signals. This rule applies to all signals routed over planes.
- Do not extend the ground plane under the transformer unless it is shielded on all sides.
- Do not extend the ground plane under the signals from the transformer to the connector.

Other ground plane considerations:

- A ground plane is not strictly a requirement for Ethernet signalling. The benefits of retaining the ground plane between the microcontroller and the transformer are:
  - Provides a low-impedance connection point for the 10pF filter capacitors. If correctly installed, these capacitors can improve Ethernet electro-magnetic compatibility (EMC).
  - Impedances are easier to control with a ground-reference plane. Without the plane, small dimensional variations in the PCB have a more significant impact on the differential impedance.
  - Smaller trace geometries are possible. Without a plane, simulations show that 0.023" traces with 0.007" spacing are needed for a typical two-layer FR-4 design.
- It may be difficult to implement a trace geometry that achieves both 100  $\Omega$  differential impedance and 50  $\Omega$  single-ended impedance. The most critical parameter to optimize for is differential impedance.

## 4.2 Ethernet and USB

This section describes design considerations related to the microcontroller's Ethernet and USB modules.

### 4.2.1 Bias Resistors

Description	Classification	Applies to...	For more information, see...
Selection and routing information on the bias resistor(s)	Schematic and layout recommendations	All Stellaris microcontrollers with Ethernet or USB	<ul style="list-style-type: none"> <li>• Microcontroller data sheet</li> <li>• Evaluation board schematics</li> </ul>

All Stellaris microcontrollers with integrated Ethernet and/or USB may require 1% precision bias resistors to provide an accurate reference for the PHY circuitry. The Ethernet PHY requires a 12.4k resistor and the USB controller may require a 9.10K resistor.

Bias resistors must be located close to the microcontroller pin (ideally <0.25"/6mm). The other resistor terminal should have a very short trace directly to GND. The trace/via for the GND connection should not be shared with any other pin.

### 4.2.2 Other PCB Design Rules

Description	Classification	Applies to...	For more information, see...
General guidelines for PCB design	Schematic recommendations	All Stellaris microcontrollers with Ethernet or USB	<ul style="list-style-type: none"> <li>• Microcontroller data sheet</li> <li>• Evaluation board schematics</li> </ul>

While solid ground and power planes are highly desirable, small areas of copper pour should be used cautiously. It is often not a good idea to pour every available area on the routing layers of multi-layer boards. On one- and two-layer board designs, multiple pours might be necessary, because dedicated plane layers are not available.

If used, never leave small copper pours floating or unconnected. Isolated conductor areas can cause unwanted coupling and EMC problems if they act as an antenna. Small copper pours should have solid connections to a ground net/trace. Ideally, use several vias to provide a low-impedance connection.

### 4.2.3 Chassis Ground

Description	Classification	Applies to...	For more information, see...
How and when to use a chassis ground to achieve optimal EMC	Schematic and PCB layout recommendations	All Stellaris microcontrollers with Ethernet or USB	Evaluation board schematics

When properly designed, a chassis ground routed on the PCB can be a very effective feature for addressing a range of Electro-Magnetic Compatibility (EMC) challenges.

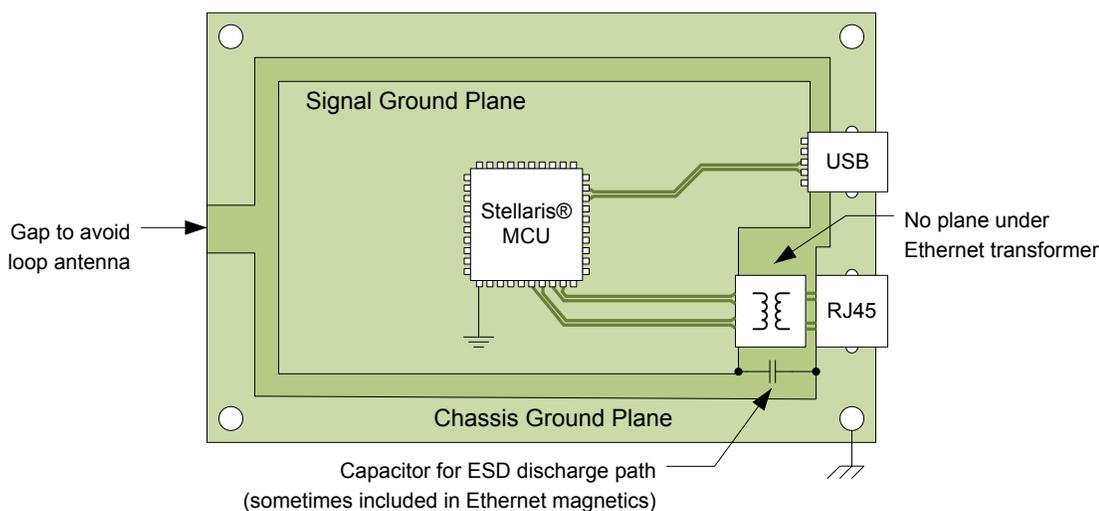
One specific benefit is improved Electro-Static Discharge (ESD) immunity due to the provision of a safe discharge path that avoids sensitive circuitry in the center of the board.

In general, a chassis ground on the PCB works in conjunction with the overall enclosure to improve electro-magnetic emissions and especially immunity.

The chassis ground should be routed or poured copper around the perimeter of the PCB, ideally on all layers. If the ground is not present on all PCB layers, then other layers should be pulled back from the chassis ground to avoid coupling. The chassis ground should not route over the top of any power or ground layer.

Typically, the chassis ground should have a break or void in to prevent loops that could cause loop antenna effects. However, depending on the size of the board, enclosure design, and ground connection point locations, it might still be acceptable or preferable to have a continuous chassis ground around the board.

A chassis ground is particularly important in systems with external connectors, metal enclosures, or apertures in the enclosure (see [Figure 8](#)).



**Figure 8. Chassis Ground Guidelines**

### 4.3 USB

Description	Classification	Applies to...	For more information, see...
PCB layout guidelines for the Stellaris USB signals	PCB layout recommendations	All Stellaris microcontrollers with a USB module	<ul style="list-style-type: none"> <li>Microcontroller data sheet</li> <li>Evaluation board schematics</li> <li>See <a href="#">"General Guidelines for All High-Speed Interfaces"</a></li> </ul>

Good PCB layout and routing practices are important in ensuring reliable USB signalling. Routing the D+/D- differential pair is the most important consideration.  $V_{BUS}$  and ID (typically used only in USB OTG and dual-mode applications) signal routing is not critical as these are low-speed signals.

#### 4.3.1 Signal Impedance

The USB D+/D- signal pair should be routed as a 100- $\Omega$  differential pair.

The optimal way to achieve 90 $\Omega$  differential impedance is a two-step process. During PCB layout, the designer should use PCB tools to set the spacing and width of the traces to get close to the target characteristic impedance.

**Note:** The PCB fab notes should include annotation that specifies which traces are to be "impedance controlled."

The second step is performed by the PCB fab house, which adjusts the trace space and width to match their specific materials and process.

Another key benefit of specifying controlled impedance is that the PCB manufacturer assumes on-going responsibility for maintaining the impedance of those traces. This can be a factor when lot-to-lot differences introduce variation.

While specifying controlled-impedance is preferred, it may be acceptable to skip that step if the trace length is less than approximately 2". If good design rules are followed during layout, it should be possible to achieve routing that provides good signal integrity. To date, the Stellaris lab has completed six designs with this approach and all boards have passed IEEE compliance tests that perform detailed signal analysis.

A slight variation of this method, that also avoids the additional cost of controlled-impedance PCBs, is sometimes called "controlled dielectric." This approach involves the PCB designer using a dielectric specification that is either supplied or agreed-to by the board fab house. The material and dielectric constant should be added to the PCB fab notes.

#### 4.3.2 Achieving 90 $\Omega$ Impedance

Some PCB design tools have an integrated trace impedance calculator that factors in trace geometry, trace length, board stack-up, and the board material's dielectric constant. There are also several free programs that can perform similar calculations. When using these tools, ensure that the differential impedance (impedance between the signals in the pair) is 90  $\Omega$ . If a ground plane is present, the single-ended impedance ( $Z_0$ ) should be 50  $\Omega$ .

The typical dielectric constant ( $E_r$ ) for FR-4 material is about 4.6.

A typical configuration for an FR-4, 0.062" circuit board with 4-layers of 1-oz copper and 1/2-oz plating is shown in Figure 9.



Typical 4 Layer PCB Stack

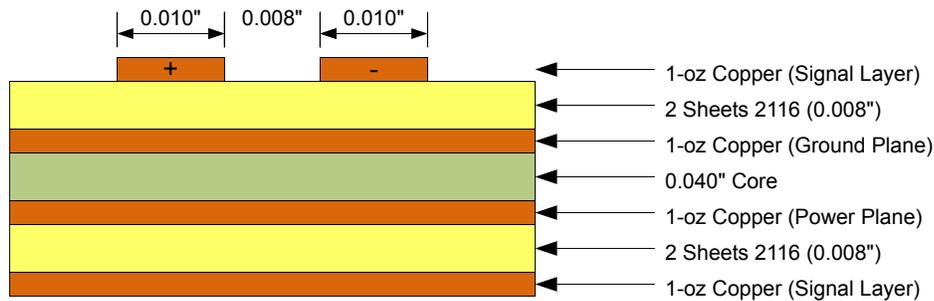
**Figure 9. Typical Four-Layer PCB Stack**

For this example, we place a solid ground plane on layer 2. The 1-oz copper plane is 1.4mils thick. The height of traces above the ground plane is defined by the thickness of the PCB prepreg material – in this case 0.008” thick. Therefore, total thickness is:

$$\text{Total thickness} = 0.062'' = 4 \times 0.0014'' + 0.040'' + 2 \times 0.008''$$

Using the free PCB ToolKit calculator from Saturn PCB Design, Inc., results in the following values for the board stack shown in [Figure 10](#).

Conductor width (W) = 0.010"  
 Conductor spacing (S) = 0.008"  
 $Z_{\text{differential}} = 90 \Omega$   
 $Z_0 = 55 \Omega$



90Ω Microstrip Differential Pair on  
 a 4-layer 0.06" FR-4 PCB stack

**Figure 10. 90Ω Microstrip Differential Pair on a Four-Layer 0.06" FR-4 PCB Stack**

The PCB fabricator improves the value and tolerance of these results if the traces are specified as controlled-impedance.

For a 2-layer board, the height of the substrate is now the full thickness of the FR-4 PCB material. The height of the substrate means that much wider traces are needed to achieve 90 Ω impedance. The following analysis was performed with HyperLynx because the dimensional aspect ratio is not supported by the free Saturn PCB Design tool.

Conductor width (W) = 0.028"  
 Conductor spacing (S) = 0.007"  
 $Z_{\text{differential}} = 90 \Omega$   
 $Z_0 = 91.5 \Omega$

### 4.3.3 Other Design Rules and Considerations

Follow these additional design rules and recommendations for best results:

- Apply the rules for high-speed signal routing listed elsewhere in this application note.
- Maintain symmetry when routing differential pairs. Some PCB layout tools can assist with this kind of routing.
- Avoid vias if possible. If it is necessary to switch layers, then both signals in the pair should pass through a via at the same distance on the trace.
- Avoid stubs when adding components to D+/D- signals. Devices such as ESD suppressors should be located directly on the signal trace.
- Route differential signal pairs on the same layer.

## 4.4 EPI

Description	Classification	Applies to...	For more information, see...
Routing recommendations for high-speed signals used by the External Peripheral Interface (EPI) module	Schematic recommendations	All Stellaris microcontrollers with EPI	<ul style="list-style-type: none"> <li>Microcontroller data sheet</li> <li>Evaluation board schematics</li> </ul>

The External Peripheral Interface (EPI) module is a high-bandwidth bus that can interface to various kinds of external memory and other devices. Due to the speed and special timing requirements of this interface, special layout considerations are necessary.

In EPI mode, Stellaris microcontroller pins are characterized with a 16pF rather than a 50pF load. To maintain timing margins over the full operating speed of the EPI module, EPI signal capacitance must be 16pF or less and the GPIO drive-strength should be set to 8 mA. This includes both the load and trace capacitance. It is not necessary to include the Stellaris microcontroller pin/pad characteristic when evaluating total capacitive loading.

For SDRAM and multiplexed host-bus modes, it is important to factor in multiple loads on some EPI signals. For example, in SDRAM mode, EPIxS0..EPIxS14 are used to drive both address and data signals to the SDRAM. For a Micron MT48LC4M16A2 SDRAM in a TSOP package, the address inputs have a worst-case capacitance of 3.8pF and the data lines (DQs) of 6.0pF. Deducting this from 16pF results in an allowance of about 8pF for trace capacitance.

Using the 0.062" 4-layer FR4 PCB stack-up from the DK-LM3S9x96 Development Kit, we can calculate the capacitance per inch for an 0.008" trace. HyperLynx and Saturn PCB tool kit both provides provide capacitance values of around 1.8pF/inch. So the maximum trace length is  $6.2 \text{ pF} / (1.8 \text{ pF/inch}) = 3.44"$ .

The Stellaris DK-LM3S9B96 Development board has worst-case trace length on the `SDCLK` signal of 3.15" on the main board and 0.225" on the SDRAM board. This total length is less than the 3.44" target. The EPI signals do pass through a board-to-board connector but the capacitance to ground is very small and can be ignored. Design tools should be used to calculate the maximum allowable trace length for a specific design based on PCB geometry and materials.

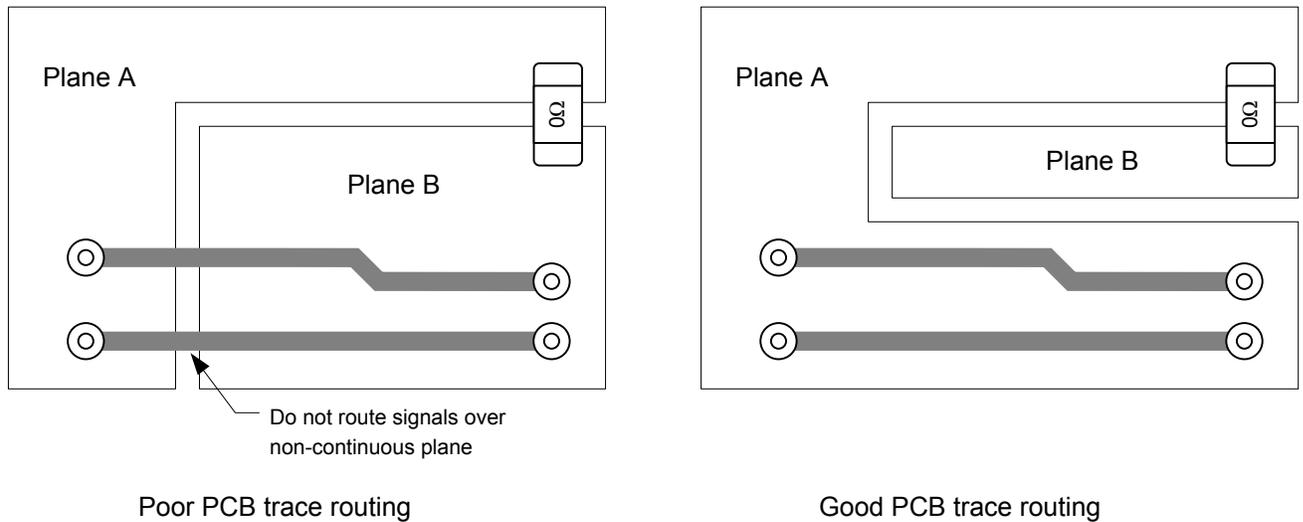
## 4.5 General Guidelines for All High-Speed Interfaces

This section describes design considerations related to the microcontroller's Ethernet, USB, EPI, and other high-speed interfaces.

### 4.5.1 PCB Design Rules: Other Routing Guidelines

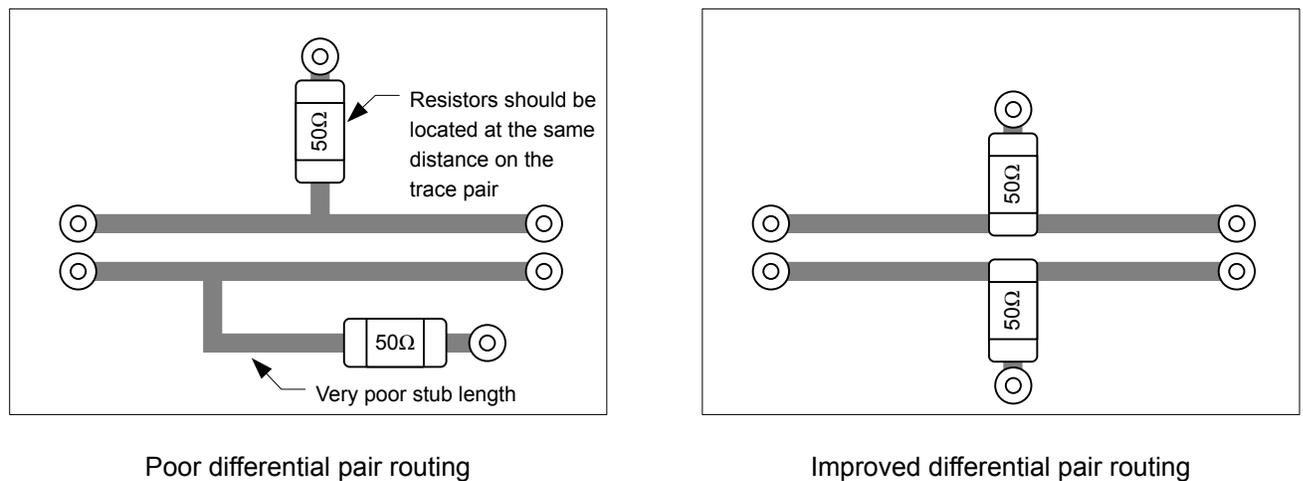
Description	Classification	Applies to...	For more information, see...
General rules for routing PCB traces on high-speed nets	PCB layout recommendations	All Stellaris microcontrollers with Ethernet, USB, EPI, or other high-speed interface	<ul style="list-style-type: none"> <li>Microcontroller data sheet</li> <li>Reference design PCB files</li> </ul>

Avoid discontinuities in ground planes and power planes under high-speed signals as shown in [Figure 11](#). For controlled-impedance interfaces like Ethernet and USB, discontinuities create impedance changes that impact signal integrity. For all signals, a break in the ground plane removes a direct path for any return current to flow through. This is important even for balanced differential pairs because perfect matching is seldom achievable and ground current is inevitable.



**Figure 11. Examples of PCB Trace Layout**

Avoid stubs in differential signal pairs where possible (see Figure 12). Where termination or bias resistors are needed, one terminal should be located directly on the trace. Both resistors should be located at the same distance from the source and load.



**Figure 12. Examples of Differential Pair Layout**

Stellaris microcontrollers provide programmable drive strength for all digital output pins. To improve the performance of digital signals, set the GPIO drive strength register appropriately. Selecting a lower drive strength can avoid signal integrity issues due to ringing and reflections. If the drive strength is too low, however, timing and rise/fall time requirements may not be satisfied.

#### 4.6 ADC

This section describes design considerations related to the microcontroller's ADC module.

#### 4.6.1 ADC Input Schematics

Description	Classification	Applies to...	For more information, see...
How to achieve optimal ADC performance through careful circuit design	Schematic recommendations	All Stellaris microcontrollers with ADC	<ul style="list-style-type: none"> <li>• Microcontroller data sheet</li> <li>• Reference design schematics</li> </ul>

In order to achieve the best possible conversion results from an ADC, it is important to start with a good schematic design.

All ADCs require a voltage reference (or occasionally a current reference), whether the voltage reference is provided from an on-chip source or via an external pin. Any deviation in the reference voltage from its ideal level results in additional gain error (or slope error) in the conversion result.

Stellaris microcontrollers incorporate an internal voltage reference which can save the cost of an external reference device. The designer should determine whether the internal reference has sufficient accuracy or if an external reference is needed. If an external reference is used, it should be used with capacitors on both the supply pin and the output pin. See the voltage reference in the corresponding microcontroller's data sheet for recommendations on value. Typically 1 $\mu$ F or more is recommended.

Optimal ADC accuracy is achieved with a low-impedance source and a large input filter capacitor. As the signal source impedance increases and capacitance decreases, noise on the conversion result increases. Noise sources include coupling from other signals, power supplies, external devices, and from the microcontroller itself.

If resistor dividers are used to scale an input voltage, then best results can be achieved with low value resistors. The resistor from the ADC input to ground should ideally be less than 1k $\Omega$ . Avoid values higher than 10k $\Omega$  unless a large filter capacitor is present.

Ceramic filter capacitors of 1 $\mu$ F or more can substantially improve noise performance. The trade-off is a reduction in signal bandwidth (as a function of the source impedance) and phase shifting.

Input protection should also be considered, especially when converting signals from external devices or where transient voltages might be present. The ADC pins on some Stellaris devices (in ADC mode) are not 5-V tolerant, but do allow some margin over the +3.0 V span. See the microcontroller data sheet for specific information.

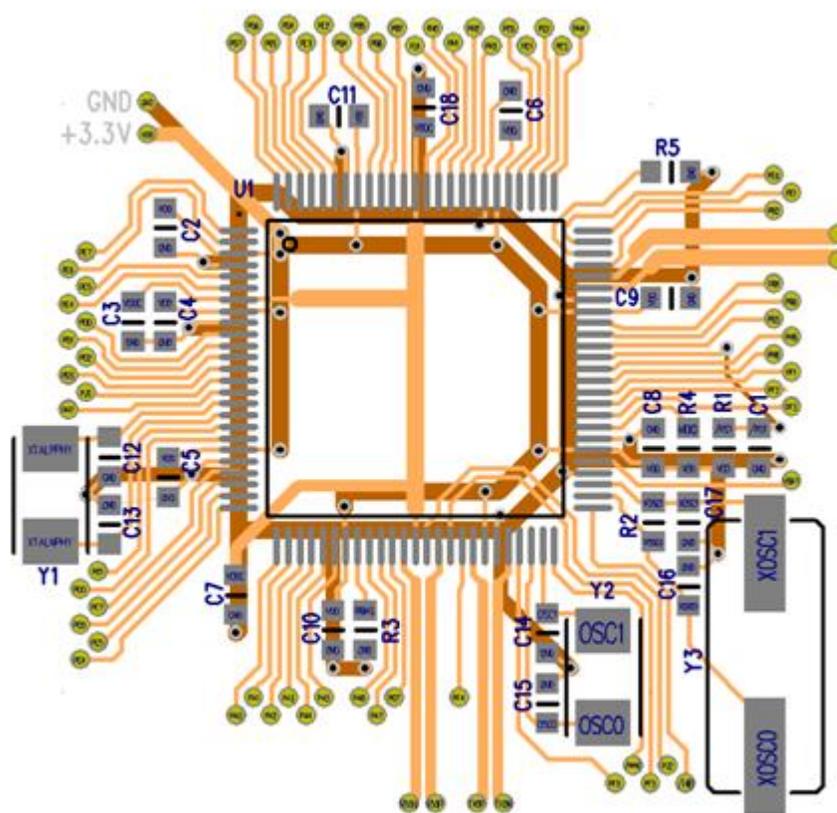
Increased source impedance can provide a degree of protection to the ADC. Semiconductor clamping circuits can also be used – typically zener diodes or clamping diodes to 3 V and GND. When specifying diodes, consider leakage current over temperature ( $I_r$ ) as this affects overall conversion accuracy.

## 5 PCB Layout Examples

This section provides PCB layout examples for a 100-pin TQFP package and a 48-pin TQFP package.

### 5.1 TQFP 100-Pin Routing

Description	Classification	Applies to...	For more information, see...
An example of a 2-layer PCB layout for a Stellaris LM3S9B90 microcontroller in a 100-pin TQFP package	PCB layout recommendations	All Stellaris microcontrollers	<ul style="list-style-type: none"> <li>• Microcontroller data sheet</li> <li>• Evaluation board schematics</li> </ul>



**Figure 13. Stellaris LM3S9B90 Microcontroller Minimal Circuit**

Figure 13 shows a minimal circuit for an LM3S9B90 Stellaris microcontroller with Ethernet, USB, and Hibernate modules. Pull-up resistors might also be needed on JTAG signals if these pins are not driven externally.  $V_{DD}$ ,  $V_{DDC}$  and GND connections are shown as thick PCB traces for clarity. Normally these connections would be extended as copper pours.

- R1 Reset input pull-up resistor
- C1 Reset input filter capacitor
- C3 LDO regulator filter capacitor
- C2, C4-C6, C11  $V_{DD}$  Decoupling capacitors
- C7, C18  $V_{DDC}$  Decoupling capacitors
- C12-C17 Crystal load capacitors
- Y1 Ethernet Crystal
- Y2 Main Oscillator Crystal
- Y3 Hibernate Module Crystal
- R3 Ethernet RBIAS resistor
- R2 Hibernate Oscillator resistor
- R5 USB RBIAS
- R4 MDIO Pull-up resistor

## 5.2 TQFP 48-Pin Routing

Description	Classification	Applies to...	For more information, see...
An example of a 2-layer PCB layout for a Stellaris LM3S811 microcontroller in a 48-pin TQFP package	PCB layout recommendations	All Stellaris microcontrollers	<ul style="list-style-type: none"> <li>Microcontroller data sheet</li> <li>Evaluation board schematics</li> </ul>

Figure 14 shows a minimal circuit for an LM3S811 Stellaris microcontroller. Pull-up resistors might be needed on PB7/TRST and JTAG signals if these pins are not driven externally.

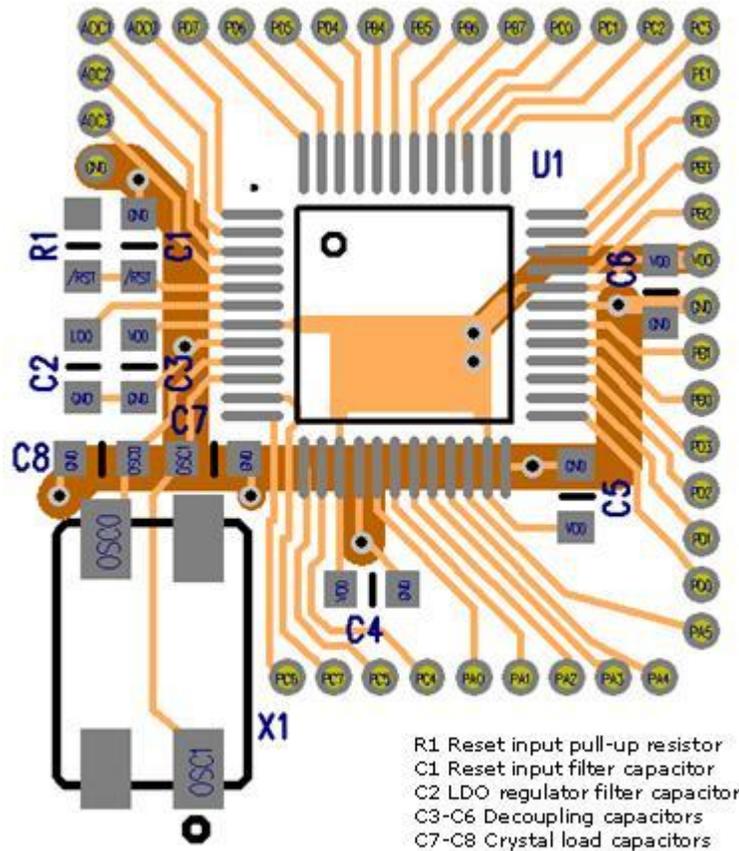


Figure 14. Stellaris LM3S811 Microcontroller Minimal Circuit

## 6 System Design Examples

For example designs using Stellaris microcontrollers, see Table 2 for the detailed list of Stellaris Reference Design Kits (RDs), Evaluation Kits (EKs), and Development Kits (DKs).

Schematics are available for all designs. Full PCB design files including Gerber files are available for Stellaris reference designs only.

Table 2. Stellaris Example Designs

Part Number	Description	Stellaris Devices	Device Package	Key Features	PCB Layer Count
EK-LM3S811	Evaluation Board	LM3S811	LQFP48	ADC, motion control	4

**Table 2. Stellaris Example Designs (continued)**

Part Number	Description	Stellaris Devices	Device Package	Key Features	PCB Layer Count
EK-LM3S1968	Evaluation Board	LM3S1968	LQFP100	ADC, motion control	4
EK-LM32965	CAN Evaluation Board	LM3S2965	LQFP100	CAN	4
EK-LM3S3748	USB Evaluation Board	LM3S3748	LQFP100	USB	4
EK-LM3S6965	Ethernet Evaluation Board	LM3S6965	LQFP100	Ethernet	4
EK-LM3S8962	CAN and Ethernet Evaluation Board	LM3S8962	LQFP100	CAN, Ethernet	4
EK-LM3S9x90	Evaluation Board	LM3S9x90	LQFP100	USB, Ethernet	4
EK-LM3S9x92	Evaluation Board	LM3S9x92	LQFP100	USB, Ethernet	4
EK-LM4F232	Evaluation Board	LM4F232H5QD	LQFP144	USB, hibernate, real-time clock	6
DK-LM3S9B96	Development Kit	LM3S9B96	LQFP100	USB, CAN, Ethernet, EPI	4
DK-LM3S9D96	Development Kit	LM3S9D96	LQFP100	USB, CAN, Ethernet, EPI	4
RDK-Stepper	Stepper Motor Control RDK	LM3S617	LQFP48	Motor control	2
RDK-ACIM	AC Induction Motor RDK	LM3S818	LQFP48	High-voltage motor control	2
RDK-IDM-L35	Intelligent Display Module RDK	LM3S1958	LQFP100	Serial, digital, analog connectivity options	4
RDK-BDC24	Brushed DC Motor Control RDK	LM3S2616	LQFP64	CAN, motor control	2
RDK-S2E	Serial to Ethernet Module RDK	LM3S6432	BGA108	Ethernet	4
RDK-IDM	Intelligent Display Module RDK with Ethernet	LM3S6918	LQFP100	Ethernet	4
RDK-BLDC	Brushless DC Motor Control RDK	LM3S8971	LQFP100	CAN, Ethernet, motor control	2
RDK-IDM-SBC	Intelligent Display Single-Board Computer	LM3S9B92	LQFP100	Ethernet, USB, EPI	4

## 7 Conclusion

Applying good system-design practices from the earliest design stages ensures a successful board bring-up. The design process should include thorough design-reviews using the information in this application note, other embedded system design resources, and reports created by the design team. These efforts will be rewarded with a reliable and properly performing Stellaris microcontroller-based design.

The use of the StellarisWare<sup>®</sup> Peripheral Driver Library also minimizes software changes to the start-up routines that configure the I/O, enabling application code to be moved to the new devices with minimal functional changes.

## 8 References

The following related documents and software are available on the Stellaris web site at [www.ti.com/stellaris](http://www.ti.com/stellaris):

- *Stellaris Microcontroller Data Sheet*
- *Stellaris Microcontroller Errata*
- *StellarisWare Peripheral Driver Library User's Guide*
- Stellaris Peripheral Driver Library

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Mobile Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Transportation and Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

TI E2E Community Home Page

[e2e.ti.com](http://e2e.ti.com)

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2011, Texas Instruments Incorporated