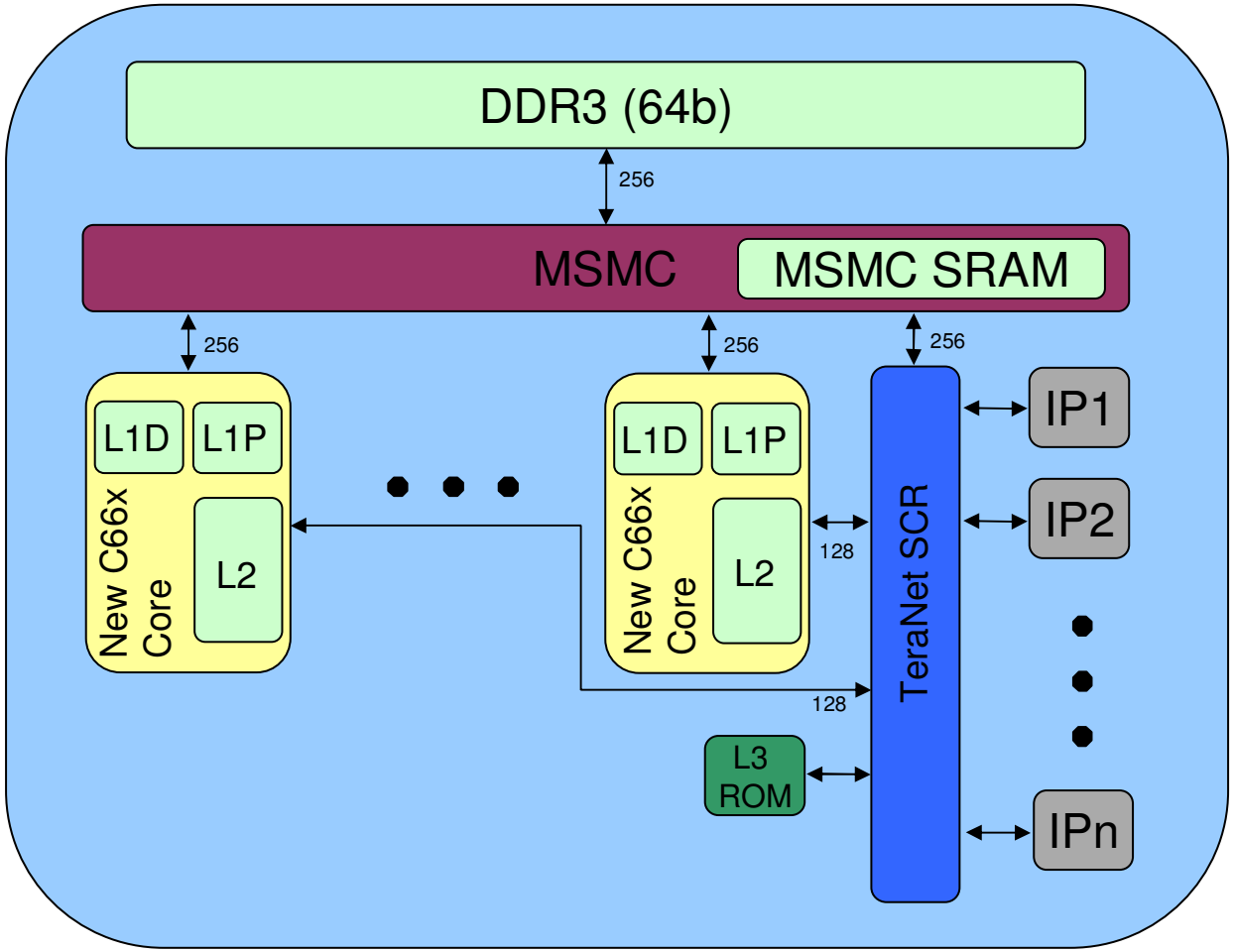
Keystone: Memory Architecture

Nov, 2011

Outline

- Keystone Memory Topology
- Multi-core Shared Memory Controller (MSMC)
- Memory Protection and Address Extension (MPAX)
- DDR Performance Comparison: C6678 VS C6472

Keystone Memory Topology (1/2)



- L1D – 32KB Cache/SRAM
- L1P – 32KB Cache/SRAM
- L2 - Cache/SRAM
  - 1024KB Nyquist
  - 512KB Shannon
- **MSMC**
  - MSM – Shared SRAM
    - 2048KB Nyquist
    - 4096KB Shannon
  - DDR3 – Up to 8GB
- L3 ROM – 128KB

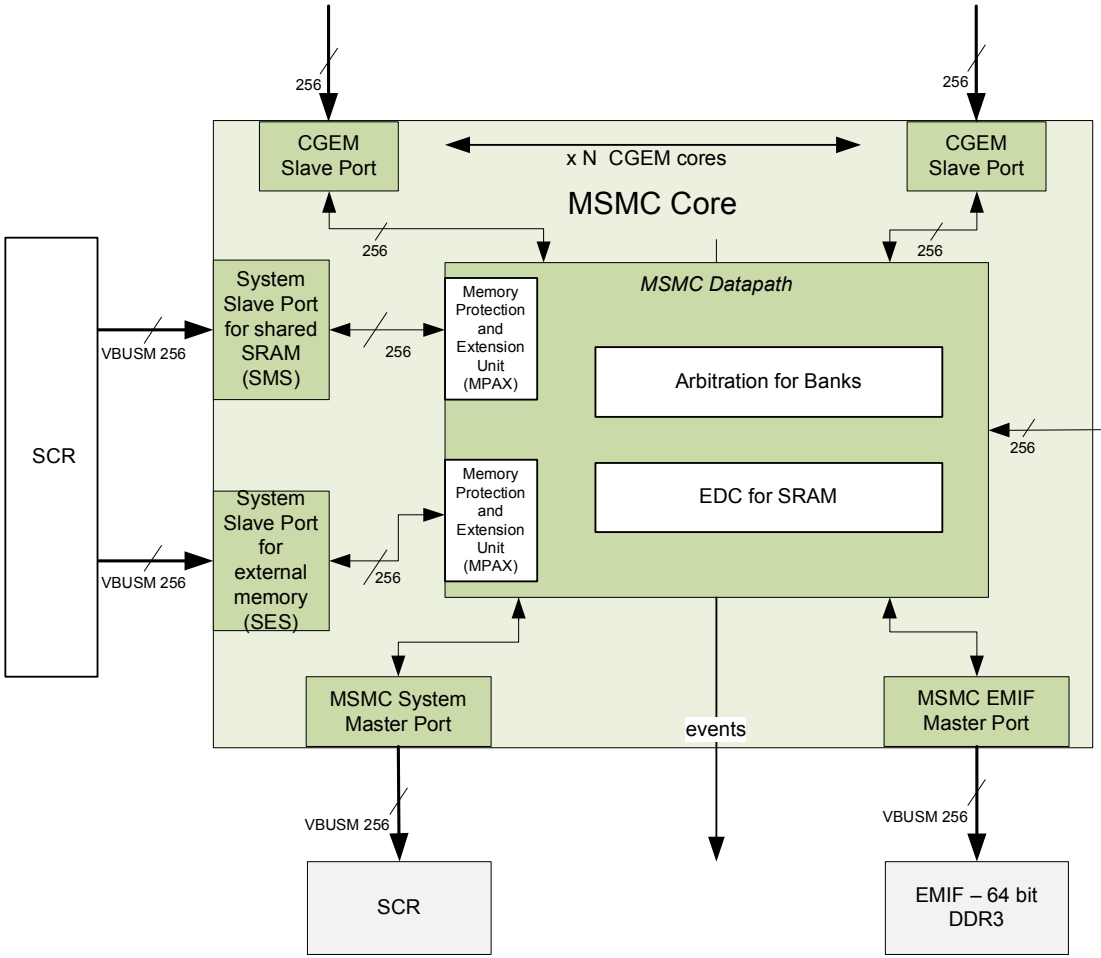
L1D & L1P Cache Options – 0KB, 4KB, 8KB, 16K or 32KB

L2 Cache Options – 0KB, 32KB, 64KB, 128KB, 256KB, 512KB, 1024KB*

* Only Nyquist supports 1024KB L2 Cache

SCR – Switched central resource

Multi-core Shared Memory Controller (MSMC) Block Diagram



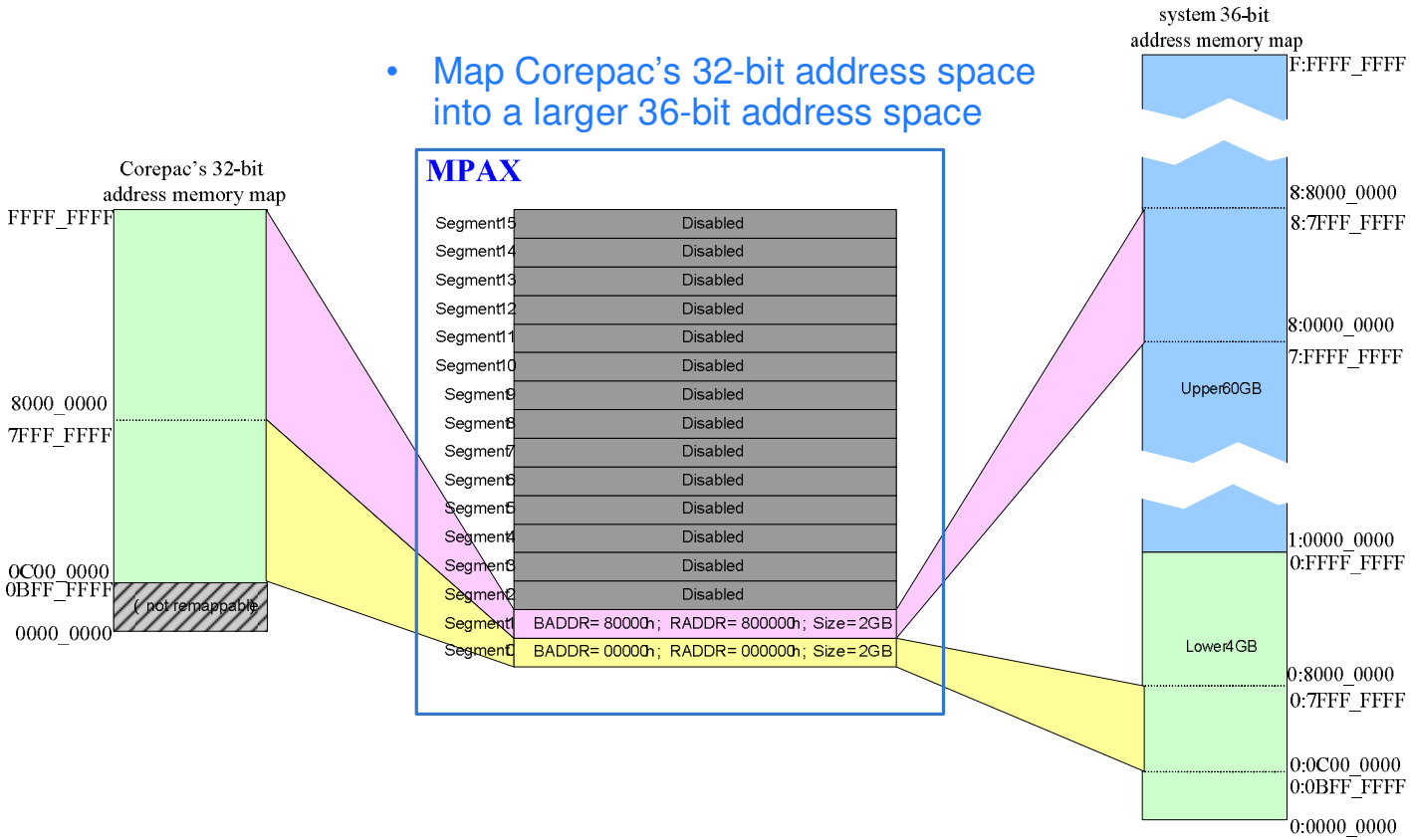
Only the logical address from 0x0C00_0000 to 0xFFFF_FFFF shall be translated through MSMC.

- One slave interface per CorePac (256 bits @ CPUCLK/2)
  - Uses a 36 bit address extended inside a CorePac core
- Two slave interfaces (256 bits @ CPUCLK/2) for access from system masters
  - SMS interface for accesses to MSMC SRAM space
  - SES interface for accesses to DDR3 space
  - Both interfaces support memory protection and address extension
- One master interface (256-bits @ CPUCLK/2) for access to the DDR3 EMIF
- One master interface (256 bits @ CPUCLK/2) for access to system slaves

Memory Protection and Address Extension (MPAX)

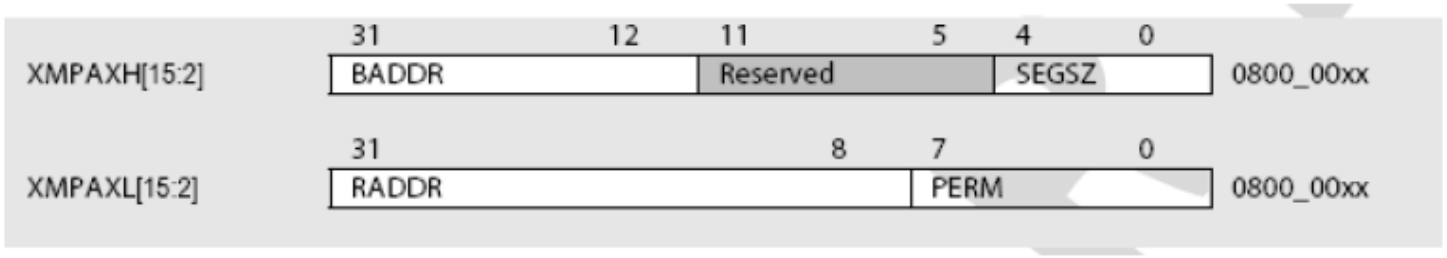
Why bring MPAX?

- Map Corepac's 32-bit address space into a larger 36-bit address space



MPAX Implementation

- MPAX Segment is defined for address extension and memory protection
  - Map a 32-bit address to a 36-bit address.
  - Controls access.
  - Segment register layout



Field	Name	Meaning
BADDR	Base Address	Upper bits of address range to match in C66x CorePac's native 32-bit address space
SEGSZ	Segment Size	Segment size. Table below indicates encoding.
RADDR	Replacement Address	Bits that replace and extend the upper address bits matched by BADDR
PERM	Permissions	Access types allowed in this address range.

Address Extension Feature

- Each segment provides a replacement address.
  - The replacement address is constrained to power-of-2 boundary equal to the size.
- Expand from 4GB to 64GB address space.
  - Note that, even if the MPAX supports a 64GB address space, Nyquist/Shannon may provide a smaller address space.
- Map identical virtual addresses to different physical addresses.
  - This may help the use of code that is shared between different CorePacs. Absolute references to private variables don't need to be redirected.
- Map different virtual addresses to a single physical address.
  - This allows giving different semantics to the same memory. For instance, by having cacheable and non-cacheable access to a memory segment you can overcome the rough (16 MB) granularity of the MAR pages. Note that prefetching is also enabled/disabled per MAR page.

Memory Protection

- The table below indicates which modes are supported in memory protection of MPAX. Through program each segment register's field "PERM", the related memory's access attribute can be controlled.

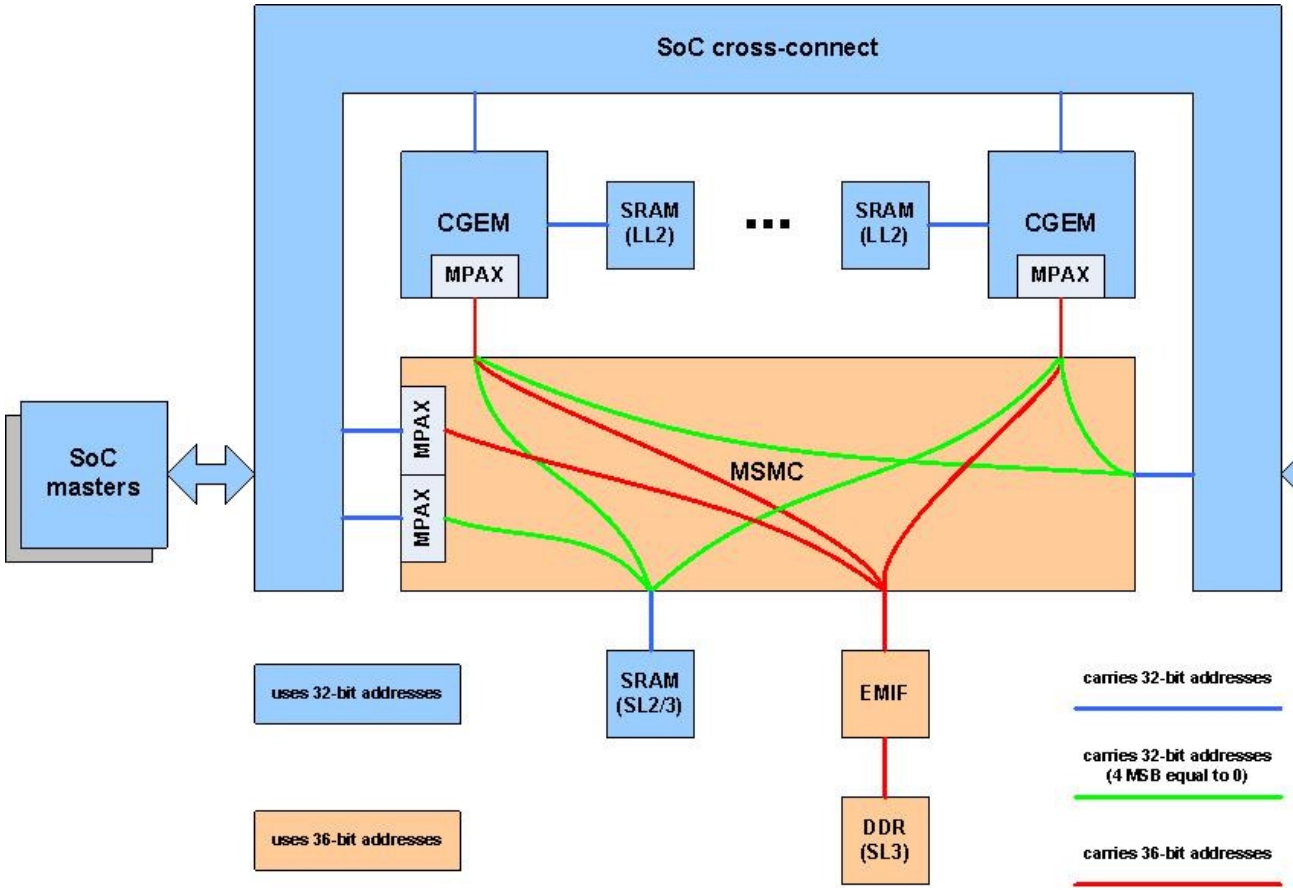
Figure 7-2 MPAXL.PERM Subfield Layout

7	6	5	4	3	2	1	0
Rsvd	Rsvd	SR	SW	SX	UR	UW	UX

Table 7-3 Summary of Permission Bits in MPAXL.PERM

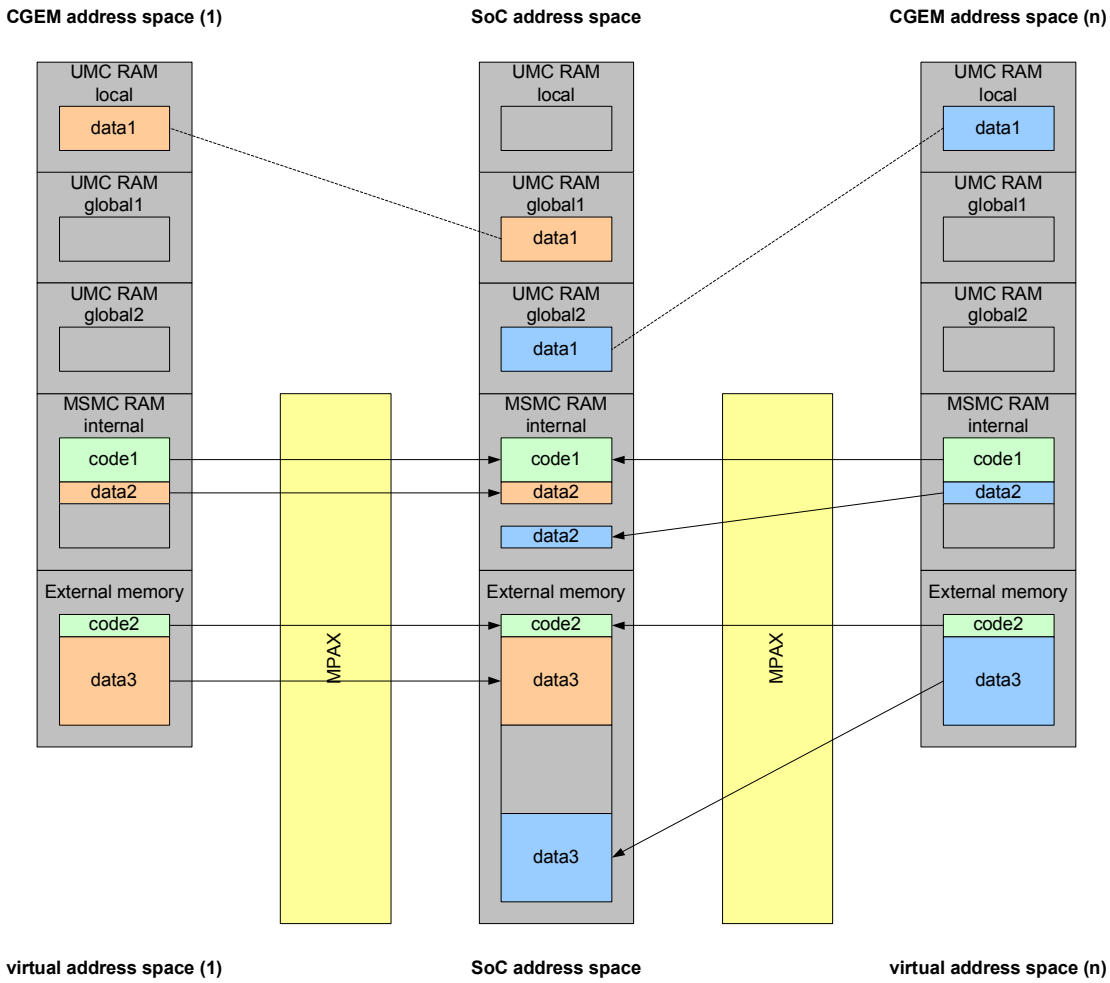
Bit	Meaning When Set	Bit	Meaning When Set
SR	Supervisor mode may read from segment	UR	User mode may read from segment
SW	Supervisor mode may write to segment	UW	User mode may write to segment
SX	Supervisor mode may execute from segment	UX	User mode may execute from segment

MPAX in the System



- **Corepac MPAX**
  - -- 16segments @Corpac
- **MSMC MPAX**
  - -- SES: 8segments @Privilege ID of the system masters
  - -- SMS 8segments @Privilege ID of the system masters

Multi-Core Virtual Memory



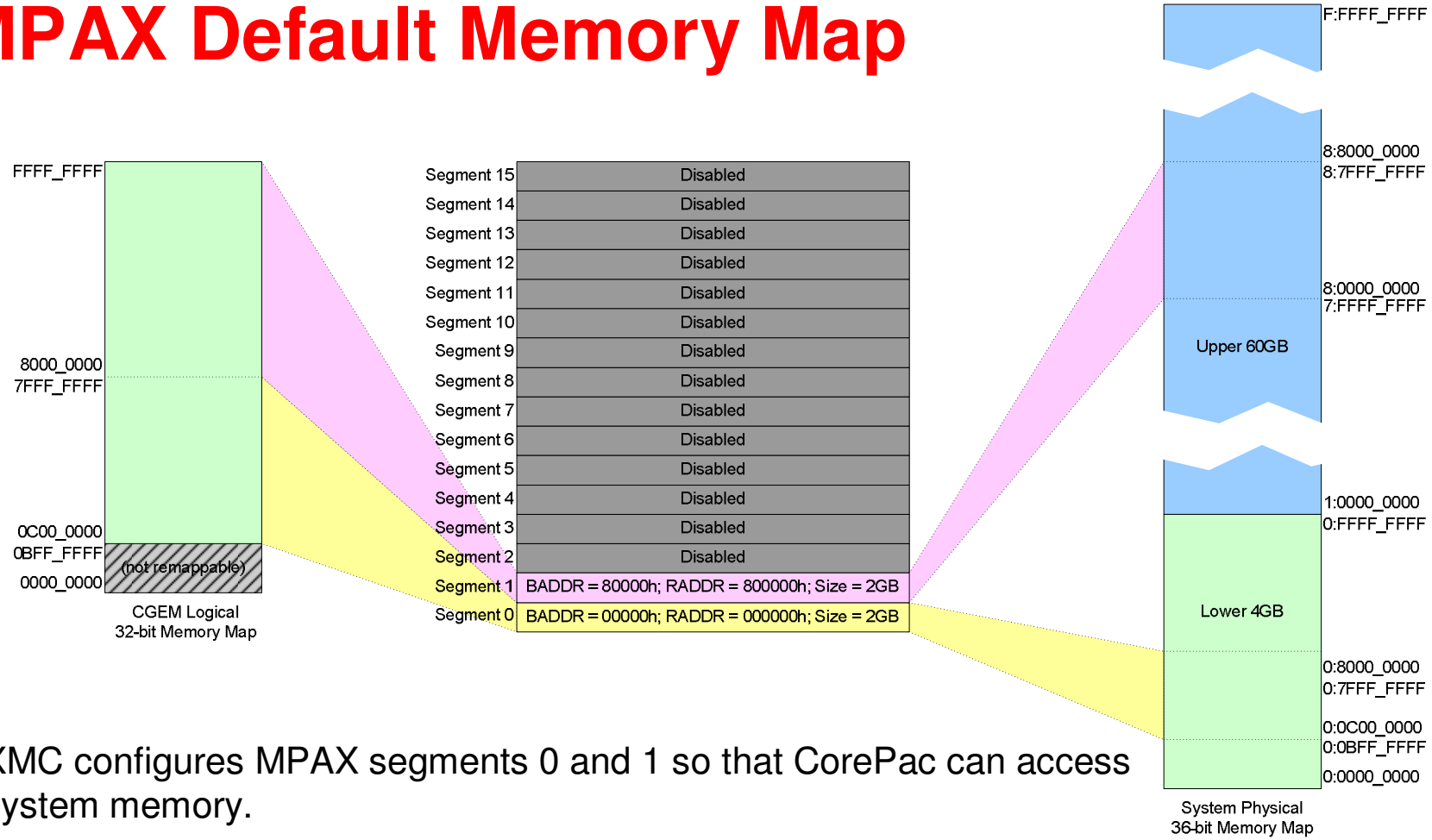
... provides more external memory per core

... isolates operating systems/applications running on different cores

... DOES NOT isolate processes running on the same core!

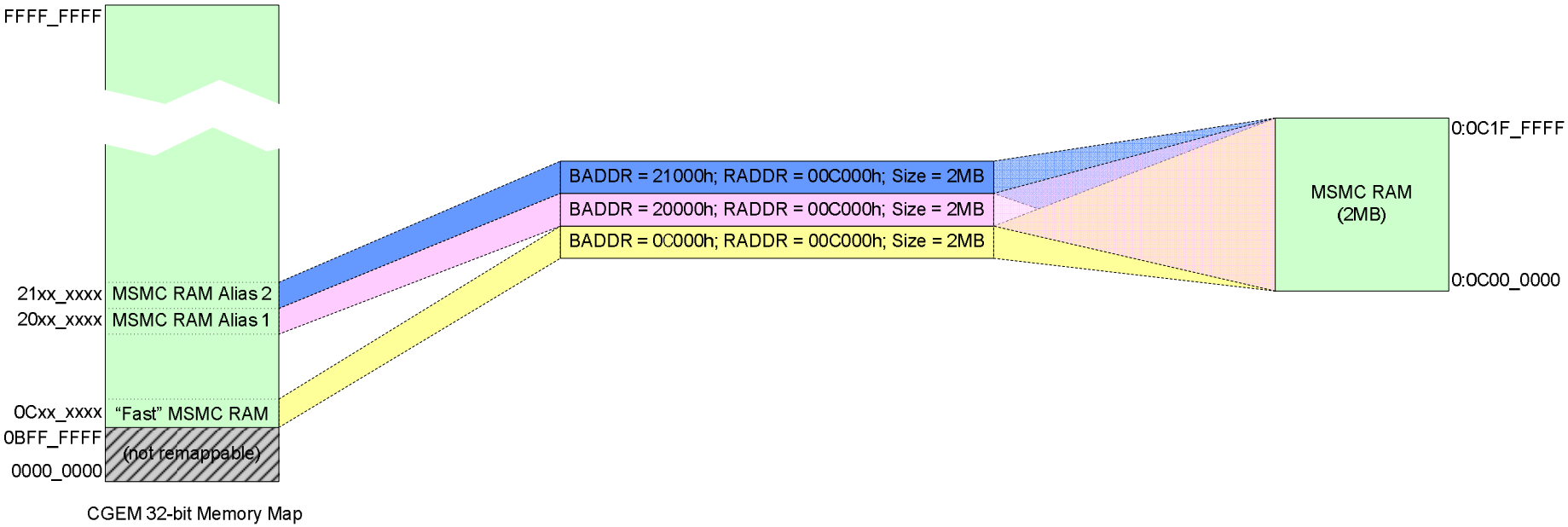
... easily supports shared programs

MPAX Default Memory Map



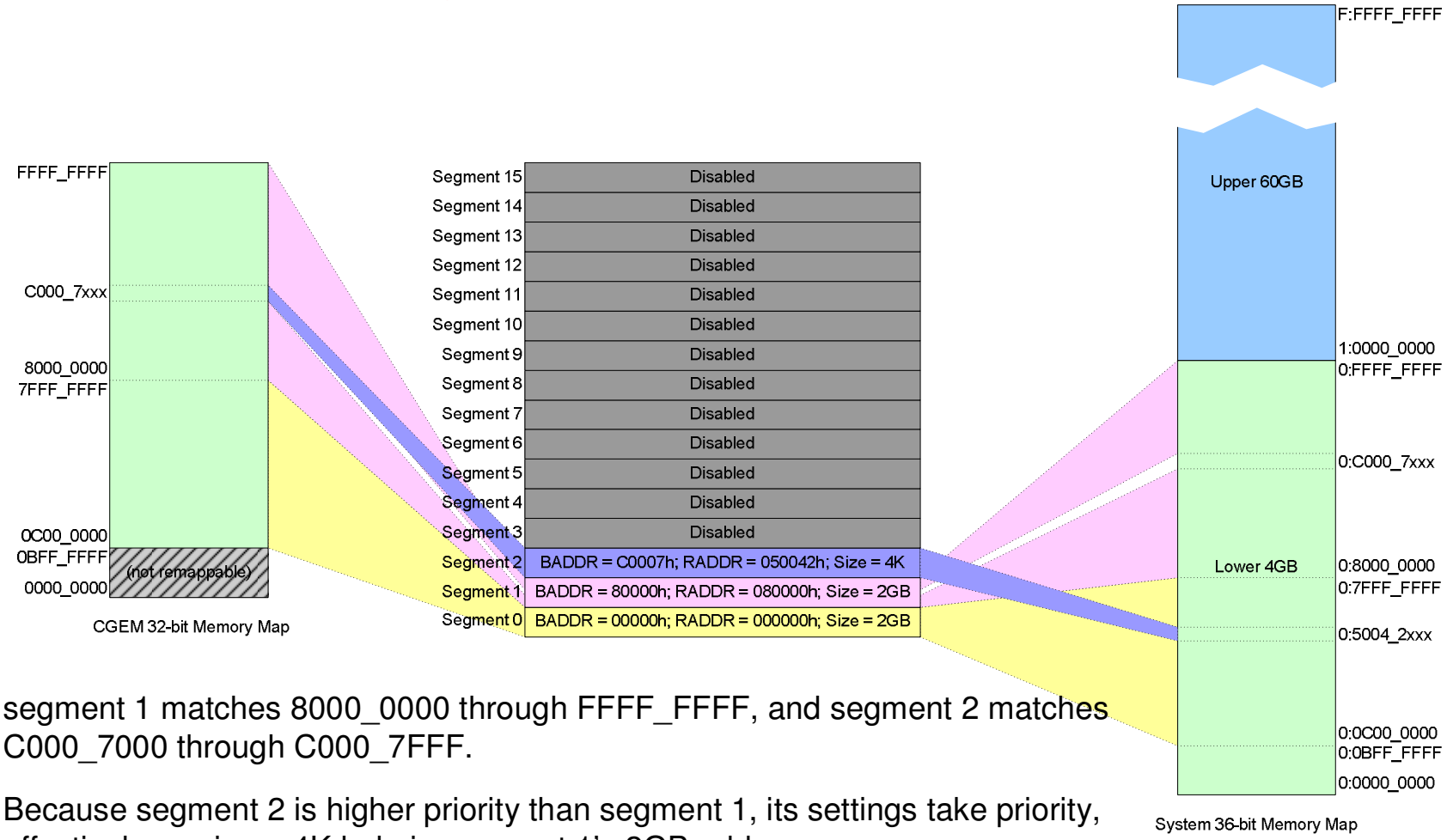
- XMC configures MPAX segments 0 and 1 so that CorePac can access system memory.
- The power up configuration is that segment 1 remaps 8000_0000 – FFFF_FFFF in CorePac's address space to 8:0000_0000 – 8:7FFF_FFFF in the system address map.
  - This corresponds to the first 2GB of address space dedicated to EMIF by the MSMC controller.

MPAX MSMC Aliasing Example



- Example shows 3 segments to map the MSMC RAM address space into CorePac's address space as three distinct 2MB ranges. By programming the MARs accordingly, the three segments could have different semantics.
- Accesses to MSMC RAM via this alias do not use the "fast RAM" path and incur additional cycles of latency.

MPAX Overlayed Segments Example



- segment 1 matches 8000_0000 through FFFF_FFFF, and segment 2 matches C000_7000 through C000_7FFF.
- Because segment 2 is higher priority than segment 1, its settings take priority, effectively carving a 4K hole in segment 1's 2GB address space.
- Furthermore, it maps this 4K space to 0:5004_2000 - 0:5004_2FFF, which overlaps the mapping established by segment 2. This physical address range is now accessible by two logical address ranges.

DDR Performance Comparison
C6678 VS C6472

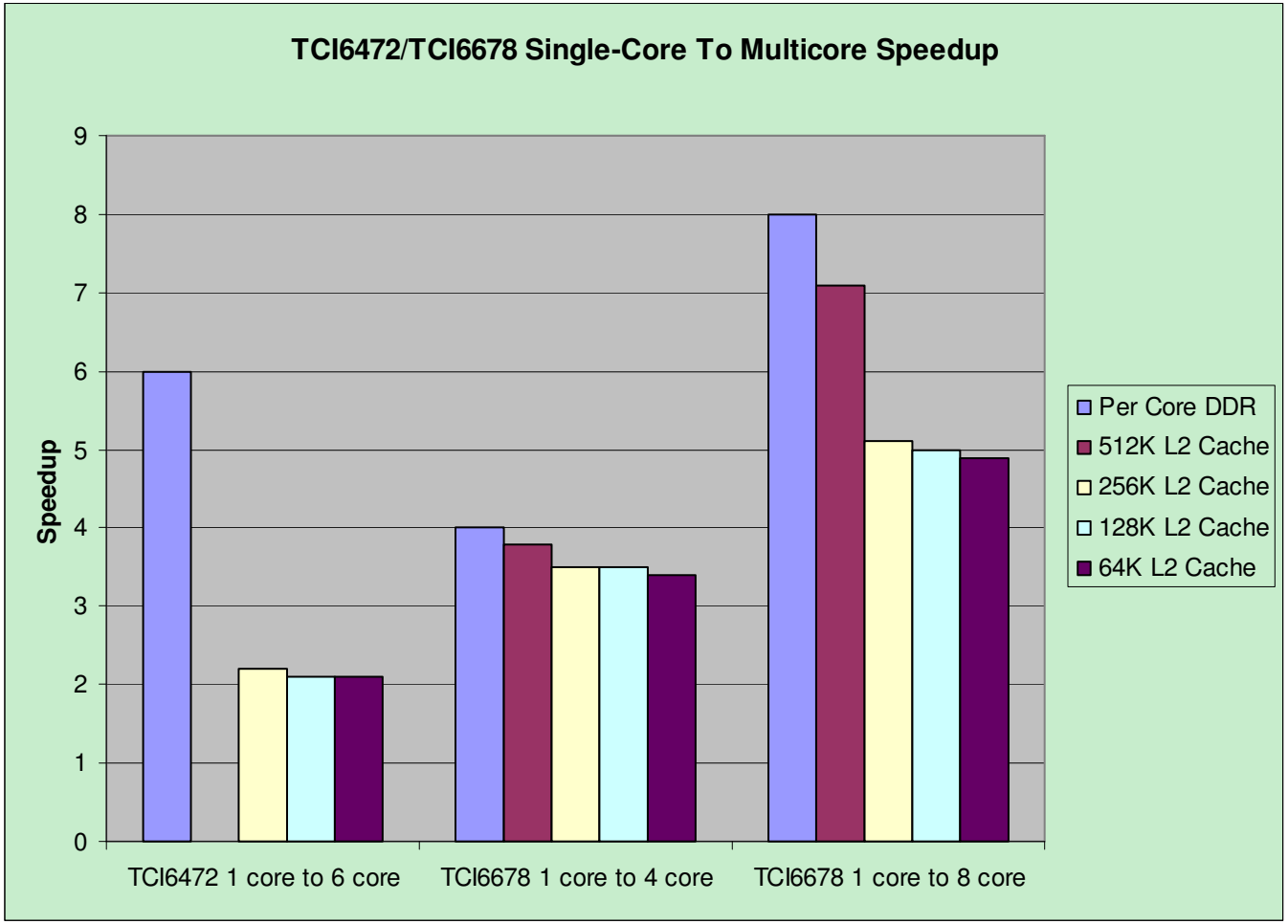
Background

- The assumption is there is an application which processes network operations (header manipulation, payload repacking, routing) across many channels/connections/contexts.
- The active code/data for this application is about 1MB.
- The TCI6472 (Tomahawk) and TCI6678 (Shannon) devices are compared.

Configuration

- All program and data is placed in DDR.
- The cache size is varied to demonstrate the potential performance gain on TCI6678.
- TCI6678 is running at 1GHZ with 64 bit DDR3-1066, and the TCI6472 is running at 500MHZ with 32 bit DDR2-533.

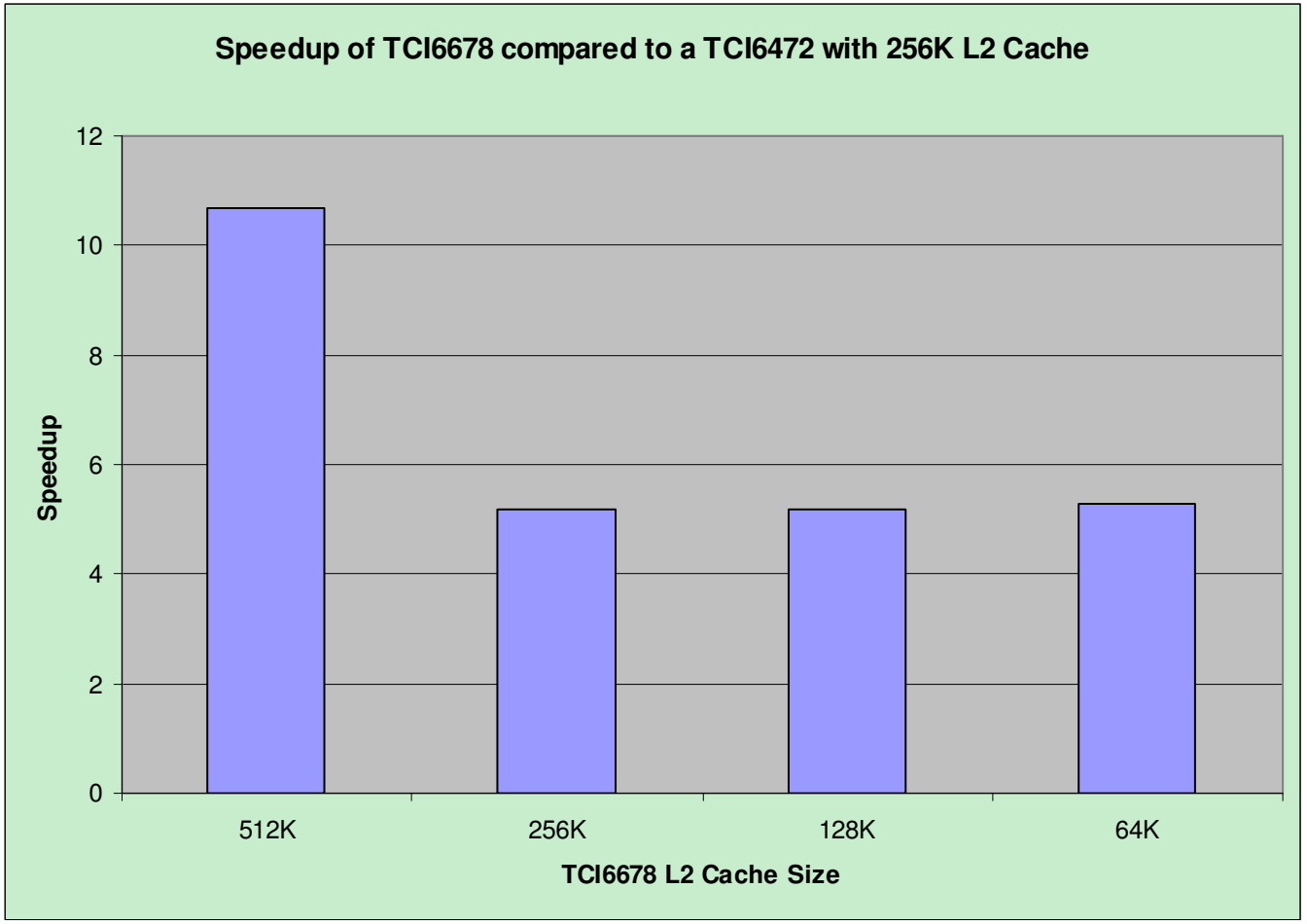
Multicore Speedup



Multicore Speedup Summary

- For this application
  - When scaling from single core to multicore on the same device, the “Per Core DDR” column indicates the hypothetical performance as if the each device had separate DDR per core.
  - Scaling from one core to all six cores on the TCI6486, the capacity is scaled by approximately 2.1x regardless of cache size. This is due to DDR bandwidth constraints. If there were no DDR constraints, then it would have scaled by 6x.
  - Scaling from one core to all 8 cores on the TCI6608 is approximately 5x for cache sizes 64K-256K. However, when using the larger 512K cache allows the capacity to scale by about 7x. **Thus the larger cache is allowing full entitlement to the 8x cores on the device.**

Device Level Speedup



Device Level Speedup Summary

- This shows the total capacity of a TCI6678 with various cache sizes compared to the total capacity of a TCI6472 with a 256K L2 cache.
- When using cache sizes <= 256K on the TCI6678, the TCI6678 has about 5x more capacity than a TCI6472.
- The TCI6678 also adds a 512K cache size option. The TCI6678 with 512K has about 11x the capacity of a TCI6472 with 256K cache.
  - This shows the potential value of the larger L2 cache size only available on the TCI6678.

Summary

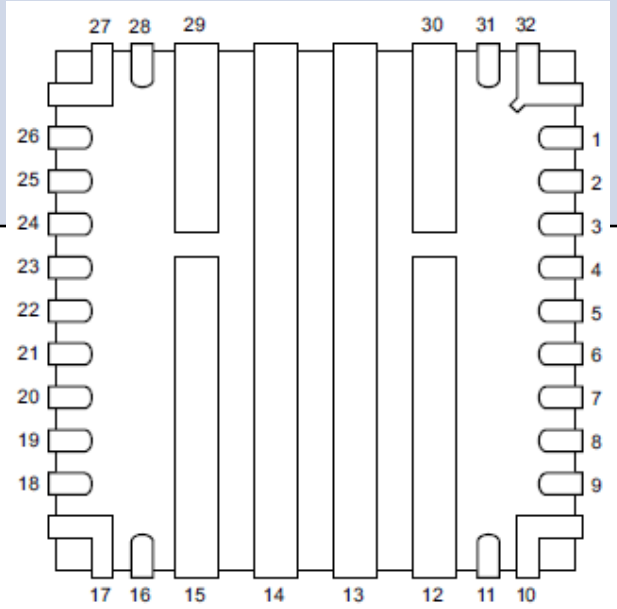
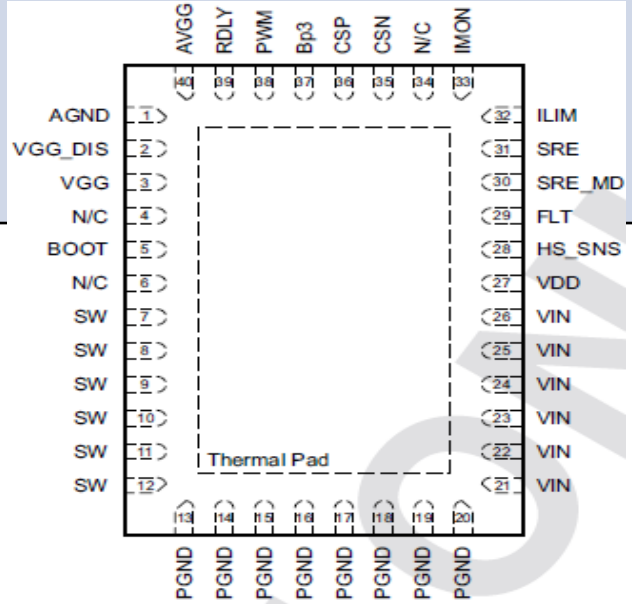
- The TCI6678 device has substantially improved DDR performance relative to TCI6472.
  - There are 2.7x more cycles available on the TCI6678 (8 GHz vs 3 GHz).
  - Improved DDR performance allows the TCI6678 to realize capacity gains greater than 2.7x.
  - For the EEMBC* networking application, the realized capacity gain is 5x.

*EEMBC: Embedded Microprocessor Benchmark Consortium

For More Information

- For more information, refer to the below user guide:
  - C66x CorePac User's Guide (http://www.ti.com/litv/pdf/sprugw0b)
  - Multicore Shared Memory Controller (MSMC) for KeyStone Devices User Guide (http://www.ti.com/litv/pdf/sprugw7a)
- For more questions, visit the TI Deyisupport forum: http://www.deyisupport.com/

C667x Power Design Solution Update

AVS Solution	UCD92xx + UCD7242	UCD92xx + UCD74111
Recommended Solution	Yes	Yes
Available	Now	Q1/2012
Features	• High Efficiency (~85% for AVS supply; **UCD7242** based power stage) • **High density, support Up to 2 AVS supplies** • Digital Power Controller with advanced power management • **Primary solution for multi-chip designs**	• Ultra-High Efficiency (~90% for AVS supply; **UCD74111** based power stage) • Easy for thermal design • Easy for SMT • Digital Power Controller with advanced power management • **Development board solution for single-chip designs**
Package		

For More Information

- For more information, refer to the below user guide:
  - Hardware Design Guide for KeyStone Device (http://www.ti.com/litv/pdf/sprabi2)

- For more questions, visit the TI Deyisupport forum: http://www.deyisupport.com/

Thank you!