Embedded Processing Portfolio for Ultrasound
High performance, programmable platform

- Processor **performance** speeds image analysis – faster, clearer results
- **Power/size efficient** processors enable portability – point of care imaging
- **Programmable DSPs** enable software upgrades – extend product life
- Complete line of **Code compatible devices** – provides **scalable platform** to address portable through high-end cart-based systems
TI’s Medical Imaging Processors

Mission: to enable performance imaging every doctor demands

TI DSP Enables

- Advances in medical processing
  - Latest algorithms
    - Improved image quality
    - More accurate diagnosis
    - Emerging Features
  - Innovative applications
    - safer, non-invasive
  - Real-time diagnosis
  - Product differentiation

TI DSP Solutions

- Complete product line of high performance DSPs
  - Software programmable
    - Flexible
    - Adaptable
    - Upgradeable
  - Real-time performance
    - 1.25GHz single core
    - 320GMACs/160GFlops multi-core
  - Medical driven roadmap

Low power processors and SOCs

- Longer battery life
- Smaller form factor

- Highly integrated
- Power efficient
- C64x+ & C66x core DSP
- OS, GUI, MMI, display
- High connectivity

Portable medical applications

- Sitara™
- C6-Integra™
- Davinci™
Ultrasound system – Where DSP fits

- DSP
  - RF Demodulation
  - B-Mode
  - Color Flow
  - Spectral Doppler
  - Scan Control

- SOC (DSP+MPU)
  - Scan Conversion
  - Speckle Reduction
  - System Control
  - O/S
  - Display
  - Storage

Product Availability and Design Disclaimer - The system block diagram depicted above and the devices recommended are designed in this manner as a reference. Please contact your local TI sales office or distributor for system design specifics and product availability.

Texas Instruments
Multi-core DSP
Console Ultrasound Solution

<table>
<thead>
<tr>
<th>Decimation</th>
<th>B-Mode</th>
<th>Color</th>
<th>Doppler</th>
</tr>
</thead>
<tbody>
<tr>
<td>• RF Demod</td>
<td>• Detection</td>
<td>• Wall Filter</td>
<td>• FFT</td>
</tr>
<tr>
<td></td>
<td>• Compression</td>
<td>• Velocity Est</td>
<td>• Peak Mean Est</td>
</tr>
<tr>
<td></td>
<td>• Scan Conv</td>
<td>• Power Est</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Speckle Red</td>
<td>• Scan Conv</td>
<td></td>
</tr>
</tbody>
</table>

- FPGA beam forms and routes data to DSP via SRIO
- C6657 (2-core) for scan control & back end image processing algorithms.
- PC performs system control, MMI, interface to PACs
- Lower power & system cost solution
Multi-core DSP
Portable Ultrasound Solution

<table>
<thead>
<tr>
<th>Decimation</th>
<th>B-Mode</th>
<th>Color</th>
<th>Doppler</th>
</tr>
</thead>
<tbody>
<tr>
<td>• RF Demod</td>
<td>• Detection</td>
<td>• Wall Filter</td>
<td>• FFT</td>
</tr>
<tr>
<td>• Detection</td>
<td>• Compression</td>
<td>• Velocity Est</td>
<td>• Peak&amp;Mean Est</td>
</tr>
<tr>
<td>• Scan Conv</td>
<td>• Speckle Red</td>
<td>• Power Est</td>
<td>• Scan Conv</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>System Ctrl</th>
<th>O/S</th>
</tr>
</thead>
<tbody>
<tr>
<td>• MMI</td>
<td>• Linux</td>
</tr>
<tr>
<td>• PACs/i</td>
<td>• Android</td>
</tr>
<tr>
<td>• Mode Switch</td>
<td>• QT</td>
</tr>
<tr>
<td>• Cineloop Mgmt</td>
<td></td>
</tr>
</tbody>
</table>

- FPGA beam forms and routes data to DSP via SRIO
- C6657 (2-core) implements mid-back end image processing algorithms
- AM3874 performs system control, MMI, interface to PACs
- C6657 + AM3874 = ~4w total

![Diagram showing the components and connections of the system](image-url)
SOC Based
Ultra-Portable Ultrasound Solution

- FPGA beam-former + RF demod and routes data to SOC via PCIe
- ARM Cortex A8 performs system control, MMI, interface to PACs
- DSP performs back end image processing
- Video & Graphics h/w accelerator
## Multi-core DSP Based Performance Ultrasound Solution

<table>
<thead>
<tr>
<th></th>
<th>B-Mode</th>
<th>Color</th>
<th>Doppler</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF Demod</td>
<td>Detection</td>
<td>Wall Filter</td>
<td>FFT</td>
</tr>
<tr>
<td>3D/4D</td>
<td>Compression</td>
<td>Velocity Est</td>
<td>Peak/Mean Est</td>
</tr>
<tr>
<td>Elastography</td>
<td>Scan Conv</td>
<td>Power Est</td>
<td></td>
</tr>
<tr>
<td>Speckle Red</td>
<td></td>
<td>Scan Conv</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### System Ctrl
- MMI
- PACs if
- Mode Switch
- Cineloop Mgmt

### O/S
- Linux
- Android
- QT

### Key Features
- FPGA beam forms and routes data to DSP via SRIO
- C6678 standard mid processing + 3D/4D, Elastography, & Speckle Reduction
- AM3874 performs system control, MMI, interface to PACs
C6655/ C6657 (Sample Now!)

- **New C66x Core**
  - 2 C66x Cores @ 1.0GHz nominal (1.4GHz max)
  - C6657 (2 Core), C6655 (1 core)
  - High Performance Fixed & Floating Point DSP Cores

- **Power Optimized Design**
  - Target 3.5W for 2 Core, 2.5W for 1 Core implementation (85c case @ 1Ghz)

- **Keystone Multi-Core Architecture**
  - Multicore Navigator, TeraNet, Hyperlink

- **Memory Architecture**
  - 1MB Local L2 per Core
  - 1MB Multicore Shared Memory (MSM)
  - Boot ROM, DDR3-1600MHz (32-bit)
  - Address Translation & ECC

- **Interfaces**
  - 4x RapidIO rev 2.1 (1x4, 2x2, 1x2+2x1)
  - 2 lanes PCIe Gen II
  - 10/100/1000 Mbps Ethernet SGMII ports
  - Universal Parallel Port (16-bit) Muxed with EMIF -16
  - I2C, SPI, 2x McBSP (Mux), 32 GPIO, 2 x UART, 4x Timers64, Semaphore

- **Other**
  - 2x VCP2, 1x TCP3d
  - Multicore debugging (embedded trace per core / chip)
  - 0.8 mm pitch flip chip package
  - 21x21 package
  - Ext Temp Range: -55C to 105C
  - 40nm High Performance Node
  - Smart reflex
Shannon (TMS320C6678) – Block Diagram

- Multi-Core KeyStone SoC
- Fixed/Floating CorePac
  - 8 CorePac @ 1.25 GHz
  - 4.0 MB Shared L2
  - 320G MAC, 160GFLOP, 60 GDFLOPS
  - ~10W
- Navigator
  - Queue Manager, Packet DMA
- Multicore Shared Memory Controller
  - Low latency, high bandwidth memory access
- 3-port GigE Switch (Layer 2)
- PCIe gen-2, 2-lanes
- SRIO gen-2, 4-lanes
- HyperLink
  - 50G Baud Expansion Port
  - Transparent to Software
DM8148 Processor

Cores
- ARM Cortex A8™ (MPU) up to 1 GHz
- C674x™ Floating Point DSP Core up to 750 MHz

Memory
- ARM: 32KB L1I-Cache, 32KB L1 D-Cache, 256K L2
- DSP: 32KB L1I-Cache, 32KB L1 D-Cache, 256K L2
- Two DDR-800 Controllers

Coprocessors/Subsystem
- HD VICP 2.0 Accelerator at 320 MHz
  - Real-Time HD Encode/Decode
- 3D Graphics engine
- Display Subsystem

Peripherals
- Gigabit EMAC Switch
- USB 2.0 Ctlr/PHY x 2
- PCIe 2.0
- SATA 3.0Gbps
- DDR3 – 800 x2
- SD/SDIO x3
- McBSP x6, McBSP
- SPI, GPIO, I2C, UART, DCAN

Power
- Total Power – Typical <4 W

Package
- 23x23, 0.8mm pitch, 684 ball BGA
  - Via Channels enable low cost design rules – 4 mil traces and 10/20 mil escape vias

Back to: DM roadmap | product positioning
Using DSPs & SOCs in Ultrasound Systems

• TI’s C6678 DSP with new C66x floating point core provides high performance signal processing capabilities at low power
  – C6657 dual core DSP can perform processing for mid-range system
  – Upgrade to 4 or 8 core C6674/C6678 for more advanced algorithms

• C66x DSPs are well suited for processing such as:
  – B-Mode (Detection, Compression)
  – Color (Wall Filter, Velocity & Power estimation)
  – Doppler (FFT, Peak Mean estimation)
  – Scan Conversion
  – 3D/4D, Elasto-graphy, Speckle Reduction

• Combining an FPGA for beam formation/routing and Sitara ARM SOC C66x DSPs can provide a flexible, low-power solution for digital ultrasound systems.
  – High Level Language “Eclipse” development environment
  – On-Chip DMA & Multicore Navigator for data movement.
  – McBSP ports address I/O needs for CW Doppler & audio
Using DSPs & SOCs in Portable Ultrasound Systems

- TI’s low-power Davinci SoCs allow flexibility on the back-end SoC for various display options, image filtering and target identification on a single chip:
  - C674x DSP (fixed-/floating-point DSPs)
  - Cortex-A8 for peripheral and communications control
  - 3D graphics engine for rich UIs
  - Rich display sub-system for multiple HD displays
  - HD video encode/decode accelerators (Davinci devices only)

- High system connectivity with peripherals such as:
  - Gigabit ethernet
  - PCIe
  - USB
  - SATA
  - SPI/GPIOs/more…
Complete DSP & ARM MPU Software Solutions by TI

**FREE** Development license to use our Linux, Android, or WinCE Board Support Packages (BSP) / Software Development Kits (SDK)

* For use on our ARM, ARM+DSP, and ARM+DSP+Multimedia Processors
* Each release seamlessly and scalable works across all products
Medical Software Toolkit 2.0

- Optimized implementations of commonly used C64x+/C66x DSP processing blocks
- Source Code:
  - Ultrasound:
    - B-mode (Envelop Detection & Compression)
    - DAS Receive Beam-forming
    - Doppler Processing
    - RF Demodulation and Decimation
    - Scan Conversion
  - Optical Coherence Tomography
    - Cubic Spline Interpolation
    - Optimized FFT
  - 3D Rendering
    - Affine Warp

Request download at: [http://focus.ti.com/docs/toolsw/folders/print/s2meddus.html](http://focus.ti.com/docs/toolsw/folders/print/s2meddus.html)
Medical Ultrasound Demo (MIDAS) Rev. 2
All B-Mode, Color Flow, and Scan Conversion Processing on OMAP3530!

**ARM Cortex A-8**
- 600MHz
- Runs Linux O/S
- User Interface, Control, Display

**C64x+ DSP**
- 430MHz
- Runs Ultrasound Algorithms

---

**Input Data Size (Post RF Demod)**

<table>
<thead>
<tr>
<th></th>
<th>Scan Lines</th>
<th>Samples/Scan Line</th>
<th>Bytes/Sample</th>
<th>Ensemble</th>
<th>kB/frame</th>
</tr>
</thead>
<tbody>
<tr>
<td>B-mode + Scan Conversion</td>
<td>128</td>
<td>416</td>
<td>4</td>
<td>-</td>
<td>208</td>
</tr>
<tr>
<td>Color Flow + Scan Conversion</td>
<td>64</td>
<td>256</td>
<td>4</td>
<td>8</td>
<td>512</td>
</tr>
</tbody>
</table>

**Loading**

<table>
<thead>
<tr>
<th></th>
<th>DSP</th>
<th>ARM</th>
<th>ms/fm</th>
</tr>
</thead>
<tbody>
<tr>
<td>B-Mode</td>
<td>19%</td>
<td>6%</td>
<td>15</td>
</tr>
<tr>
<td>B-Mode + Color Flow</td>
<td>46%</td>
<td>21%</td>
<td>28</td>
</tr>
</tbody>
</table>

https://gstreamer.ti.com/gf/project/med_ultrasound/
Medical Imaging DSP
Value Proposition

- **New & innovative algorithms in software**
  Improved image quality & emerging features
  Field upgrades, Flexibility, Adaptive coding

- **Deterministic signal processing architecture**
  Supports latest real-time O/S for predictable & reliable performance

- **Portable imaging applications**
  Low power SOC’s replace PC. (DSP+ARM, Graphics, Video accl…) Longer battery life. Smaller form factor.

- **Scalable platforms: Portable→Value→Premium**
  Code compatible family of products

- **R&D Savings**
  Reuse (code, hardware, development environment)
  No hardware spins, eco’s, & timing closure bottlenecks

- **Time to Market**
  State of the art development tools: (Compilers, trace, emulation)
  Develop & debug in high level language
  Imaglib & Medical Software toolkit, 3d parties

- **Roadmap & Product continuity**
  Long term supplier, Full product line: Analog, DSP, Power, etc…
  10GHz-320GMACs/160GFlop DSP’s today,
  Application support (Field, Factory, domain white papers & app notes)