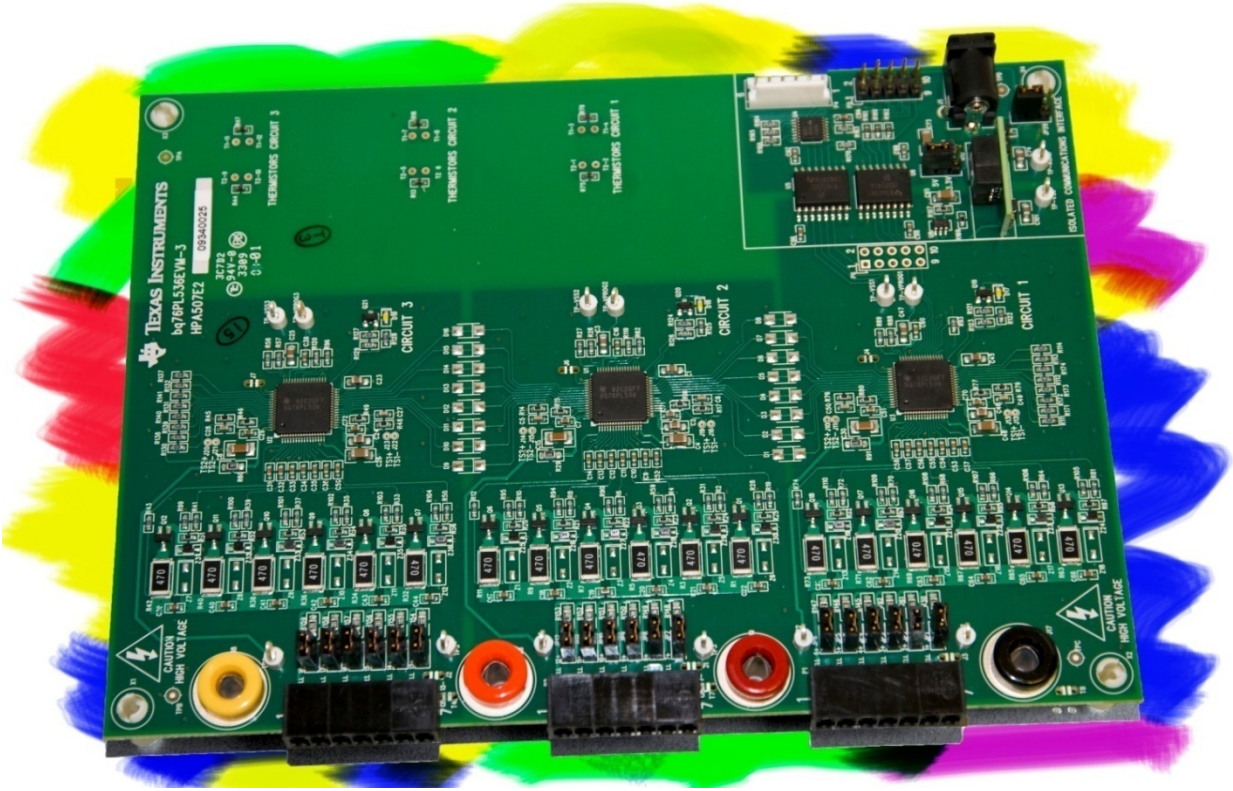
bq76PL536

• Design and Layout Guide •



Abstract

The bq76PL536 is designed to communicate at high speed in the noisy conditions present in automotive and industrial large-format battery applications. These environments are typically filled with nearby noise sources producing fast rise-time signals and broad-spectrum RF interference. Sources include single-phase and 3-phase inverters, dc/dc converters, motor commutation, contactor arc, and even inductively coupled noise from nearby high-current bus bars. For starters, good layout of printed-circuit board (PCB), use of ground planes, and high-quality, low-capacitance shielded cable are required necessities of a successful system. Other contributing factors include minimizing cable distances, careful attention to grounding, keeping cables and PCB assemblies away from noise sources, and taking steps to reduce common-mode noise in the bq76PL536 stack.

This document presents specific PCB layout considerations to optimize over all performance of bq76PL536 by reducing noise to a minimum, improve EMC immunity, random hot plug, improving cable lengths, optimizing ground planes, suppressing ESD/HV transient suppressions and more.

Content

1.0 Mechanisms of ESD Damage in Battery Management Units

1.1 **Inadequate attenuation**. The IC pins will usually be rated for 2kV without damage, so to withstand a 15kV ESD hit, circuitry on the PCB must attenuate the applied voltage spike from 15kV to the 2kV IC rating. External R's and C's can do this job, though most of the work should be done by the Cs since the voltage might even arc across a resistor in the discharge path. Be sure to use very short connections to both ends of decoupling caps, as inductance in the ground connection to the cap is just as harmful as having it in the "hot" side of the connection. When routing PCB traces, remember that ESD will generally head towards capacitors, these should be placed close to the likeliest ESD touch point such as connectors, etc.

1.2 **Capacitive coupling track-to-track.** A voltage spike on one trace can be capacitively coupled on to tracks on adjacent layers in the PCB and also to components mounted to the PCB.

1.3 **Inductive voltage drop**. A fast current surge (high dI/dt) will cause a large voltage drop across the inductance of traces where the current surge flows. If connections to circuitry are made at different points along the trace with the high current surge, there can be large transient voltages between the points. Using wide etch will reduce the inductance along the path that could see the high surge transient.

1.4 **Magnetic coupling**. ESD may produce a high current surge on a PCB trace, which will create a magnetic field around the current-carrying conductor. This current surge will have a very high dI/dt and as such, the varying magnetic field can induce current flow in adjacent etch runs and components, especially circuits with components or etch runs that are parallel and in close proximity to the ESD surge current flow.

1.5 **Improper grounding of ESD protection components**. If the components used to provide ESD transient protection are grounded to the low-current etch runs around sensitive circuits, these will be just another mechanism to couple the ESD transient into where you don't want it. The ground connections to the ESD protection components should be short and wide, as inductance in this connection will simply reduce the effectiveness of the protection. In general, ground planes should be used to decouple ESD wherever possible.

2.0 Design.
2.1 HV Transient Suppression

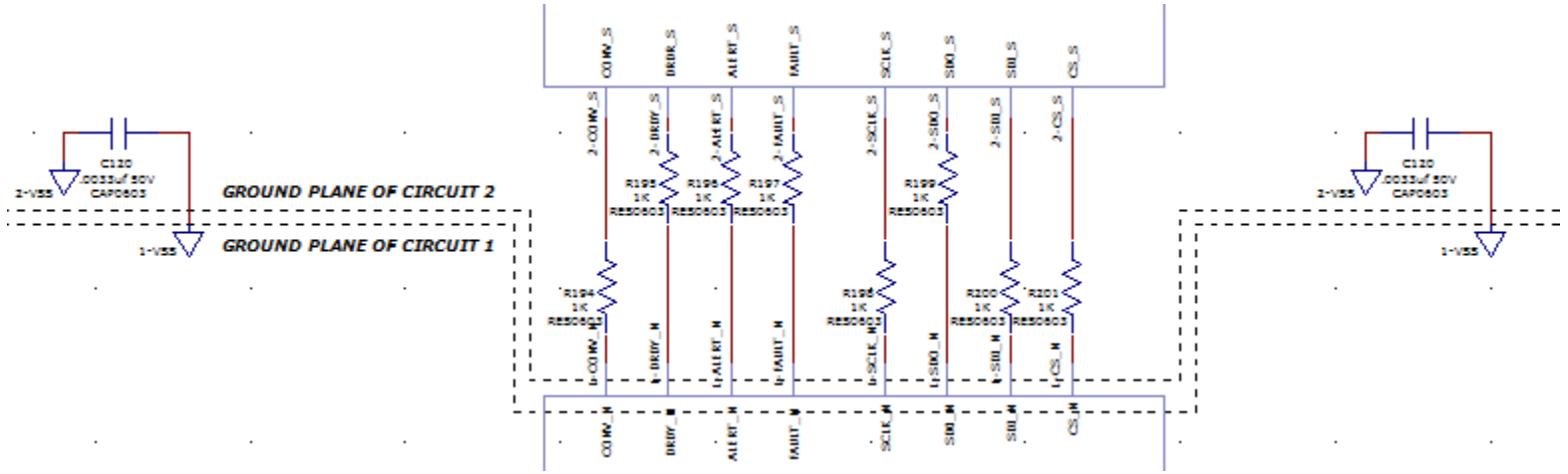
- Always follow standard IEC practices for PCB design, including recommendations for isolation of high voltages.

- Add Transient Voltage Suppression from Cell1(-) to Cell6(+) for each IC in the stack. This is best implemented as a ~5.1 to 5.6V TVS-type zener diode across each cell input pair (i.e. VC0-1, VC1-2, etc).

- A capacitor across each cell in the stack is necessary to help protect the IC from ESD and to help protect the IC during random hot-plug cell connections. These connections occur as a result of connector pins making contact randomly as the male-female connectors are joined. This results in a random, and changing voltage across the IC pins during connection. The capacitors form a fast voltage divider to help distribute the voltage evenly.

2.2 Ground Planes

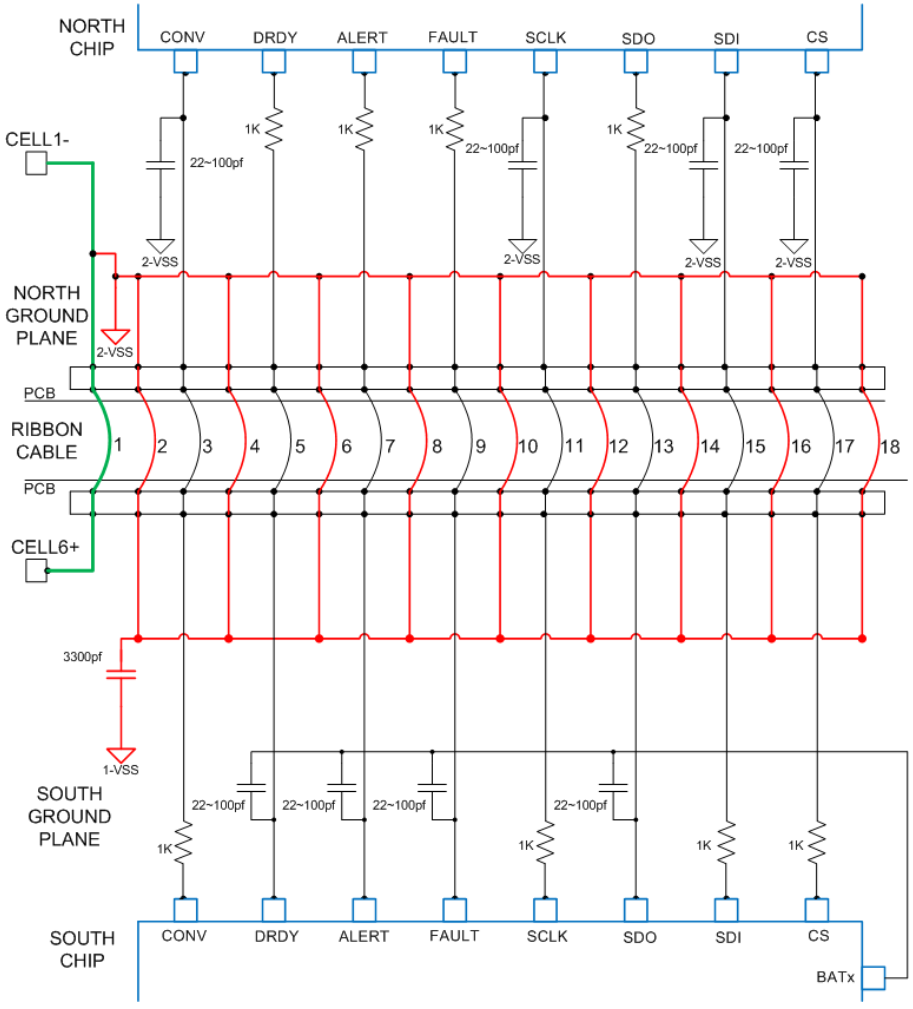
- A multilayer board with proper Ground Plane(s) is required for correct performance. The ground plane should extend fully under the IC, and be connected to the power tab for good thermal performance.
- The ground plane from a “North” IC should extend under the communications signals from the North IC all the way to the “South” IC for best communications performance. The signals between two IC are referenced to the VSS of the North IC.
- Add a low impedance AC connection between ground planes using 3.3nF-10nF capacitors between planes. This will reduce sensitivity to EMC (susceptibility). If the plane is relatively large, or highly rectangular similar to the TI HPA507Ex EVM, it is better to use two smaller capacitors than one large one. For small planes of a few square inches, a single capacitor is OK. The larger planes have higher inductance, and distributed capacitors offer slightly better performance.



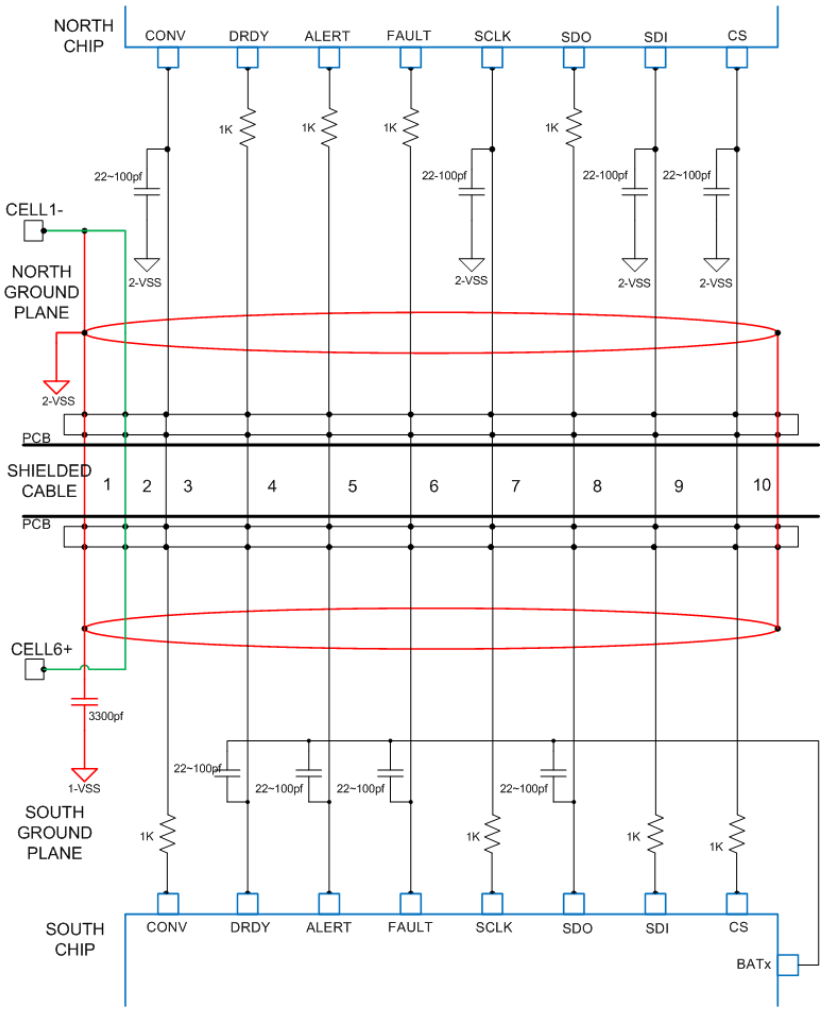
2.3 Communications & Cabling

- Use 1K resistors in series with each communications line in the vertical-communications path. Place these resistors close to the transmit pins (CS_N, SCLK_N, SDI_N, CONV_N, SDO_S, FAULT_S, ALERT_S, DRDY_S) of each IC. Values in the range 0R to 1K will work, the higher values provide better immunity to random hot-plug cell connections, 1K is recommended.
- Additional small capacitors should be added to the receive inputs of each IC (CS_S, SCLK_S, SDI_S, CONV_S, SDO_N, FAULT_N, ALERT_N, DRDY_N) to improve EMC (susceptibility) performance in the HF and VHF bands. Values are typically 22pf to 100pf maximum, 33pF is recommended. Note that the north receivers have the cap tied to BAT, the south receivers connect the cap to VSS. These capacitors may lower the potential communications speed. Please refer to the tables in the Application Brief “Improving Communications in the bq76PL536.pdf”.
- If cabling is added between IC’s, it should be the minimum length required, and avoid running near high-energy noise sources such as battery or cell bus-bars, other communications cables, etc. Any cable added forms an antenna for reception of out-of-band signals which may interfere with IC-to-IC communications.
- Ribbon-type cables should use inter-digitated grounds - every other wire should be VSS from the “North” IC of the pair. On the “South” end, the VSS (grounds) should be combined, and connected via 10nF capacitor to the VSS signal of the South IC.
- Round cables should use stranded conductors, 22ga or larger, inside a shielded outer jacket. The shielding provides a more uniform impedance for each conductor. Conductors should not be twisted pair, unless one conductor from each pair is connected to VSS of the North IC as mentioned above for ribbon cable. The shield or VSS signals should be connected to the South IC VSS plane using a 10nF capacitor.

2.4 Cabling Considerations



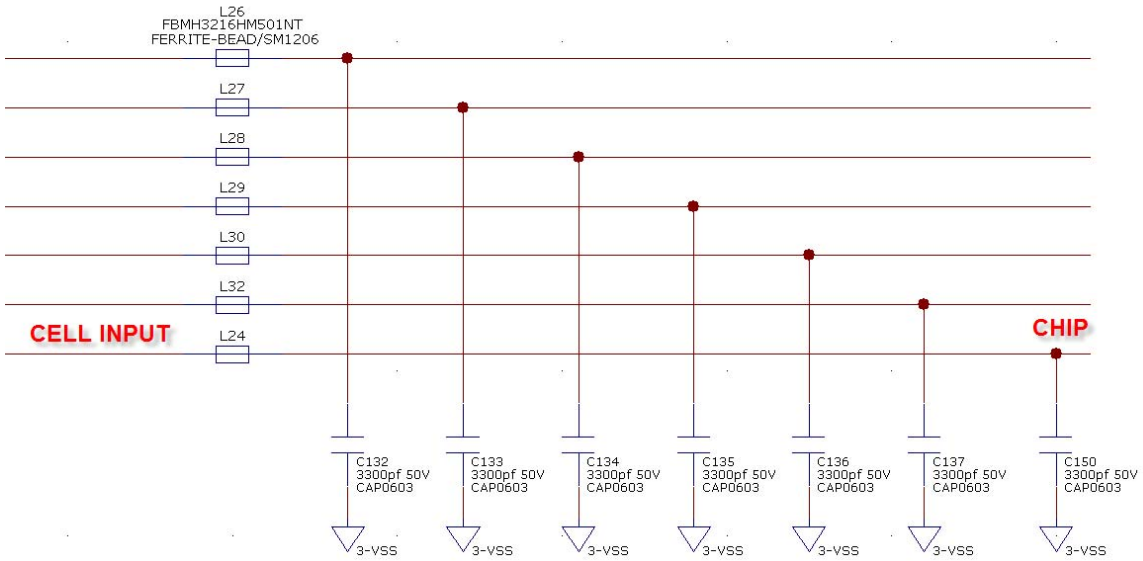
Ribbon Cable Design



Shielded Round Cable Design

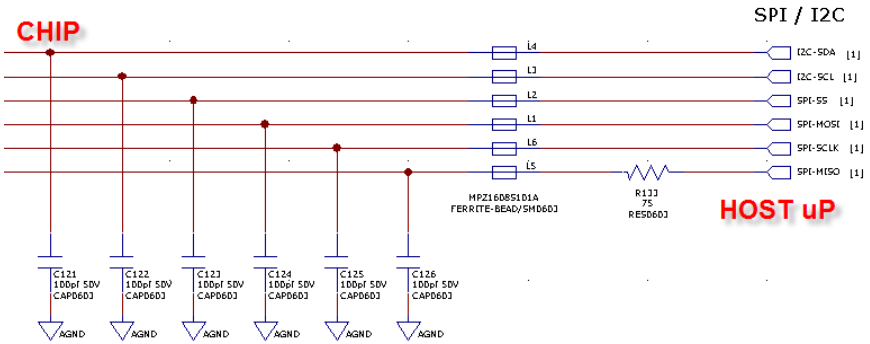
2.5 EMC Susceptibility on Cell Inputs

- Use ferrite beads or small inductors in series with the cell inputs. The bead and small capacitor should be located near each other.
- Add a 0.0033uf capacitor from each cell input to the VSS (cell1-) of that IC. This value may need adjustment for your PCB layout and field conditions.
- These components are necessary to improve EMC performance in automotive applications in electrically noisy environments.



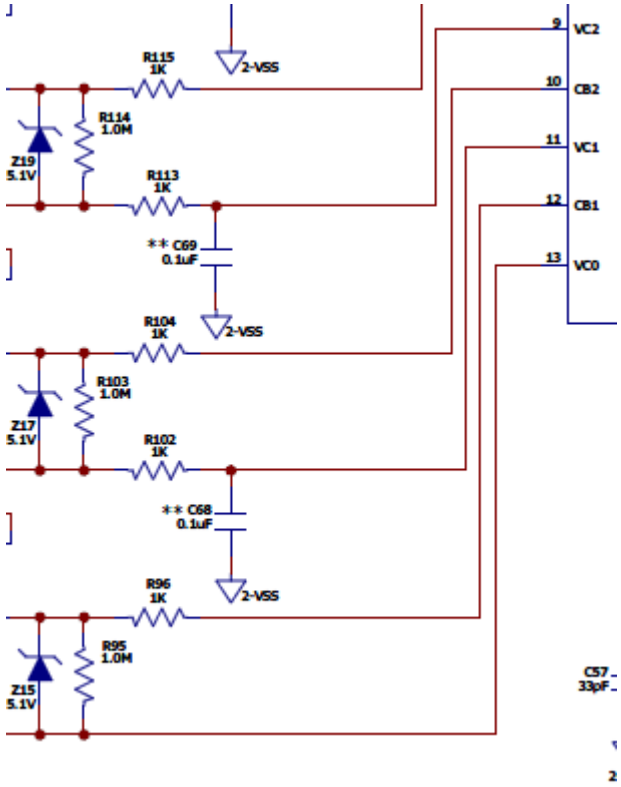
2.6 Filter Components

- Keep low-pass filter components close to the IC wherever possible, especially the capacitors.
- An inductor or ferrite bead should usually be added to SPI_H connections to host CPU. An RC (substitute R for L) may be just as effective and less expensive, but requires an empirical approach; the values depend on cable type used. For ribbon cable, ~110 ohms and 100-560pF is a good starting point.
- The 75Ω resistor on the SPI-MISO signal is recommended for most applications to further reduce ringing.
- If a galvanic isolator is used such as the TI ISO7241, 100-330R series resistors should be added between the ISO part and the ‘536 to reduce ringing.



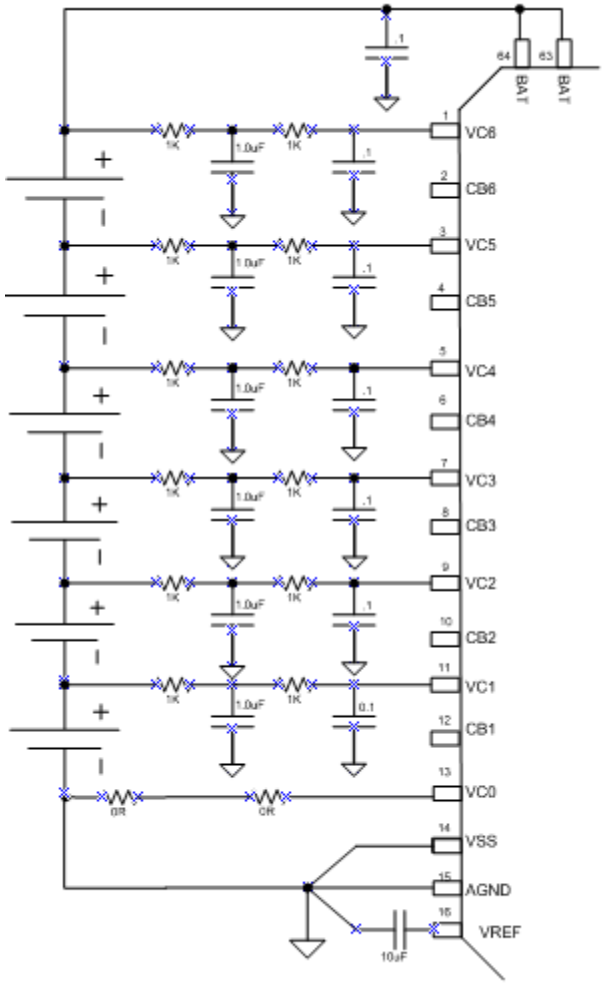
2.7 V_{CELL} Nyquist Filter

- Basic circuit: single pole RC filter at ~10kHz using 1KΩ + 100nF.



2.8 Improved V_{CELL} Nyquist Filter

- Enhanced performance filter: Addition of this simple two pole filter decreases the noise bandwidth and measurement error introduced by the typical inverter noise and multiplexed ADC readings.
- The two pole filter is created by adding a ~1kHz filter to the basic one by using 1KΩ + 1.0µF preceding the basic filter. The lower Z filter should be inserted ahead of the higher impedance filter. Capacitor values must remain at minimum 100nF to support ADC switched-cap input.
- Better coherence with the pack current measurement is possible.



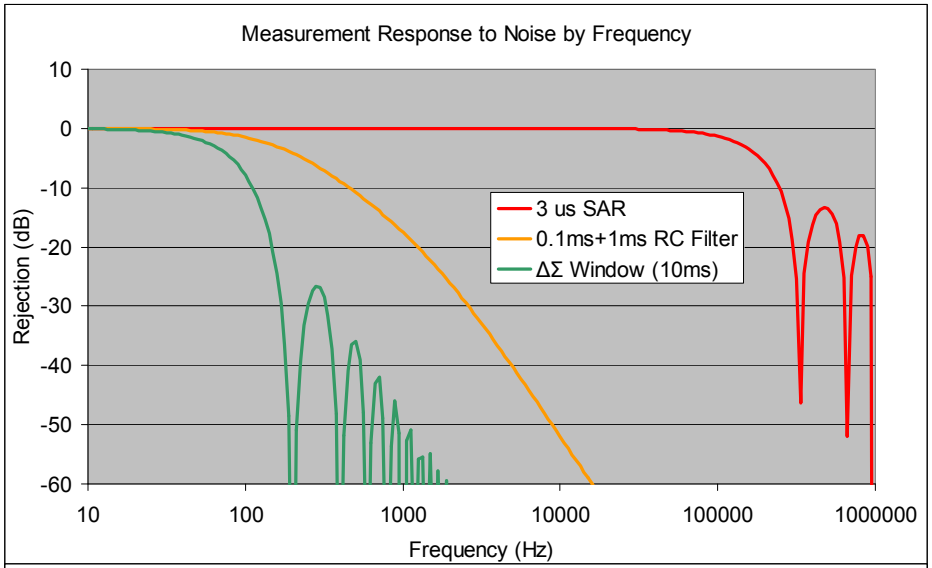
2.9 Improved Filter, Frequency Domain

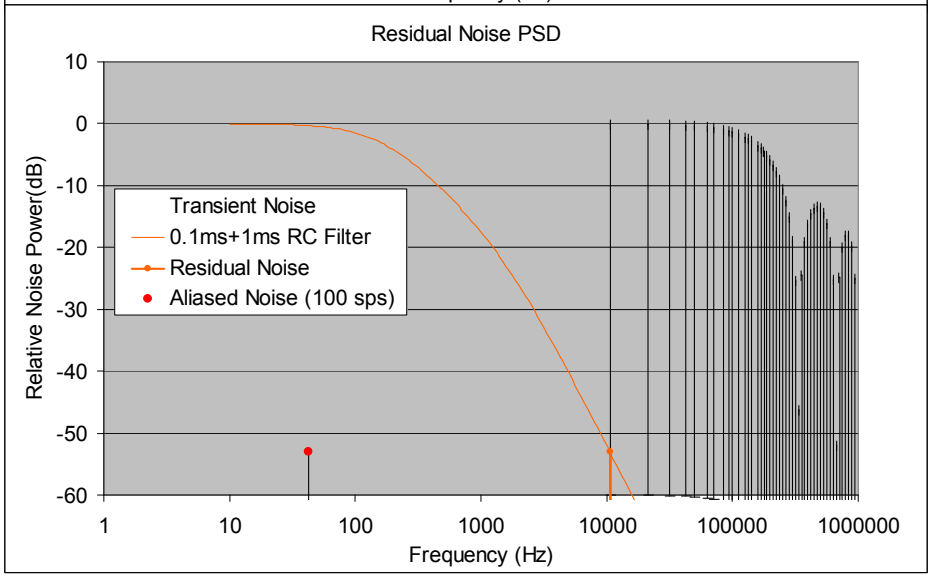
- **Improving the Noise rejection for the SAR**
- Consider 2 pole (Dual RC) input filter to provide further rejection

- **SAR + Dual RC Provides…**

  > 50 dB rejection of Transient Noise @10kHz

  1v Transients at the cell result in ~1mV error

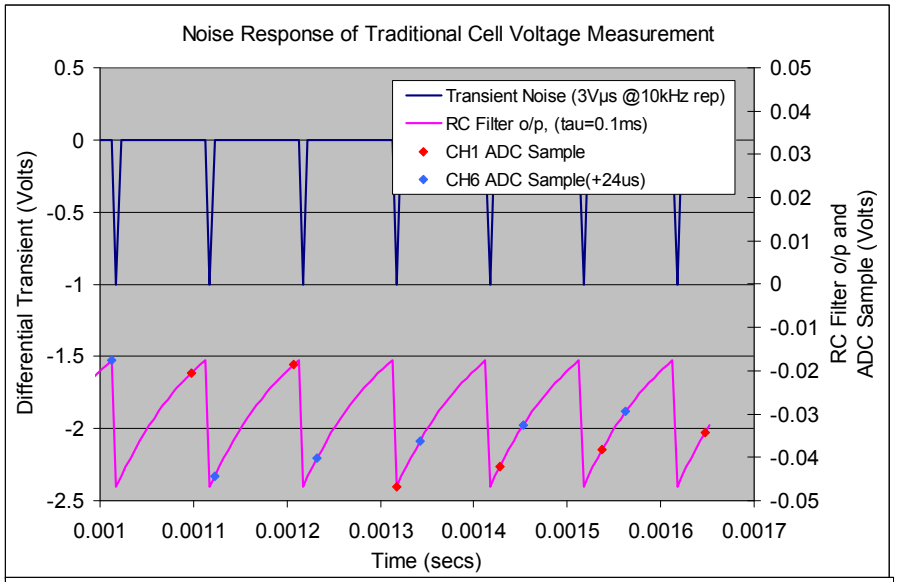


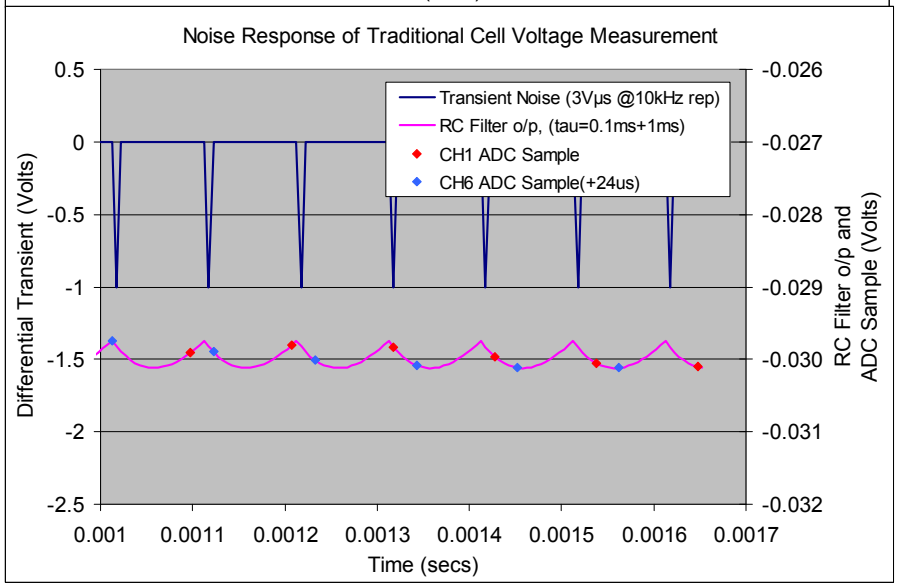


2.10 Improved Filter, Time Domain

- Improving the Noise rejection for the SAR
- Scenario
  - 3Vμs transient,10kHz rep
  - 2 pole (Dual RC) input filter to provide further rejection

- Resulting Performance :
  - ~1mv pp ADC input Noise
  - Negligible Delta between Cells



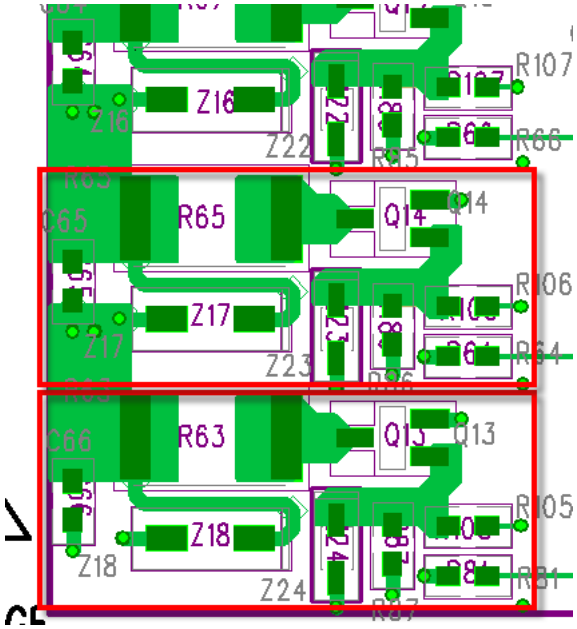


3.1General Guidelines

- Always follow standard IPC practices for layout spacing and current capabilities.
  a) IPC-M-106 Technology Reference for Design Manual
- Add ground planes and extra copper as shields on circuit board to improve EMC.
  a) At high frequencies, Capacitors become inductive, Inductors become capacitive and Resistors become capacitive or inductive.
  b) At high frequencies, stand-alone wires/traces become inductive, and then become antennas (that's why we need proper ground planes and shielding)
- Proper Power PAD™ layout is essential for low noise and proper thermal control. See the Power PAD reference page in this document.
- ICs can be damaged due to magnetic and capacitive coupling from high current paths. Generally keep the IC away from sources of high inductance or magnetic fields.
- It will be necessary to know the power dissipation of the cell balancing components. Allow enough copper near pads to act as heat sinking for your power components (FET and resistor). Design or add heat sinks as needed. (Note: Using the copper on the PCB as a heat sink can affect the temperature rise of the entire circuit. Know the temperature characteristics and limits of your circuit, and design accordingly). Generally keep heat away from the '536 to lessen the effects on the measurement circuit performance.

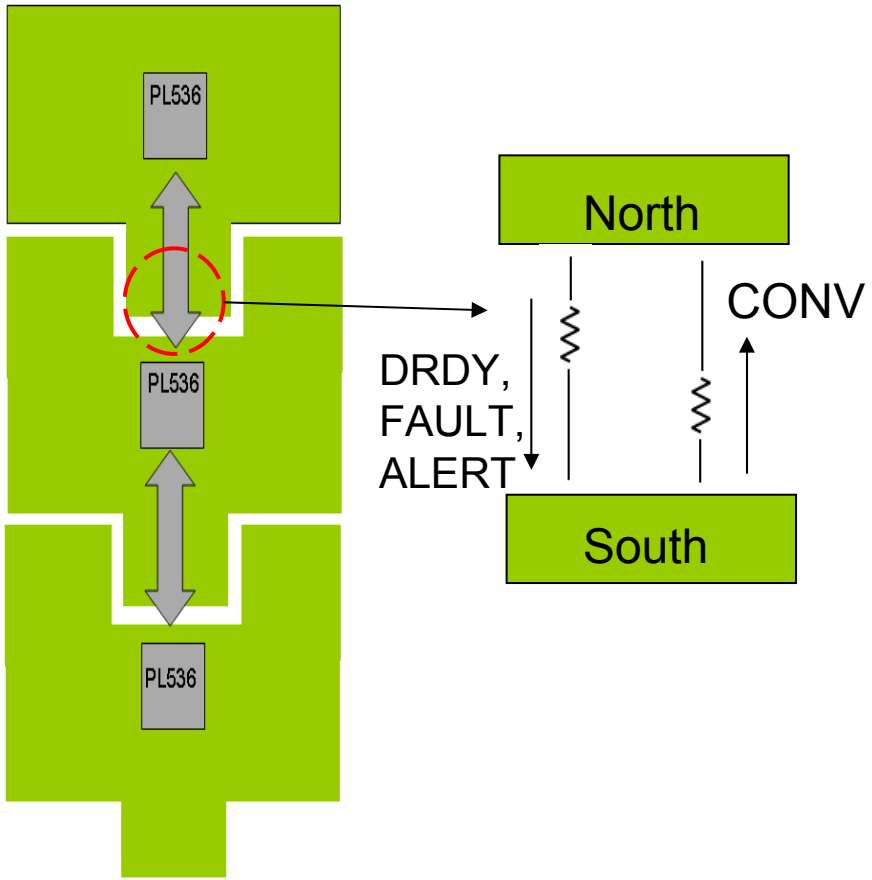
Layout – General Guidelines Con't.

- Keep cell balancing circuit components in a tight grouping.
- Use tracks sized to carry the current and help dissipate heat.
- The tracks should be large enough to handle the current of the cell balancing with less than a 10 deg C rise.
- For balancing, several power resistors in parallel perform better than a single resistor by dissipating heat over a larger surface area.
- The vertical bus communications connections between the IC's should be should be as short and direct as possible. Keep these away from other noise sources in the system, and on the board.



3.2 Ground Planes

- Proper ground plane design is necessary to protect signal integrity and keep noise impact on EMC performance at a minimum.
- Each chip in the circuit needs to have it's own ground plane, referenced to the Cell1 negative terminal of the lowest cell in it's 6 cell stack.
  a. For the most south circuit the ground reference is cell1-.
  b. For the second circuit it's ground plane reference will be cell7- (cell6+)
  c. The third circuit will use cell13- (cell12+) for it's ground plane and so on.
- Each ground plane must be separate and isolated from the other ground planes physically but must be connected through a capacitor electrically.
- A good ground (VSS) plane should have a dedicated layer and extended from the North IC under it's vertical-comm's tracks down to next IC to the south in the stack.



3.3 PowerPAD™ “PAP” Package

- The PowerPAD package is a thermally enhanced standard size IC package designed to eliminate the use of bulky heat sinks and slugs traditionally used in thermal packages. This package can be easily mounted using standard printed circuit board (PCB) assembly techniques, and can be removed and replaced using standard repair procedures.
- The PowerPAD package is designed so that the leadframe die pad (or thermal pad) is exposed on the bottom of the IC. This provides an extremely low thermal resistance (θJC) path between the die and the exterior of the package. The thermal pad on the bottom of the IC can then be soldered directly to the printed circuit board (PCB), using the PCB as a heat sink. In addition, through the use of thermal vias, the thermal pad can be directly connected to a ground plane or special heat sink structure designed into the PCB.

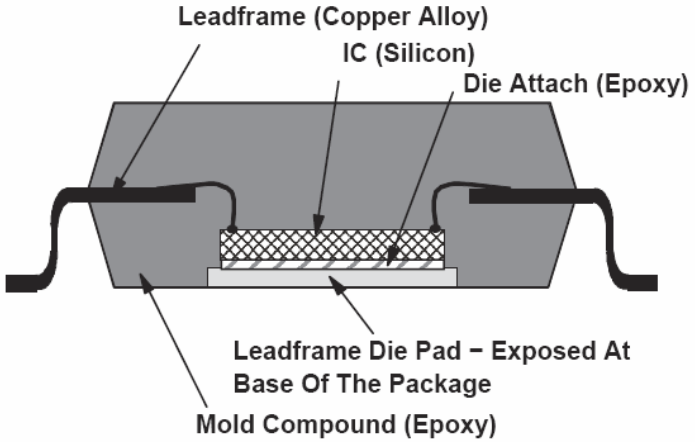
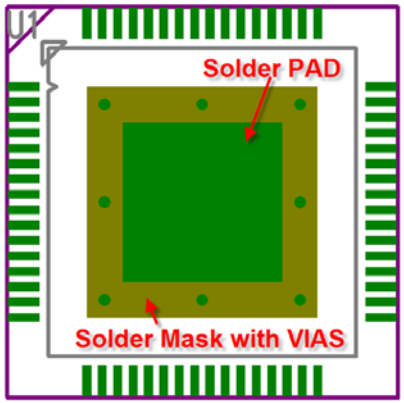


Figure 1. Section View of a PowerPAD Package



- For more information and proper foot print design see:
  - Application Report SLMA002E–November 1997–Revised January 2010
  - Application Brief SMLA004B